MDS105

Unmanaged 5-Port 10/100 Mbps Ethernet Switch

Data Sheet

February 2003

Features

- 4 10/100Mbps auto-negotiating RMII ports
- 1 10/100Mbps auto-negotiating MII/serial port (port 4) that can be used as a WAN uplink or as a 5th port
- External I^2C EEPROM for power-up configuration
  - Default mode allows operation without external EEPROM
- Up to 4 port-based VLANs
- Full wirespeed layer 2 switching on all ports (up to 1.448M packets per second)
- Internal 1k MAC address table
  - Auto address learning
  - Auto address aging
- Leading edge QoS capabilities provided based on 802.1p and IP TOS/DS field
  - 2 queues per output port
  - Packet scheduling based on Weighted Round-Robin (WRR) and Weighted Random Early Detection/Drop (WRED)
  - Without flow control can drop packets during congestion using WRED
  - 2 levels of packet drop provided
- Supports both Full/Half duplex ports
- Supports external parallel port for configuration updates
- Port 3 can be used to mirror traffic from the other 3 ports (0-2)

Ordering Information

MDS105AL 208 Pin PQFP

-40°C to +85°C

- Provides port-based prioritization of packets on up to 2 ports (0-1)
  - Input ports are defined to be high or low priority
  - Allows explicit identification of IP Phone ports
- Ports 0 & 1 can be trunked to provide a 200Mbps link to another switch or server
- Utilizes a single low-cost external SSRAM for buffer memory
  - 256k bytes or 512k bytes (1 chip)
- Flow Control capabilities
  - Provides back pressure for half-duplex
  - 802.3x flow control for full-duplex
- Special power-saving mode for inactive ports
- Ability to support WinSock2.0 and Windows2000 smart applications
- Transmit delay control capabilities
  - Provides maximum delay guarantee (<1ms)
  - Supports mixed voice-data networks
- Optimized pin-out for easy board layout

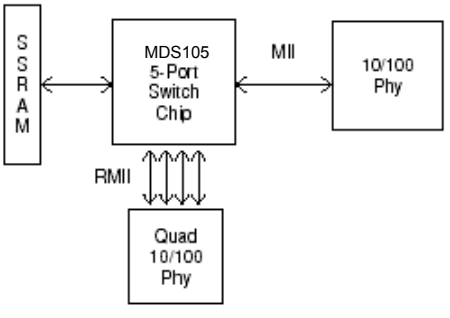


Figure 1 - System Block Diagram

Description

The MDS105 is a fully integrated 5-port Ethernet switch designed to support the low-cost requirements of unmanaged switch applications. The MDS105 provides features that are normally not associated with plug-and-play technology, while not requiring an external processor to facilitate their utilization.

The MDS105 begins operating immediately at power-up, learning addresses automatically, and forwarding packets at full wire speed to any of its four output ports or the uplink expansion port. The default configuration allows operation without using an external EEPROM.

With an EEPROM to configure the device at power up, however, the MDS105 provides flexible features: port trunking, port mirroring, port-based VLANs, and Quality of Service (QoS) capabilities that are usually associated only with managed switches.

The built-in intelligence of the MDS105 allows it to recognize and offer packet prioritization using Zarlink's QoS scheme. Packets are prioritized based upon their layer 2 VLAN priority tag or the layer 3 Type-Of-Service/Differentiated Services (TOS/DS) field. This priority can be defined as transmit and/or drop priority.

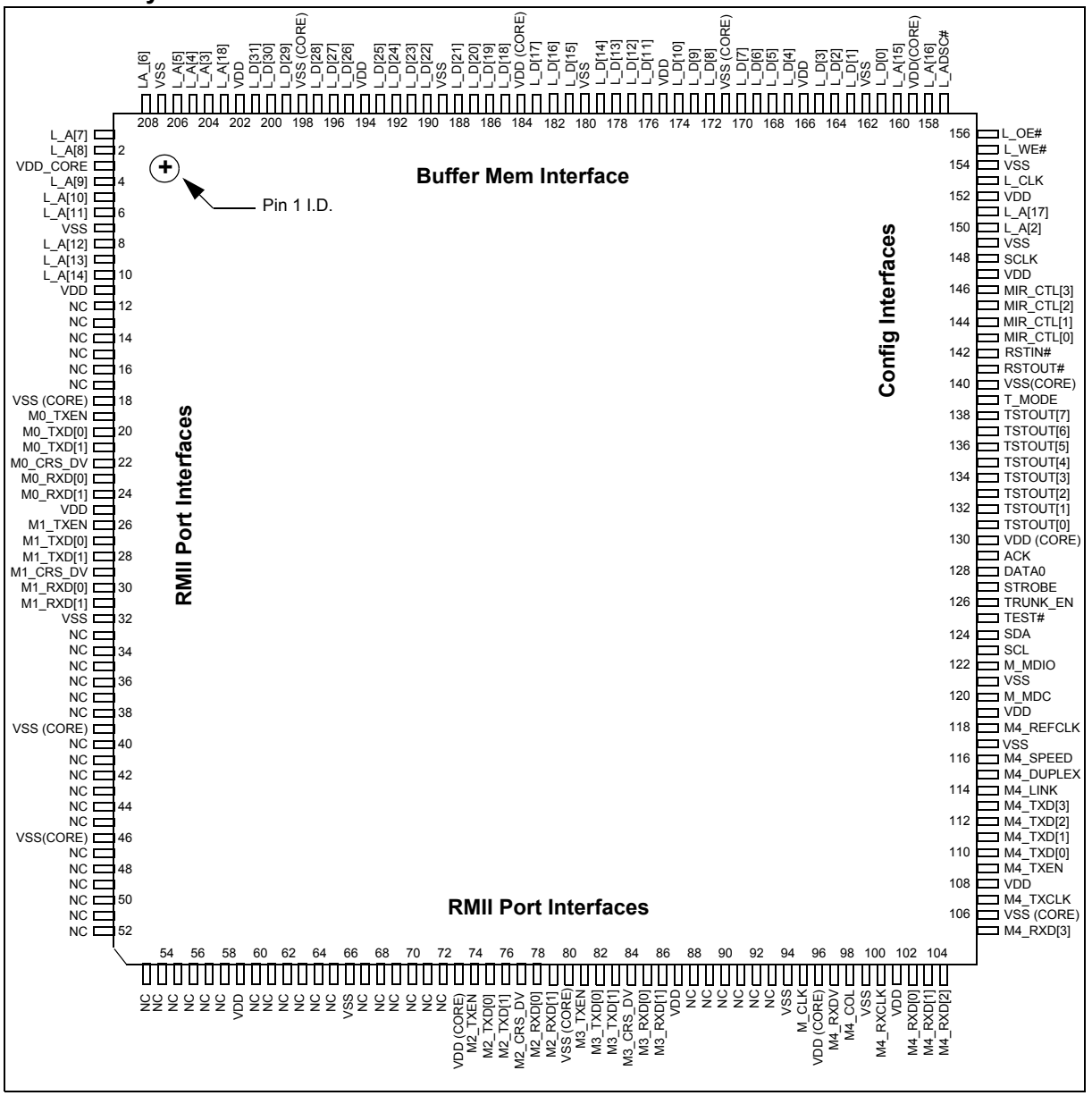
The MDS105 can be used to create an 4 port unmanaged switch with one WAN router port by connecting a CPU (ARM or MPC 850) to the additional MII port (port 4). The only external components needed are the physical layer transceivers and a single SSRAM, resulting in a low total system cost.

Designed to support the requirements of converging networks, the MDS105 utilizes a power conserving architecture. To further enhance this power management, the chip automatically detects when a switch port is not being utilized, and turns off the logic associated with that port, thereby saving power and reducing the current load on the switch power supply.

Operating at 66 MHz internally, and with a 66 MHz interface to the external SSRAM, the MDS105 sustains full wire-speed switching on all five ports.

The chip is packaged in a small 208 pin Plastic Quad Flat-Pak (PQFP) package.

MDS105 Physical Pinout



PIN Reference Table

Pin #	Pin Name
1	L_A[7]
2	L_A[8]
3	VDD (CORE)
4	L_A[9]
5	L_A[10]
6	L_A[11]
7	VSS
8	L_A[12]
9	L_A[13]
10	L_A[14]
11	VDD
12	NC
13	NC
14	NC
15	NC
16	NC
17	NC
18	VSS (CORE)
19	M0_TXEN
20	M0_TXD[0]
21	M0_TXD[1]
22	M0_CRS_DV
23	M0_RXD[0]
24	M0_RXD[1]
25	VDD
26	M1_TXEN
27	M1_TXD[0]
28	M1_TXD[1]
29	M1_CRS_DV
30	M1_RXD[0]
31	M1_RXD[1]
32	VSS
33	NC
34	NC
35	NC
36	NC
37	NC
38	NC
39	VDD (CORE)
40	NC
41	NC
42	NC
43	NC
44	NC
45	NC
46	VSS (CORE)
47	NC
48	NC
49	NC
50	NC
51	NC
52	NC
53	NC
54	NC
55	NC
56	NC
57	NC
58	NC
59	VDD
60	NC
61	NC
62	NC
63	NC
64	NC
65	NC
66	VSS
67	NC
68	NC
69	NC
70	NC
71	M5_RXD[0]
72	M5_RXD[1]
73	VDD (CORE)
74	M6_TXEN
75	M6_TXD[0]
76	M6_TXD[1]
77	M6_CRS_DV
78	M6_RXD[0]]
79	M6_RXD[1]
80	VSS (CORE)
81	M7_TXEN
82	M7_TXD[0]
83	M7_TXD[1]
84	M7_CRS_DV
85	M7_RXD[0]
86	M7_RXD[1]
87	VDD
88	NC
89	NC
90	NC
91	NC
92	NC
93	NC
94	VSS
95	M_CLK
96	VDD (CORE)
97	M8_RXDV/S8_CRS_DV
98	M8_COL/S8_COL
99	VSS
100	M8_RXCLK/S8_RXCLK
101	VDD
102	M8_RXD[0]/S8_RXD
103	M8_RXD[1]
104	M8_RXD[2]
105	M4_RXD[3]
106	VSS (CORE)

107	M8_TXCLK/S8_TXCLK
108	VDD
109	M8_TXEN[0]/S8_TXEN
110	M8_TXD[0]/S8_TXD
111	M8_TXD[1]
112	M8_TXD[2]
113	M8_TXD[3]
114	M8_LINK/S8_LINK
115	M8_DUPLEX/S8_DUPLEX
116	M8_SPEED
117	VSS
118	M8_REFCLK
119	VDD
120	M_MDC
121	VSS
122	M_MDIO
123	SCL
124	SDA
125	TEST#
126	TRUNK_ENABLE
127	STROBE
128	DATA0
129	ACK
130	VDD (CORE)
131	TSTOUT[0]
132	TSTOUT[1]
133	TSTOUT[2]
134	TSTOUT[3]
135	TSTOUT[4]
136	TSTOUT[5]
137	TSTOUT[6]
138	TSTOUT[7]
139	T_MODE
140	VSS (CORE)
141	RSTOUT#

142	RSTIN#
143	MIRROR_CONTROL[0]
144	MIRROR_CONTROL[1]
145	MIRROR_CONTROL[2]
146	MIRROR_CONTROL[3]
147	VDD
148	SCLK
149	VSS
150	L_A[2]
151	L_A[17]
152	VDD
153	L_CLK
154	VSS
155	L_WE#
156	L_OE#
157	L_ADSC#
158	L_A[16]
159	VDD (CORE)
160	L_A[15]
161	L_D[0]
162	VSS
163	L_D[1]
164	L_D[2]
165	L_D[3]
166	VDD
167	L_D[4]
168	L_D[5]
169	L_D[6]
170	L_D[7]
171	VSS (CORE)
172	L_D[8]
173	L_D[9]
174	L_D[10]
175	VDD
176	L_D[11]
177	L_D[12]

178	L_D[13]
179	L_D[14]
180	VSS
181	L_D[15]
182	L_D[16]
183	L_D[17]
184	VDD (CORE)
185	L_D[18]
186	L_D[19]
187	L_D[20]
188	L_D[21]
189	VSS
190	L_D[22]
191	L_D[23]
192	L_D[24]
193	L_D[25]
194	VDD
195	L_D[26]
196	L_D[27]
197	L_D[28]
198	VSS (CORE)
199	L_D[29]
200	L_D[30]
201	L_D[31]
202	VDD
203	L_A[18]
204	L_A[3]
205	L_A[4]
206	L_A[5]
207	VSS
208	L_A[6]

MDS105 Block Diagram

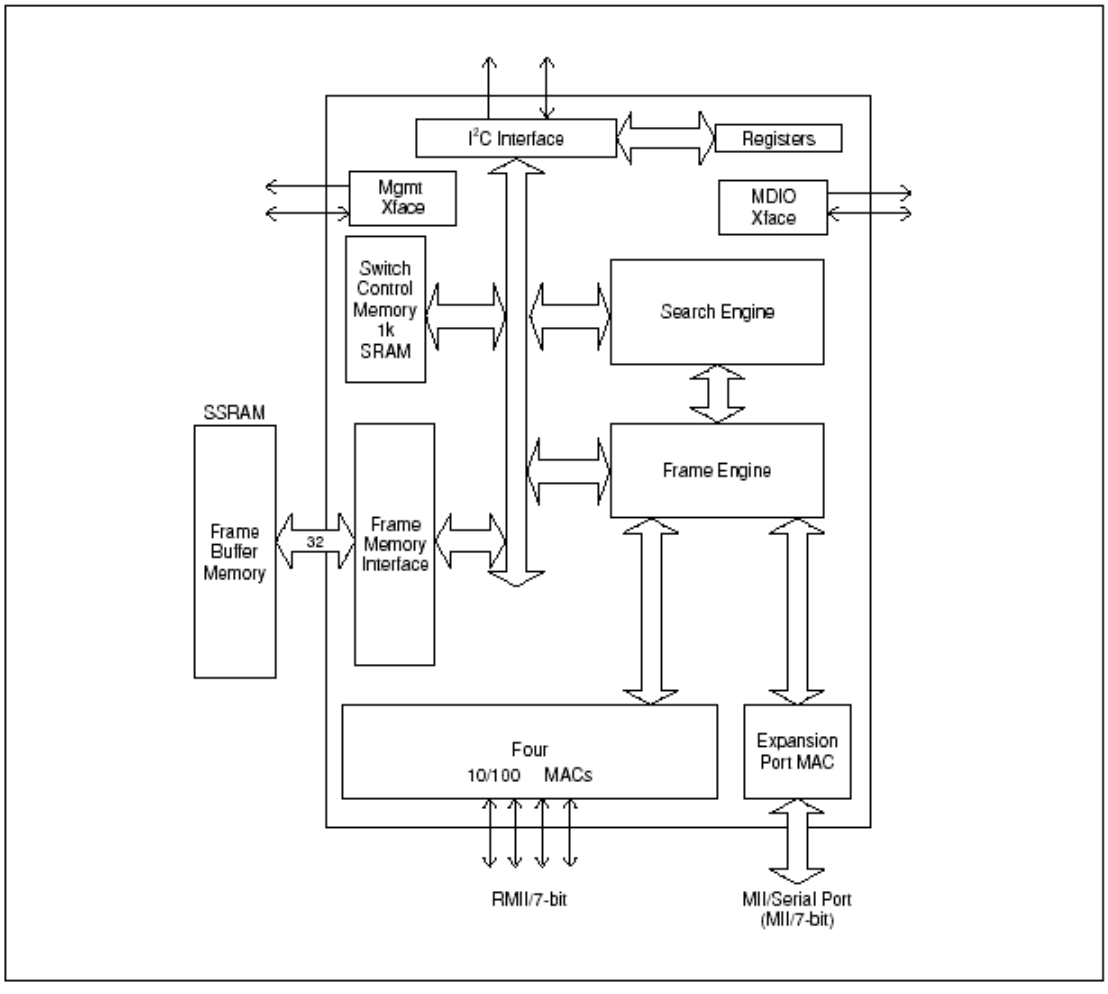


Figure 2 - MDS105 Block Diagram

1.0 Functional Operation

The MDS105 is designed to provide a cost effective layer 2 switching solution, using technology from the Zarlink family to offer a highly integrated product for the unmanaged, Differentiated Services (DS) ready, Ethernet switch market.

Five 10/100 Media Access Controllers (MAC) provide the protocol interface. These MACs perform the required packet checks to ensure that each packet that is provided to the Frame Engine has met all the IEEE 802.1 standards. Each MAC supports half duplex “back pressure,” and full duplex 802.3x “PAUSE” Flow Control.

Data packets longer than 1518 (1522 with VLAN tag) bytes and shorter than 64 bytes are dropped, and the MDS105 is designed to support minimum interframe gaps between incoming packets. The Frame Engine (FE) is the primary packet buffering and forwarding engine within the MDS105. As such, the FE controls the storage of packets into and out of the external frame buffer memory, keeps track of frame buffer availability, and schedules packet transmissions. While packet data is being buffered, the FE extracts the necessary information from each packet header and sends it to the Search Engine for processing. Search results returned to the FE initiate the scheduling of packet transmission. When a packet is chosen for transmission, the FE reads the packet from external buffer memory and places it in the output FIFO of the output port.

2.0 Address Learning and Aging

The MDS105 is able to begin address learning and packet forwarding shortly after power up is completed. The Search Engine examines the contents of its internal Switch Database Memory for each valid packet that is received on a MDS105 input port.

Unknown source and destination MAC addresses are detected when the Search Engine does not find a match within its database. These unknown source MAC addresses are learned by creating a new entry in the switch database memory, and storing the necessary resulting information in that location. Subsequent searches to a learned destination MAC address will return the new contents of that MAC Control Table (MCT) entry.

After each source address search the MCT entry aging flag is updated. MCT entries that have not been accessed during a user configurable time period (1 to 67,108 seconds) will be removed. This aging time period can be configured using the 16-bit value stored in the registers MAC Address Aging Timer Low and High (AGETIME_LOW, AGETIME_HIGH). The aging period is defined as the bit concatenation of AGETIME_HIGH with AGETIME_LOW, multiplied by 1024 ms. For example, if AGETIME_LOW = 25, and AGETIME_HIGH = 01 (in hexadecimal), then the concatenated value 125 is equal to decimal 293. Multiplying 293 by 1024 ms, we determine that the corresponding aging time is 300 ms. In fact, 300 ms is the default aging time for the MDS105.

The aging of all MCT entries is checked once during each time period. If the MCT entry has not been exercised before the end of the next time period, it will be deleted.

3.0 Quality of Service

The MDS105 applies Zarlink’s architecture to provide new Quality of Service (QoS) capabilities for unmanaged switch applications. Similar to the QoS capabilities of other Zarlink chipset members, the MDS105 offers two transmit queues per output port.

The Frame Engine (FE) manages the output transmission queues for all MDS105 ports. Once the destination address search is complete, and the switch decision is sent back to the FE, the packet is inserted into the appropriate output queue. Whether the packet is inserted into a high or low priority queue is determined by either the VLAN tag information or the Type of Service/Differentiated Services (TOS/DS) field in the IP header. Either of these priority fields can be used to select the transmission priority (as per the USE_TOS bit in the FCR register). The mapping of the priority field values into either the high or low priority queue can be configured using the MDS105 configuration registers AVPM and TOSPM.

If the system uses the TOS/DS field to prioritize packets, there are two choices regarding which bits of the TOS/DS field are used. Bits [0:2] of the TOS byte (known as the IP precedence field) or bits [3:5] of the TOS byte (known as the Delay/Throughput Reliability, DTR, field) can be used to resolve the transmission queue priority. Either bit group, [0:2] or [3:5], can also be used to resolve packet drop precedence, as per bits 6 and 7 of the register FCBST.

The MDS105 utilizes Weighted Round Robin (WRR) to schedule packets for transmission. To enable MDS105's intelligent QoS scheduling capabilities requires the use of an external EEPROM to change the default register configurations.

Weighted Round Robin is an efficient method to ensure that each of the transmission queues receives at least a minimum service level. With two output transmission queues, the MDS105 will transmit X packets from the high priority queue before transmitting a single packet from the low priority queue. The MDS105 allows the designer to set the high priority weight X to a value between 1 and 15. If both queues contain packets, and the high priority weight is set to the value 4, then the MDS105 will transmit 4 high priority packets before transmitting each low priority packet.

The MDS105 also employs a proprietary mechanism to ensure the timely delivery of high priority packets. When the latency of high priority packets reaches a threshold, the MDS105 will override the WRR weights and transmit only high priority packets until the high priority packet delays are below the threshold. This threshold limit is 1 ms (last-in-first-out). The MDS105's proprietary scheduling algorithm is also designed to push low priority traffic through the device faster, if necessary to unclog congested queues. Loading the appropriate values into the configuration registers enables the QoS scheduling capabilities of the MDS105. QoS for packet transmission is enabled by performing the following four steps:

1. Select the TOS/DS or VLAN Priority Tag field as the decision-maker for IP packet scheduling. The selection is made using bit 7 of the Flooding Control Register (FCR).
   - FCR[7] = 0: Use VLAN Priority Tag field to determine the transmission priority, if this Tag field exists.
   - FCR[7] = 1: Use TOS/DS field for IP packet priority resolution.
2. Select which TOS/DS subfield to use as the decision-maker for packet transmission priority if the TOS/DS field was selected in step 1. The selection is made using bit 6 of the FCB Buffer Low Threshold Register (FCBST).
   - FCBST[6] = 0: Use DTR subfield to resolve the transmission priority.
   - FCBST[6] = 1: Use IP precedence subfield[1] to resolve the transmission priority.
3. Enable QoS using bit 5 of the Transmission Scheduling Control Register (AXSC). Set the transmission queue weight for the high priority queue using bits 0 to 3.
4. Create the mapping from the value in the TOS/DS or VLAN Priority Tag field to the corresponding high or low priority output queue. The mapping is created using the VLAN Priority Map (AVPM) and TOS Priority Map (TOSPM) registers.

Note that for half duplex operation, the priority queues[2] must be enabled using bit 7 in the Transmission Scheduling Control (AXSC) register to use QoS scheduling.

When QoS and flow control are enabled, the MDS105 will utilize enhanced WRR to schedule packet transmission, and will use either back pressure or 802.3X flow control to handle buffer congestion. When QoS is enabled and flow control is disabled, the MDS105 will utilize enhanced WRR to schedule packet transmission, and will use Weighted Random Early Detection/Drop (WRED) to drop random packets in order to handle buffer congestion. Because of WRED, only a few packet flows are slowed down while the remaining see no impact from the network traffic congestion.

WRED is a method of handling traffic congestion in the absence of flow control mechanisms[3]. When flow control is enabled, all devices that are connected to a switch node that is exercising flow control are effectively unable to

1. IP precedence and DTR subfields are referred to as TOS/DS[0:2] and TOS/DS[3:5] in the IP TOS/DS byte.

2. In Half Duplex mode, QoS scheduling functions are disabled by default.

3. Flow control, of course, provides the advantage of not dropping packets. However, its primary disadvantage is that a flow controlled port may experience head-of-line blocking. This means that if even 1 packet is destined to a congested output port, then all other packets originating from the same source may, in the worst case, be delayed – even if these other packets have uncongested destinations. On the other hand, WRED may cause some packet loss, but with no such head-of-line blocking problem. Which method of handling traffic congestion should be chosen will depend on the application.

transmit, including nodes that are not directly responsible for the congestion problem. This inability to transmit during flow control periods would wreak havoc with voice packets, or other high priority packet flows, and therefore flow control is not recommended for networks that mix voice and data traffic.

WRED allows traffic to continue flowing into ports on a switch, and randomly drops packets with different probabilities based upon each packet's priority markings. As the switch congestion increases, the probability of dropping an incoming packet increases, and as congestion decreases, the probability of dropping an incoming packet decreases. Not surprisingly, packets designated high-drop are sacrificed with higher odds during congestion than packets designated low-drop.

The following table summarizes the WRED operation of the MDS105. It lists the buffer thresholds at which each drop probability takes effect.

	WRED Threshold		**Drop Percentage**	
	Condition for High Priority Queue	**Condition for Low Priority Queue**	**Drop Percentage for High-Drop Packet**	**Drop Percentage for Low-Drop Packet**
Level 0	Total buffer space available in device is ≤LPBT		50%	0%
Level 1	24 buffers occupied	72 buffers occupied	75%	25%
Level 2		84 buffers occupied	100%	50%

Table 1 - WRED Operation of the MDS105

The WRED packet drop capabilities of the MDS105 are enabled by performing the following four steps:

1. Select the TOS/DS or VLAN Tag field as the decision-maker for dropping packets. The selection is made using bit 7 of the Flooding Control Register (FCR).
   - FCR[7] = 0: Use VLAN Priority Tag field to resolve the drop level, if this field exists.
   - FCR[7] = 1: Use TOS/DS field for IP packet drop level resolution.
2. Select which TOS/DS Tag subfield to use for dropping packets provided that the TOS/DS field was selected in step 1. The selection is made using bit 7 of the FCB Buffer Low Threshold Register (FCBST).
   - FCBST[7] = 0: Use DTR subfield to resolve the drop precedence.
   - FCBST[7] = 1: Use IP precedence subfield to resolve the drop precedence.
3. Create the mapping from the values in the TOS DS or VLAN Tag field to the packet flags representing high or low drop precedence. The mapping is created using the VLAN Discard Map (AVDM) and TOS Discard Map (TOSDM) registers.
4. Make sure that the desired ports are flow control disabled, using the ECR1Px registers.

Note that to apply the WRED QoS function of the MDS105, flow control must be disabled.

3.1 A Few Examples

- **No QoS Scheduling Desired At All**. The default setting for the MDS105 is no QoS scheduling at all. Packets are transmitted using a simple first-in-first-out (FIFO) approach, without the reordering that would result from prioritization. All destinations use 1 queue only. QoS scheduling can be disabled for the entire chip using AXSC[5].
- **No QoS Scheduling Desired for Half-Duplex Ports.** It is possible to disable QoS for half duplex ports in the MDS105. Indeed, this is the default setting, because it is difficult to assure quality of service for half-duplex ports, which tend to experience unpredictable delay. All destinations configured as half-duplex use 1 transmission queue only in this setting. QoS scheduling can be disabled for all half-duplex ports using AXSC[7].
- **QoS Scheduling for Some Destinations, But Not Others.** The MDS105 does not support this feature. The three options offered are: (a) all ports are QoS-enabled, (b) no ports are QoS-enabled, and (c) only full-duplex ports are QoS-enabled. Of course, the MDS105 will still exhibit single-queue scheduling at a port if all packets destined for it are marked with a single transmission priority.
- **No Flow Control Desired**. It is possible to disable flow control for the entire chip, regardless of the individual port settings. During congestion, some packets will be lost. This capability is located in AXSC[6].
- **Flow Control Desired for Some Sources, But Not Others.** By configuring each port separately using bit 0 in the ECR1Px registers, one may enable flow control for some ports, but not others. Flow control cannot be globally disabled in AXSC[6] if this function is to be achieved. At a congested destination, an incoming packet from a flow control enabled source will trigger a flow control message sent back to that source. On the other hand, an incoming packet from a flow control disabled source may or may not be dropped, as per WRED, but will never trigger flow control.
- **Scheduling vs. Dropping.** Using the configuration registers in the MDS105, as in earlier examples, a port may or may not have flow control enabled, and a port may or may not have QoS scheduling enabled. All four combinations are permissible parameter settings, and which one is chosen depends on application. In one common application, suppose voice, critical data, and web traffic packets originate from the same set of input ports, and are destined for the same set of output ports. The MDS105's enhanced WRR scheduling can be used to ensure a delay bound for the voice packets. Furthermore, because we want to guarantee that web traffic congestion does not block critical data or voice, we must disable flow control and use WRED to intelligently drop packets.

On the other hand, if the goal were file transfer without any packet dropping, one would enable the MDS105's flow control function, which halts incoming traffic when the system is congested. QoS scheduling can be disabled, both because flow control may make quality of service unpredictable, and because, in any case, delay is not critical in this application.

3.2 Port-Based Prioritization

Some applications may require an explicit prioritization of packets based upon the port the packet originates from. Defining specific ports of a switch to be IP Phone ports is a specific example that makes use of MDS105's ability to assign default priorities to ports.

The MDS105 can be configured to provide specific priority definitions on up to two ports (ports 0 – 1). These user defined port priorities override the packet priority markings (VLAN tag or TOS/DS), and the new priority is applied to all packets that enter the switch from that port. These port priority definitions are configured in the Port Priority (PTPRI) register. There are two bits for each of the two ports that can support port-based priorities. The EN bit allows the designer to turn on port priorities for each port, and the P bit allows the designer to select either high (1) or low (0) transmission priority for all packets that enter the switch through that port.

When port priorities are enabled, the remaining ports will provide QoS based upon the VLAN Tag or TOS DS field mappings in the configuration registers. Only those ports that have port priorities enabled will override the priority mappings.

4.0 Buffer Management

The MDS105 stores each input packet into the external frame buffer memory while determining the destination the packet is to be forwarded to. The total number of packets that can be stored in the frame buffer memory depends upon the size of the external SSRAM that is utilized. For a 256 KB SSRAM the MDS105 can buffer 170 packets. For a 512 KB SSRAM the MDS105 can buffer 340 packets.

In order to provide good quality of service characteristics, the MDS105 must carefully allocate the available buffer space. Such careful allocation can be accomplished using the external EEPROM to load the appropriate values into the MDS105 configuration registers. The Low Drop Precedence Buffer Threshold (LPBT) register assures that traffic designated as low-drop actually receives reserved buffer space. The designer can set the minimum number of buffers reserved for low-drop unicast traffic, by setting this register with a value between 0 and 255. Unreserved buffers are treated as shared, and are accessible to all types of incoming traffic.

To set the maximum number of buffers permitted for all multicast packets, use the Multicast Buffer Control Register (MBCR). Unlike the LPBT register, the MBCR register does not define a reserved area of buffer memory, but instead provides a bound on the number of multicast packets that can be buffered at any one time.

During operation the MDS105 will continuously monitor the amount of frame buffer memory that is available, and when the unused buffer space falls below a designer configurable threshold, the MDS105 will initiate flow control if enabled or WRED if not. This threshold is set using the FCB Buffer Low Threshold (FCBST) register.

5.0 Virtual LANs

The MDS105 provides the designer the ability to define a single port-based Virtual LAN (VLAN) for each of the five ports. This VLAN is individually defined for each port using the Port Control Registers (ECR1Px[6:4]). Bits [6:4] allow the designer to define a VLAN ID (value between 0 – 3) for each port.

When packets arrive at an input of the MDS105, the search engine will determine the VLAN ID for that port, and then determine which of the other ports are also members of that VLAN by matching their assigned VLAN ID values. The packet will then be transmitted to each port with the same VLAN ID as the source port.

6.0 Port Trunking

Port trunking allows the designer to configure the MDS105, such that ports 0 and 1 are defined as a single logical port. This provides a 200 Mbps link to a switch or server utilizing two 100 Mbps ports in parallel.

Ports 0 and 1 can be trunked by pulling the TRUNK_EN pin to the high state. In this mode, the source MAC addresses of all packets received from the trunk are checked against the MCT database to ensure that they have a port ID of 0 or 1. Packets that have a port ID other than 0 and 1 will cause the MDS105 to learn the new MAC address for this port change.

On transmission, the trunk port is determined by hashing the source and destination MAC addresses. This provides a mapping between each MAC address and an associated trunk port. Subsequent packets with the same MAC address will always utilize the same trunk port.

The MDS105 also provides a safe fail-over mode for port trunking. If one of the two ports goes down, as identified by the port's link status signal, then the MDS105 will switch all traffic over to the remaining port in the trunk. Thus, the trunk link is maintained, albeit at a lower effective bandwidth.

7.0 Port Mirroring

Utilizing the four port mirroring control pins provides the ability to enable or disable port mirroring, select which of the remaining 3 ports is to be mirrored, and choose whether the receive or transmit data is being mirrored. The control for this function is shown in the following table.

Mirrored Port	Mirror_Control [3]	Mirror_Control [2]	Mirror_Control [1]	Mirror_Control [0]
Port 0 RX	1	0	0	0
Port 0 TX	0	0	0	0
Port 1 RX	1	0	0	1
Port 1 TX	0	0	0	1
Port 2 RX	1	1	1	0
Port 2 TX	0	1	1	0
Disabled	0/1	1	1	1

Table 2 - Port Mirroring Configuration

When enabled, port mirroring will allow the user to monitor traffic going through the switch on output Port 3. If the port mirroring control pins MIR_CTL[3:0] are left floating, the MDS105 will operate with the port mirroring function disabled.

When port mirroring is enabled, the user must configure Port 3 to operate in the same mode as the port it is mirroring (autonegotiation, duplex, speed, flow control).

8.0 Power Saving Mode in MAC

The MDS105 was designed to be power efficient. When the internal MAC sections detect that the external port is not receiving or transmitting packets, it will shut off and conserve power. When new packet data is loaded into the output transmit FIFO of a MAC in power saving mode, the MAC will return to life and begin operating immediately.

When the MAC is in power saving mode and new packet data is received on the RMII, the MAC will return to life and receive data normally into the receive FIFO. This wakeup occurs when the MAC sees the Carrier Sense Data Valid (CRS_DV) signal asserted.

Using this method, the switch will turn off all MAC sections during periods when there is no network activity (at night, for example), and save power. For large networks this power savings could be large. To achieve the maximum power efficiency, the designer should use a physical layer transceiver that utilizes “Wake-On-LAN” technology.

9.0 EEPROM I^2C Interface

A simple 2 wire serial interface is provided to allow the configuration of the MDS105 from an external EEPROM. The MDS105 utilizes a 1K bit EEPROM with an I^2C interface.

10.0 Management Interface

The MDS105 uses a standard parallel port interface to provide external CPU access to the internal registers. This parallel interface is composed of 3 pins: DATA0, STROBE, and ACK. The DATA0 pin provides the address and data content input to the MDS105, while the ACK pin provides the corresponding output to the external CPU. The STROBE pin is provided as the clock for both serial data streams. Any of the MDS105 internal registers can be modified through this parallel port interface[1].

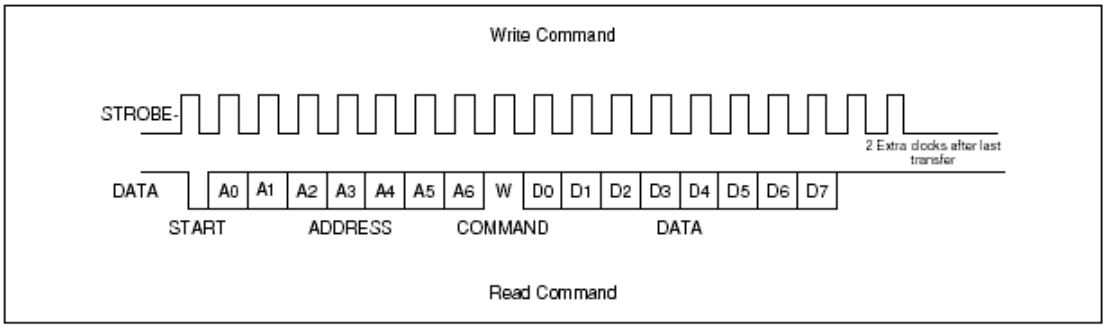


Figure 3 - Write Command

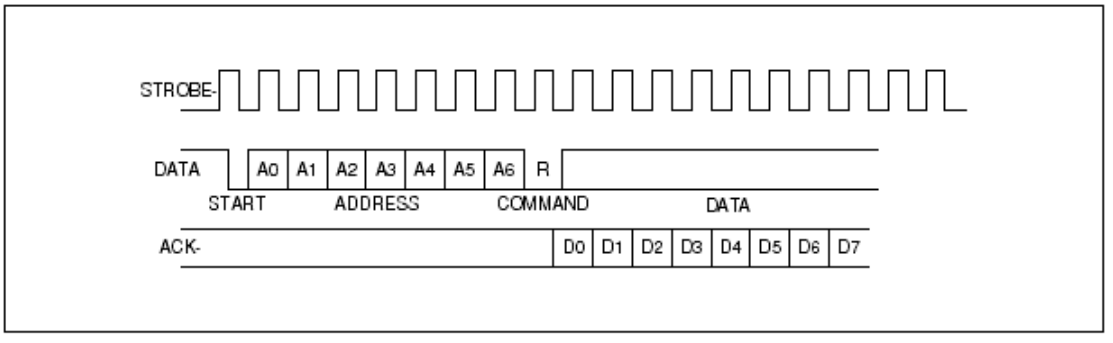


Figure 4 - Read Command

Each management interface transfer consists of four parts:

1. A START pulse – occurs when DATA is sampled high when STROBE is rising followed by DATA being sampled low when STROBE falls.
2. Register address strobed into DATA0 pin, using the high level of the STROBE pin.
3. Either a read or write command (see waveforms above).
4. Data to be written provided on DATA0, or data to be read provided on ACK.

Any command can be aborted in the middle by sending an ABORT pulse to the MDS105. An ABORT pulse occurs when DATA is sampled low and STROBE is rising, followed by DATA being sampled high when STROBE falls.

1. The 3-bit parallel interface is not “parallel” in the usual sense of the word; it is actually a synchronous serial architecture. However, the MDS105 management interface adheres to IEEE 1284 parallel port standards.

11.0 Configuration Register Definitions

The MDS105 registers can be accessed via the parallel interface and/or the I^2C interface. Some registers are only accessible through the parallel interface. The access method for each register is listed in the individual register definitions. Each register is 8 bits wide.

11.1 GCR - Global Control Register

- Access: parallel interface, Write Only
- Address: h30

Bit 0	Save configuration into EEPROM	(Default = 0)
Bit 1	Save configuration into EEPROM and reset system	(Default = 0)
Bit 2	Start Built-In Self-Test (BIST)	(Default = 0)
Bit 3	Reset system	(Default = 0)

11.2 DCR - Device Status and Signature Register

- Access: parallel interface, Read Only
- Address: h31

Bit 0	Busy writing configuration from I^2C
Bit 1	Busy reading configuration from I^2C
Bit 2	Built-In Self-Test (BIST) in progress
Bit 3	RAM error during BIST
Bits [7:6]	Revision number

11.3 DA – DA Register

- Access: parallel interface, Read Only
- Address: h36

Returns 8-bit value DA (hexadecimal) if the parallel port connection is good. Otherwise, returns some other value indicating failure.

11.4 MBCR – Multicast Buffer Control Register

- Access: parallel interface and I^2C, Read/Write
- Address: h00

Bit [7:0]	MAX_CNT_LMT	Maximum number of multicast frames allowed to be buffered inside the device at any one time	(Default = 1F)

11.5 FCBST – FCB Buffer Low Threshold

- Access: parallel interface and I^2C, Read/Write
- Address: h01

Bits [5:0]	BUF_LOW_TH	Buffer Low Threshold – the number of free buffers below which flow control or WRED is triggered	(Default = 1F)
Bit 6		Use IP precedence subfield (TOS[0:2]) for Transmission Priority	(Default = 0)
Bit 7		Use IP precedence subfield (TOS[0:2]) for Drop Level	(Default = 0)
	Note that, for Bits 6 and 7, Default = 0 means to use TOS[3:5].		

11.6 LPBT – Low Drop Precedence Buffer Threshold

- Access: parallel interface and I^2C, Read/Write
- Address: h02

Bits [7:0]	LOW_DROP_CNT	Number of frame buffers reserved for low-drop traffic	(Default 3F)

11.7 FCR – Flooding Control Register

- Access: parallel interface and I^2C, Read/Write
- Address: h03

Bits [3:0]	U2MR	Maximum number of flooded frames allowed within any time interval indicated by TimeBase bits (violations are discarded)	(Default = 8)
Bits [6:4]	TimeBase	000 = 100 μs 001 = 200 μs 010 = 400 μs 011 = 800 μs 100 = 1.6 μs 101 = 3.2 μs 110 = 6.4 μs 111 = 100 μs	(Default = 000)
Bit 7	USE_TOS	Use TOS instead of VLAN priority for IP packet	(Default = 0)

11.8 AVTCL – VLAN TYPE CODE REGISTER LOW

- Access: parallel interface and I^2C, Read/Write
- Address: h04

Bit [7:0]	VLANType_LOW	Lower 8 bits of VLAN type code	(Default = 00)

11.9 AVTCH – VLAN Type Code Register High

- Access: parallel interface and I^2C, Read/Write
- Address: h05

Bit [7:0]	VLANType_HIGH	Upper 8 bits of VLAN type code	(Default 81)

11.10 AVPM – VLAN Priority Map

- Access: parallel interface and I_2 C, Read/Write
- Address: h06

Map VLAN tag into 2 transmit queues (0 = low priority, 1 = high priority)

Bit 0	Mapped priority of tag value 0	(Default 0)
Bit 1	Mapped priority of tag value 1	(Default 0)
Bit 2	Mapped priority of tag value 2	(Default 0)
Bit 3	Mapped priority of tag value 3	(Default 0)
Bit 4	Mapped priority of tag value 4	(Default 0)
Bit 5	Mapped priority of tag value 5	(Default 0)
Bit 6	Mapped priority of tag value 6	(Default 0)
Bit 7	Mapped priority of tag value 7	(Default 0)

11.11 AVDM – VLAN Discard Map

- Access: parallel interface and I^2C, Read/Write
- Address: h07

Map VLAN tag into frame discard levels (0 = low drop, 1 = high drop).

Bit 0	Frame discard for tag value 0	(Default 0)
Bit 1	Frame discard for tag value 1	(Default 0)
Bit 2	Frame discard for tag value 2	(Default 0)
Bit 3	Frame discard for tag value 3	(Default 0)
Bit 4	Frame discard for tag value 4	(Default 0)
Bit 5	Frame discard for tag value 5	(Default 0)
Bit 6	Frame discard for tag value 6	(Default 0)
Bit 7	Frame discard for tag value 7	(Default 0)

11.12 TOSPM – TOS Priority Map

- Access: parallel interface and I^2C, Read/Write
- Address: h08

Map TOS field in IP packet into 2 transmit queues (0 = low priority, 1 = high priority).

Bit 0	Mapped priority when TOS is 0	(Default 0)
Bit 1	Mapped priority when TOS is 1[1]	(Default 0)
Bit 2	Mapped priority when TOS is 2	(Default 0)
Bit 3	Mapped priority when TOS is 3	(Default 0)
Bit 4	Mapped priority when TOS is 4	(Default 0)
Bit 5	Mapped priority when TOS is 5	(Default 0)
Bit 6	Mapped priority when TOS is 6	(Default 0)
Bit 7	Mapped priority when TOS is 7	(Default 0)

1. TOS = 1 means the appropriate 3-bit TOS subfield is “001.

11.13 PTPRI – Port Priority

- Access: parallel interface and I^2C, Read/Write
- Address: h09

Enable and configure port-based priorities for ports 0, and 1

Bit 0	EN0	Port 0: Enable; 1 = enabled	(Default 0)
Bit 1	P0	Port 0: Priority; 1 = high, 0 = low	(Default 0)
Bit 2	EN1	Port 1: Enable; 1 = enabled	(Default 0)
Bit 3	P0	Port 1: Priority; 1 = high, 0 = low	(Default 0)
Bit 7:4	Reserved		

11.14 TOSDM – TOS Discard Map

- Access: parallel interface and I^2C, Read/Write
- Address: h0A

Map TOS into frame discard levels (0 = low drop, 1 = high drop).

Bit 0	Frame discard when TOS is 0	(Default 0)
Bit 1	Frame discard when TOS is 1	(Default 0)
Bit 2	Frame discard when TOS is 2	(Default 0)
Bit 3	Frame discard when TOS is 3	(Default 0)
Bit 4	Frame discard when TOS is 4	(Default 0)
Bit 5	Frame discard when TOS is 5	(Default 0)
Bit 6	Frame discard when TOS is 6	(Default 0)
Bit 7	Frame discard when TOS is 7	(Default 0)

11.15 AXSC – Transmission Scheduling Control Register

- Access: parallel interface and I^2C, Read/Write
- Address: h0B

Bits [3:0]	Transmission Queue Service Weight for high priority queue	(Default F)
Bit [5]	Global Quality of Service Enable	(Default 0)
Bit [6]	Global Flow Control Disable – if 1, flow control is disabled globally; if 0, each port's flow control settings are separately configurable	(Default 0)
Bit [7]	Half Duplex Priority Enable – if 0, priority is disabled for all half duplex ports; if 1, priority is enabled unless AXSC[5] = 0	(Default 0)

11.16 MII_OP0 – MII Register Option 0

- Access by parallel interface and I^2C, Read/Write
- Address: h0C

Permits a non-standard address for the Phy Status Register. When low and high Address bytes are 0, the MDS108 will use the standard address.

Bit [7:0]	Low order address byte	(Default 00)

11.17 MII_OP1 – MII Register Option 1

- Access: parallel interface and I^2C, Read/Write
- Address: h0D

Bit [7:0]	High order address byte	(Default 00)

11.18 AGETIME_LOW – MAC Address Aging Timer Low

- Access: parallel interface and I^2C, Read/Write
- Address: h0E

Bit [7:0]	Low byte of the MAC address aging timer	(Default 25)

11.19 AGETIME_HIGH – MAC Address Aging Timer High

- Access: parallel interface and I^2C, Read/Write
- Address: h0F

Bit [7:0]	High byte of the MAC address aging timer.	(Default 01)
	The aging time is based on the following formula: {AGETIME_HIGH, AGETIME_LOW} x 1024 ms	The default setting provides a 300 second aging time.

11.20 ECR1P0 – Port 0 Control Register

- Access: parallel interface and I^2C, Read/Write
- Address: h10

Bits [3:0]	Port Mode		(Default 0000)
Bit [3]		1 – Force configuration based on Bits [2:0] 0 – Autonegotiate and advertise based on Bits [2:0]	
Bit [2]		1 – 10 Mbps 0 – 100 Mbps	
Bit [1]		1 – Half Duplex 0 – Full Duplex	
Bit [0]		1 – Flow Control Off 0 – Flow Control On	
Bits [6:4]	PVID	Port-based VLAN ID	(Default 000)
Bit [7]	Reserved		

11.21 ECR1P1 – Port 1 Control Register

- Access: parallel interface and I^2C, Read/Write
- Address: h11

Bits [3:0]	Port Mode		(Default 0000)
Bit [3]		1 – Force configuration based on Bits [2:0] 0 – Autonegotiate and advertise based on Bits [2:0]	
Bit [2]		1 – 10 Mbps 0 – 100 Mbps	
Bit [1]		1 – Half Duplex 0 – Full Duplex	
Bit [0]		1 – Flow Control Off 0 – Flow Control On	
Bits [6:4]	PVID	Port-based VLAN ID	(Default 000)
Bit [7]	Reserved		

11.22 ECR1P2 – Port 2 Control Register

- Access: parallel interface and I^2C, Read/Write
- Address: h16

Bits [3:0]	Port Mode		(Default 0000)
Bit [3]		1 – Force configuration based on Bits [2:0] 0 – Autonegotiate and advertise based on Bits [2:0]	
Bit [2]		1 – 10 Mbps 0 – 100 Mbps	
Bit [1]		1 – Half Duplex 0 – Full Duplex	
Bit [0]		1 – Flow Control Off 0 – Flow Control On	
Bits [6:4]	PVID	Port-based VLAN ID	(Default 000)
Bit [7]	Reserved		

11.23 ECR1P3 – Port 3 Control Register

- Access: parallel interface and I^2C, Read/Write
- Address: h17

Bits [3:0]	Port Mode		(Default 0000)
Bit [3]		1 – Force configuration based on Bits [2:0] 0 – Autonegotiate and advertise based on Bits [2:0]	
Bit [2]		1 – 10 Mbps 0 – 100 Mbps	
Bit [1]		1 – Half Duplex 0 – Full Duplex	
Bit [0]		1 – Flow Control Off 0 – Flow Control On	
Bits [6:4]	PVID	Port-based VLAN ID	(Default 000)
Bit [7]	Reserved		

11.24 ECR1P4 – Port 4 Control Register

- Access: parallel interface and I^2C, Read/Write
- Address: h18

Bits [3:0]	Port Mode		(Default 0000)
Bit [3]		1 – Force configuration based on Bits [2:0] 0 – Autonegotiate and advertise based on Bits [2:0]	
Bit [2]		1 – 10 Mbps 0 – 100 Mbps	
Bit [1]		1 – Half Duplex 0 – Full Duplex	
Bit [0]		1 – Flow Control Off 0 – Flow Control On	
Bits [6:4]	PVID	Port-based VLAN ID	(Default 000)
Bit [7]	Reserved		

11.25 FC_0 – Flow Control Byte 0

- Access: parallel interface and I^2C, Read/Write
- Address: h19

The flow control hold time parameter is the length of time a flow control message is effectual (i.e. halts incoming traffic) after being received. The hold time is measured in units of “slots,” the time it takes to transmit 64 bytes at wire speed. The default setting is 32 slots, or for a 100 Mbps port, approximately 164 ms.

Bits [7:0]	Flow control hold time byte 0	(Default 20)

11.26 FC_1 – Flow Control Byte 1

- Access: parallel interface and I^2C, Read/Write
- Address: h1A

Bits [7:0]	Flow control hold time byte 1	(Default 00)

11.27 FC_2 – Flow Control CRC Byte 0

- Access: parallel interface and I^2C, Read/Write
- Address: h1B

Bits [7:0]	Flow control frame CRC byte 0	(Default E5)

11.28 FC_3 – Flow Control CRC Byte 1

- Access: parallel interface and I^2C, Read/Write
- Address: h1C

Bits [7:0]	Flow control frame CRC byte 1	(Default DE)

11.29 FC_4 – Flow Control CRC Byte 2

- Access: parallel interface and I^2C, Read/Write
- Address: h1D

Bits [7:0]	Flow control frame CRC byte 2	(Default 3F)

11.30 FC_5 – Flow Control CRC Byte 3

- Access: parallel interface and I^2C, Read/Write
- Address: h1E

Bits [7:0]	Flow control frame CRC byte 3	(Default 76)

11.31 CHECKSUM - EEPROM Checksum

- Access: parallel interface and I^2C, Read/Write
- Address: h24

The calculation is 0x100 - ((sum of registers 0x00~0x23) & 0xff)

Bits [7:0]	Checksum	(Default 2D)

12.0 MDS105 Pin Descriptions

Note: # Active low signal
I Input signal
S Input signal with Schmitt-Trigger
O Output signal
OD Open-Drain driver
I/O Input & Output signal
SL Slew Rate Controlled
D Pulldown
U Pullup
5 5V Tolerance

Pin No(s).	Symbol	Type	Name & Functions
Frame Buffer Memory Interface			
201, 200, 199, 197, 196, 195, 193, 192, 191, 190, 188, 187, 186, 185, 183, 182, 181, 179, 178, 177, 176, 174, 173, 172, 170, 169, 168, 167, 165, 164, 163, 161	L_D[31:0]	I/O, U, SL	Databus to Frame Buffer Memory
203, 151, 158, 160, 10, 9, 8, 6, 5, 4, 2, 1, 208, 206, 205, 204, 150	L_A[18:2]	I/O, U, SL	Address pins for buffer memory
153	L_CLK	O	Frame Buffer Memory Clock
155	L_WE#	O, SL	Frame Buffer Memory Write Enable
156	L_OE#	O	Frame Buffer Memory Output Enable
157	L_ADSC#	O, SL	Frame Buffer Memory Address Status Control
MII Management Interface			
120	M_MDC	O	MII Management Data Clock
122	M_MDIO	I/O, U	MII Management Data I/O
I^2C Interface (Serial EEPROM Interface)			
123	SCL	O, U, 5	I^2C Data Clock
124	SDA	I/O, U, OD, 5	I^2C Data I/O
Parallel Port Management Interface			
127	STROBE	I, U, S, 5	Strobe Pin
128	DATA0	I, U, 5	Data Pin
129	ACK	O, U, OD, 5	Acknowledge Pin
Port 0 RMII Interface			
24, 23	M0_RXD[1:0]	I, U	Port 0 Receive Data
22	M0_CRS_DV	I, D	Port 0 Carrier Sense and Data Valid
21, 20	M0_TXD[1:0]	O	Port 0 Transmit Data
19	M0_TXEN	O	Port 0 Transmit Enable
Port 1 RMII Interface			
31, 30	M1_RXD[1:0]	I, U	Port 1 Receive Data

Pin No(s).	Symbol	Type	Name & Functions
29	M1_CRS_DV	I, D	Port 1 Carrier Sense and Data Valid
28, 27	M1_TXD[1:0]	O	Port 1 Transmit Data
26	M1_TXEN	O	Port 1 Transmit Enable
Port 2 RMII Interface			
79, 78	M2_RXD[1:0]	I, U	Port 2 Receive Data
77	M2_CRS_DV	I, D	Port 2 Carrier Sense and Data Valid
76, 75	M2_TXD[1:0]	O	Port 2 Transmit Data
74	M2_TXEN	O	Port 2 Transmit Enable
Port 3 RMII Interface			
86, 85	M3_RXD[1:0]	I, U	Port 3 Receive Data
84	M3_CRS_DV	I, D	Port 3 Carrier Sense and Data Valid
83, 82	M3_TXD[1:0]	O	Port 3 Transmit Data
81	M3_TXEN	O	Port 3 Transmit Enable
Port 4 RMII Interface			
105, 104, 103, 102	M4_RXD[3:0]	I, U	Port 4 Receive Data
113, 112, 111, 110	M4_TXD[3;0]	O	Port 4 Transmit Data
109	M4_TXEN	O	Port 4 Transmit Enable
97	M4_RXDV	I, D	Port 4 Receive Data Valid
100	M4_RXCLK	I, U	Port 4 Receive Clock
107	M4_TXCLK	I/O, U	Port 4 Transmit Clock
114	M4_LINK	I, U	Port 4 Link Status
116	M4_SPEED	I/O, U	Port 4 Speed Select (100Mb = 1)
115	M4_DUPLEX	I, U	Port 4 Full-Duplex Select (half-duplex = 0)
98	M4_COL	I, U	Port 4 Collision Detect
Port 4 Serial Interface			
102	S4_RXD	I, U	Port 4 Serial Receive Data
100	S4_RXCLK	I, U	Port 4 Serial Receive Clock
97	S4_CRS_DV	I, D	Port 4 Serial Carrier Sense and Data Valid
110	S4_TXD	O	Port 4 Serial Transmit Data
107	S4_TXCLK	I	Port 4 Serial Transmit Clock
109	S4_TXEN	O	Port 4 Serial Transmit Enable
98	S4_COL	I, U	Port 4 Serial Collision Detect
114	S4_LINK	I, U	Port 4 Link Status
115	S4_DUPLEX	I, U	Port 4 Full-Duplex Select (half-duplex = 0)
Miscellaneous Control Pins			
95	M_CLK	I	Reference RMII Clock
118	M4_REFCLK	O, U	Port 4 Reference Clock (M_CLK/2)
148	SCLK	I	System Clock (25 - 50 Mhz)
125	TEST#	I, U	No Connect

Pin No(s).	Symbol	Type	Name & Functions
126	TRUNK_EN	I, D	Port Trunking Enable
146, 145, 144, 143	MIR_CTL[3:0]	I/O, U	Port Mirroring Control
142	RESIN_	I, S	Reset Pin
141	RESETOUT_	O	PHY Reset Pin
Test Pins			
139	TMODE	I/O, U	Puts MDS105 into test mode for ATE test
138, 137, 136, 135	TSTOUT[7:4]	O	Test Outputs
134, 133, 132, 131	TSTOUT[3:0]	I/O, U	Test Outputs
NC Pins			
12, 13, 14, 15, 16, 17, 33, 34, 35, 36, 37, 38, 40, 41, 42, 43, 44, 45, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 60, 61, 62, 63, 64, 65, 67, 68, 69, 70, 71, 72, 88, 89, 90, 91, 92, 93	N/C Reserved		No Connect
Power Pins			
3, 39, 73, 96, 130, 159, 184	VDD (Core)	Input	+3.3 Volt DC Supply for Core Logic (7 pins)
11, 25, 59, 87, 101, 108, 119, 147, 152, 166, 175, 194, 202	VDD	Input	+3.3 Volt DC Supply for I/O Pads (13 pins)
18, 46, 80, 106, 140, 171, 198	VSS (Core)	Input	Ground for Core Logic (7 pins)
7, 32, 66, 94, 99, 117, 121, 149, 154, 162, 180, 189, 207	VSS	Input	Ground for I/O Pads (13 pins)

12.1 Strap Options

The Strap options are relevant during the initial power-on period, when reset is asserted. During reset, the MDS105 will examine the boot strap address pin to determine its value and modify the internal configuration of the chip accordingly.

"1" means Pull-up

"0" means Pull-down with an external 1K Ohm

Default value is 1, (all boot strap pins have internal pull up resistor).

Pin No(s)	Symbol	Name & Functions
Boot Strap Pins		
206 (L_A[5])	Memory Size	1 - Memory size = 256 KB, 0 - Memory size = 512KB
208 (L_A [6])	EEPROM	1 - NO EEPROM Installed 0 - EEPROM Installed[1]
151 (L_A[17])	Port 4 MII/Serial	1 - MII Mode for port 4 0 - Serial mode for port 4
150 (L_A[2])	Link Polarity	Link Polarity for serial interface 1 - Active Low 0 - Active High
204 (L_A[3])	FDX Polarity	Full/Half Duplex Polarity for serial interface 1 - Active Low 0 - Active High
205 (L_A[4])	SPD100 Polarity	Speed polarity for serial interface 1 - Active Low 0 - Active High
133 (TST[2])	SRAM Self Test	For Board/System Manufacturing Test[2] 1 - Disable 0 - Enable

1. If the MDS105 is configured from EEPROM preset (L_A[6] pulled down at reset), it will try to load its configuration from the EEPROM. If the EEPROM is blank or not preset, it will not boot up. The parallel port can be used to program the EEPROM at any time.

2. During normal power-up the MDS105 will run through an external SSRAM memory test to ensure that there are no memory interface problems. If a problem is detected, the chip will stop functioning. To facilitate board debug in the event that a system stops functioning, the MSD105 can be put into a continuous SSRAM self test mode to allow an operator to determine if there are stuck pins in the memory interface (using network analyzer).

13.0 Characteristics and Timing

13.1 Absolute Maximum Rating

Storage Temperature	-65C to +150C
Operating Temperature	-40C to +85C
Supply Voltage VDD with Respect to VSS	+3.0 V to +3.6 V
Voltage on 5V Tolerant Input Pins	-0.5 V to (VDD +3.3V)
Voltage on Other Pins	-0.5V to (VDD +0.3V)

Caution: Stresses above those listed may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the absolute Maximum Ratings for extended Ratings for extended periods may affect device reliability.

13.2 DC Electrical Characteristics

VDD = 3.0V to 3.6V (3.3v +/- 10%) TAMBIENT = -40C to +85C

Symbol	Parameter Description	Min	Typ.	Max	Unit
f_{OSC}	Frequency of Operation	50	66	80	MHz
I_{DD}	Supply Current - @ 80 MHz (VDD = 3.3V)			TBD	mA
V_{OH}	Output High Voltage (CMOS)	VDD - 0.5			V
V_{OL}	Output Low Voltage (CMOS)			0.5	V
V_{IH_TTL}	Input High Voltage (TTL 5V tolerant)	VDD x 70%		VDD + 2.0	V
V_{IL_TTL}	Input Low Voltage (TTL 5V tolerant)			VDD x 30%	V
I_{IH_5VT}	Input Leakage Current (0.1 V < V_{IN} < VDD) (all pins except those with internal pull-up/ pull-down resistors)			10	µA
I_{IL_5VT}	Output Leakage Current (0.1 V < V_{OUT} < VDD)			10	µA
C_{IN}	Input Capacitance			5	pF
C_{OUT}	Output Capacitance			5	pF
$C_{I/O}$	I/O Capacitance			7	pF

13.3 Clock Frequency Specifications

Symbol	Parameter	(Hz)	Note:
C1	SCLK - Core System Clock Input	50M	
C2	M_CLK - RMII Port Clock	50M	
C3	M4_REFCLK - MII Reference Clock	25M	
C4	L_CLK - Frame Buffer Memory Clock	55M	L_CLK = SCLK
C5	M_MDC - MII Management Data Clock	1.56M	M_MDC = SCLK/32
C6	SCL - I^2C Data Clock	50K	SCL = M_CLK/1000

Suggestion Clock rate for various configurations:

		Input		Output		
Configuration		SCLK	M_CLK (RMII)	L_CLK	M_MDC	SCL
Port 0-3	Port 4					
10M RMII	10/100M MII	50M	50M	=SCLK	=SCLK/32	50K
100M RMII	Not Used	55M	50M	=SCLK	=SCLK/32	50K
100M RMII	10/100M MII	60M	50M	=SCLK	=SCLK/32	50K

14.0 AC Timing Characteristics

14.1 Frame Buffer Memory Interface:

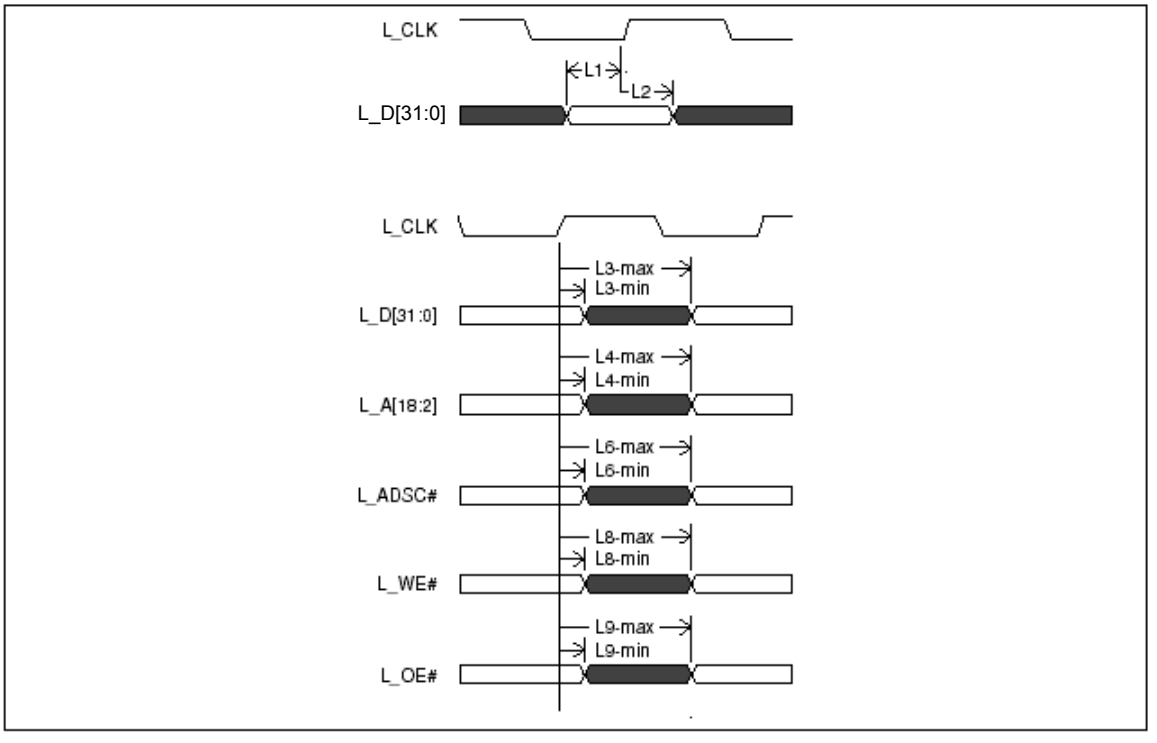


Figure 5 - Frame Buffer Memory Interface Timing

Symbol	Parameter	50MHz		Note
		Min (ns)	Max (ns)	
L1	L_D[31:0] input setup time	5		
L2	L_D[31:0] input hold time	0		
L3	L_D[31:0] output valid delay	1	8	C_L = 30pF
L4	L_A[18:2] output valid delay	1	8	C_L = 50pF
L6	L_ADSC# output valid delay	1	8	C_L = 50pF
L8	L_WE# output valid delay	1	8	C_L = 30pF
L9	L_OE# output valid delay	1	8	C_L = 30pF

Table 3 - Frame Buffer Memory Interface Timing

14.2 RMII Timing Requirements

Symbol	Parameter	50MHz		Note
		Min (ns)	Max (ns)	
M1	M_CLK			Reference Input Clock
M2	M[3:0]_RXD[1:0] input setup time	4		
M3	M[3:0]_RXD[1:0] input hold time	1		
M4	M[3:0]_CRS_DV input setup time	4		
M5	M[3:0]_TXEN output delay time	1	11	C_L = 30pF
M6	M[3:0]_TXD[1:0] output delay time	1	11	C_L = 30pF
M7	M[3:0]_LINK input setup time	4		

Table 4 - RMII Timing Requirements

14.3 MII Timing Requirements

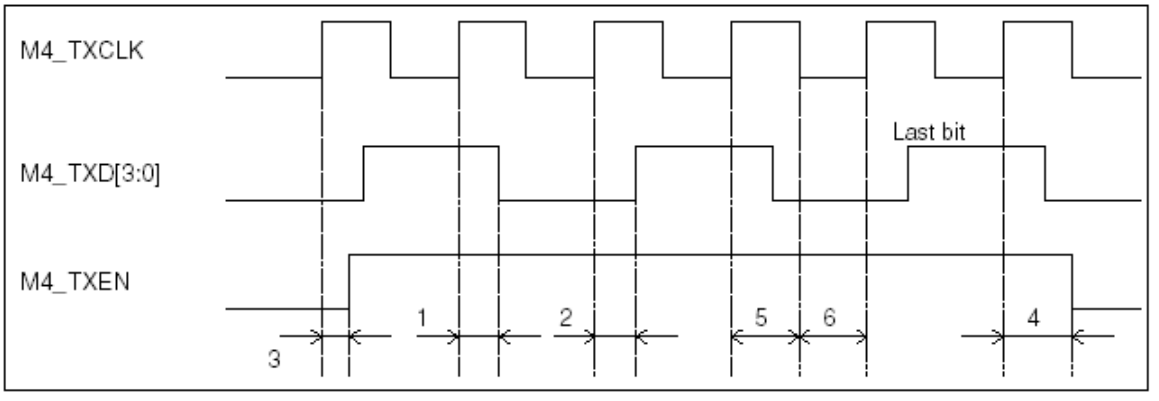


Figure 6 - Transmit Timing

Symbol	Parameter	Time		Unit
		Min	Max	
1	M4_TXCLK rise to M4_TXD[3:0] inactive delay	5	20	ns
2	M4_TXCLK rise to M4_TXD[3:0] active delay	5	20	ns
3	M4_TXCLK rise to M4_TXEN active delay	5	20	ns
4	M4_TXCLK rise of last M4_TXD bit to M4_TXEN inactive delay	5	20	ns
5	M4_TXCLK High wide	25	Inf.	ns
6	M4_TXCLK Low wide	25	Inf.	ns
	M4_TXCLK input rise time require		5	ns
	M4_TXCLK input fall time require		5	ns

*Inf. - infinite

Table 5 - Transmit Timing Requirements

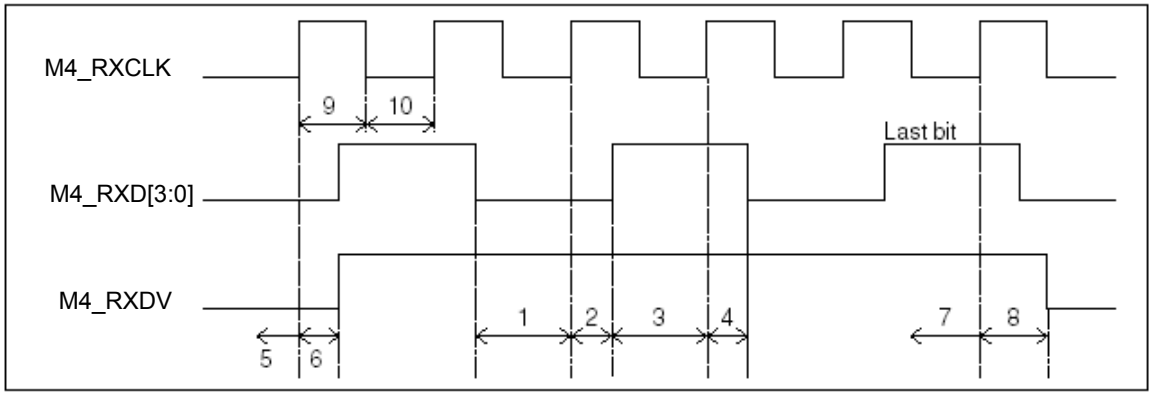


Figure 7 - Receive Timing

Symbol	Parameter	Time		Unit
		Min	Max	
1	M4_RXD[3:0] Low input setup time	10		ns
2	M4_RXD[3:0] Low input hold time		5	ns
3	M4_RXD[3:0] High input setup time	10		ns
4	M4_RXD[3:0] High input hold time		5	ns
5	M4_RXDV Low input setup time	10		ns
6	M4_RXDV Low input hold time		5	ns
7	M4_RXDV High input setup time	10		ns
8	M4_RXDV High input hold time		5	ns
9	M4_RXCLK High wide	25	Inf.	ns
10	M4_RXCLK Low wide	25	Inf.	ns
	M4_RXCLK input rise time require		5	ns
	M4_RXCLK input fall time require		5	ns

*Inf. - infinite

Table 6 - Receive Timing Requirements

14.4 Port 4 Serial Mode AC Timing

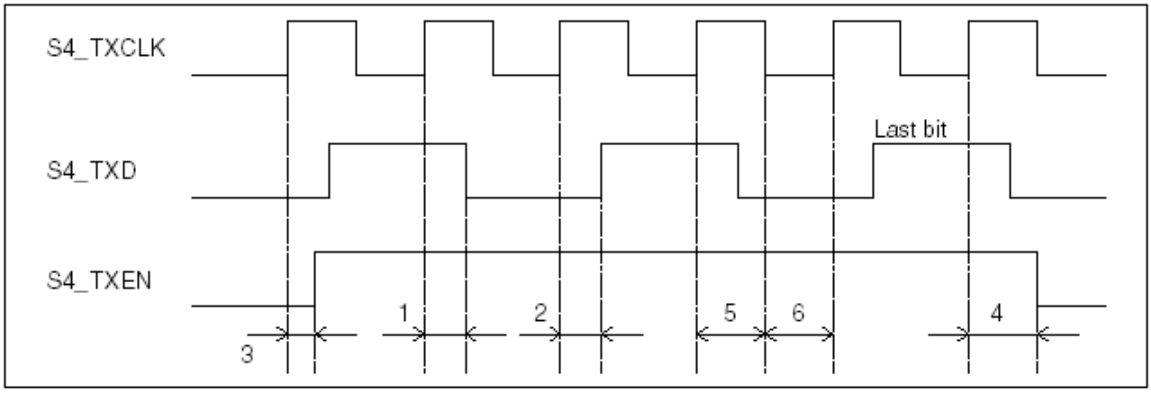


Figure 8 - Transmit Timing

Symbol	Parameter	Time		Unit
		Min	Max	
1	S4_TXCLK rise to S4_TXD inactive delay	5	20	ns
2	S4_TXCLK rise to S4_TXD active delay	5	20	ns
3	S4_TXCLK rise to S4_TXEN active delay	5	20	ns
4	S4_TXCLK rise of Last S4_TXD bit to S4_TXEN inactive delay	5	20	ns
5	S4_TXCLK High wide	25	Inf.	ns
6	S4_TXCLK Low wide	25	Inf.	ns
	S4_TXCLK input rise time require		5	ns
	S4_TXCLK input fall time require		5	ns

*Inf. - infinite

Table 7 - Transmit Timing Requirements

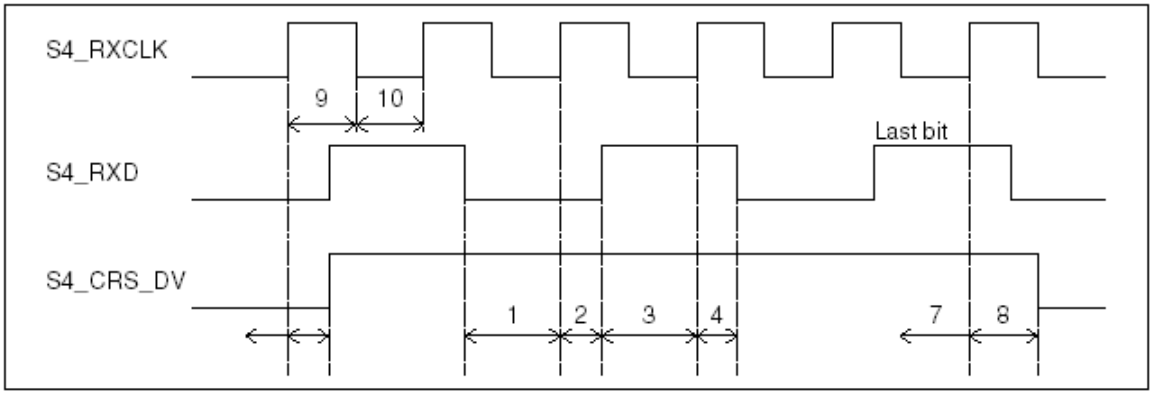
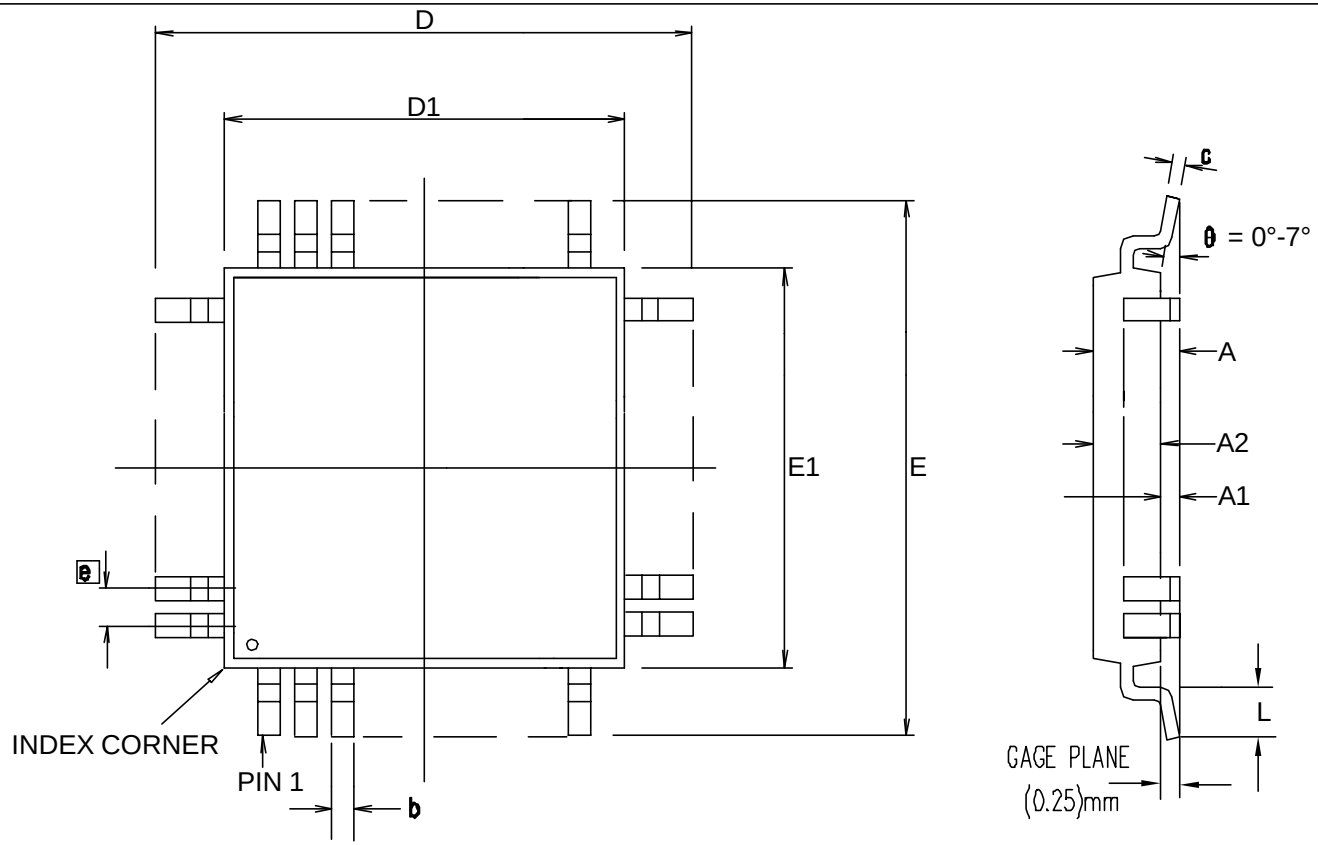


Figure 9 - Receive Timing

Symbol	Parameter	Time		Unit
		Min	Max	
1	S4_RXD Low input setup time	10		ns
2	S4_RXD Low input hold time		5	ns
3	S4_RXD High input setup time	10		ns
4	S4_RXD High input hold time		5	ns
5	S4_CRS_DV Low input setup time	10		ns
6	S4_CRS_DV Low input hold time		5	ns
7	S4_CRS_DV High input setup time	10		ns
8	S4_CRS_DV High input hold time		5	ns
9	S4_RXCLK Hi wide	25	Inf.	ns
10	S4_RXCLK Low wide	25	Inf.	ns
	S4_RXCLK input rise time require		5	ns
	S4_RXCLK input fall time require		5	ns

*Inf. - infinite

Table 8 - Receive Timing Requirements



Symbol	Control Dimensions in millimetres		
	MIN	Nominal	MAX
A	–	–	4.10
A1	0.25	–	–
A2	3.20	3.32	3.60
D	30.60 BSC		
D1	28.00 BSC		
E	30.60 BSC		
E1	28.00 BSC		
L	0.45	0.60	0.75
e	0.50 BSC		
b	0.17	0.20	0.27
c	0.09	0.15	0.20
θ	0°	–	7°
ccc	–	0.08	–
N	208		
ND	52		
NE	52		

Conforms to JEDEC MO-143

Notes:

1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.

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ZARLINK SEMICONDUCTOR

Previous package codes: GP / L

Package Code QB

Package Outline for 208 Lead MQFP (28x28x3.32mm) + 2.6 mm (footprint)

GPD00828



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