

PESD4V0Z1BCSF

Extremely low capacitance bidirectional ESD protection diode

29 March 2019

Product data sheet

1. General description

Extremely low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode, part of the TrEOS protection family . The device is housed in a DSN0603-2 (SOD962-2) leadless ultra small Surface-Mounted Device (SMD) package designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- · Bidirectional ESD protection of one line
- Extremely low diode capacitance C_d = 0.45 pF
- Extremely low clamping to protect sensitive I/Os
- · Extremely low-inductance protection path to ground
- ESD protection up to ± 30 kV according to IEC 61000-4-2
- Surge robustness I_{PPM} = 15 A according to IEC 61000-4-5
- Ultra small SMD package

3. Applications

- · Cellular handsets and accessories
- · Portable electronics
- · Communication systems
- · Computers and peripherals

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{RWM}	reverse standoff voltage		-	-	4	V
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C	-	0.45	0.6	pF



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)		K1 [5] K2
2	K2	cathode (diode 2)		sym045
			Transparent top view	
			DSN0603-2 (SOD962-2)	

6. Ordering information

Table 3. Ordering information

Type number Package					
	Name	Description	Version		
PESD4V0Z1BCSF		silicon, leadless ultra small package; 2 terminals; 0.4 mm pitch; 0.6 mm x 0.3 mm x 0.3 mm body	SOD962-2		

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD4V0Z1BCSF	C4

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{RWM}	reverse standoff voltage			-	4	V
I _{PPM}	rated peak pulse current	t _p = 8/20 μs	[1] [2]	-	15	Α
T _{amb}	ambient temperature			-40	125	°C
T _{stg}	storage temperature			-65	150	°C
ESD maximum	ratings					
V _{ESD}	electrostatic discharge	IEC 61000-4-2; contact discharge	[3]	-30	30	kV
	voltage	IEC 61000-4-2; air discharge	[3]	-30	30	kV

- [1] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
- [2] In positive and negative direction.
- [3] Device stressed with ten non-repetitive ESD pulses.

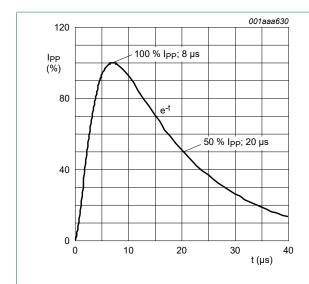


Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5 and IEC 61643-321

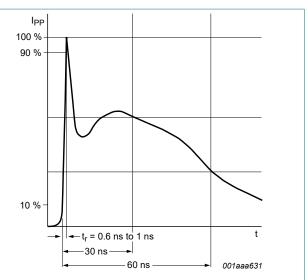


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

 t_{amb} = 25°C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{BR}	breakdown voltage	I _R = 1 mA		-	6.8	-	V
I _{RM}	reverse leakage current	V _{RWM} = 4 V; T _{amb} = 25 °C	[1]	-	1	50	nA
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C		-	0.45	0.6	pF
		f = 1 MHz; V _R = 1.5 V		-	0.4	-	pF
V_{CL}	clamping voltage	I _{PPM} = 4 A	[2]	-	3.1	-	V
		I _{PPM} = 15 A	[2]	-	4.8	-	V
R _{dyn}	dynamic resistance	I _R = 10 A	[3]	-	0.11	-	Ω
		I _R = -10 A	[3]	-	0.11	-	Ω
f _{-3dB}	-3 dB cut-off frequency	normalized to attenuation at 1 MHz		-	14.3	-	GHz

- [1] Guaranteed by design.
- [2] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
- [3] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.

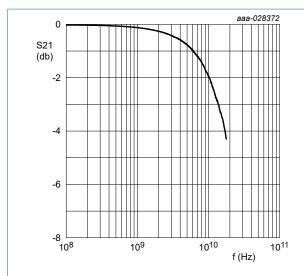


Fig. 3. Insertion loss; typical values

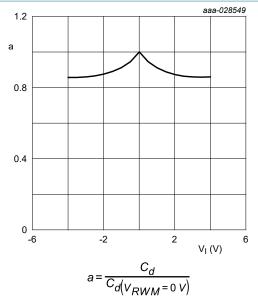


Fig. 4. Relative capacitance as a function of input voltage; typical values

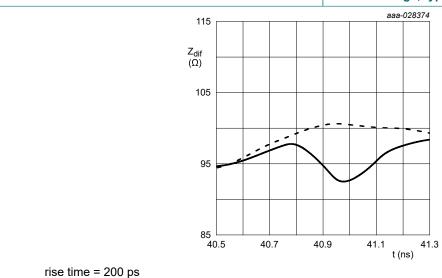
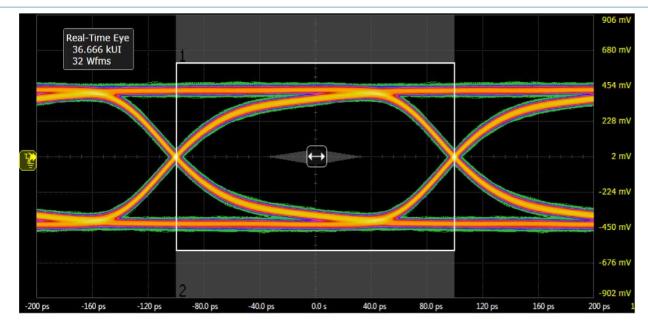


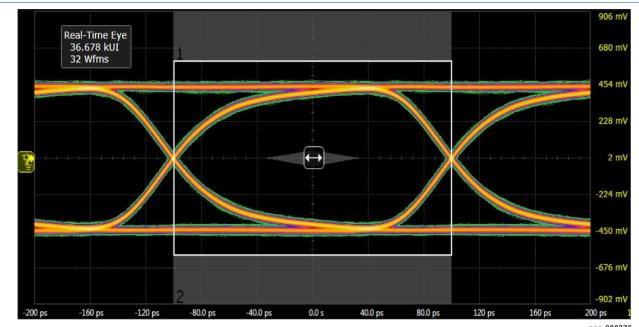
Fig. 5. Differential Time Domain Reflectometer (TDR) plot; typical values



aaa-028375

Data rate: 5 Gbit/s

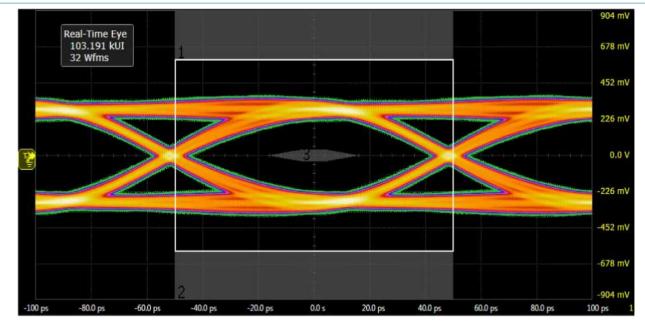
Fig. 6. USB 3.1 eye diagram, PCB with device; typical values



aaa-028376

Data rate: 5 Gbit/s

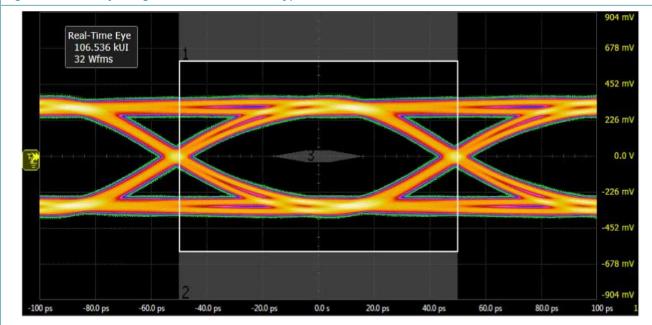
Fig. 7. USB 3.1 eye diagram, PCB without device; typical values



aaa-028377

Data rate: 10 Gbit/s

Fig. 8. USB 3.1 eye diagram, PCB with device; typical values



aaa-028378

Data rate: 10 Gbit/s

Fig. 9. USB 3.1 eye diagram, PCB without device; typical values

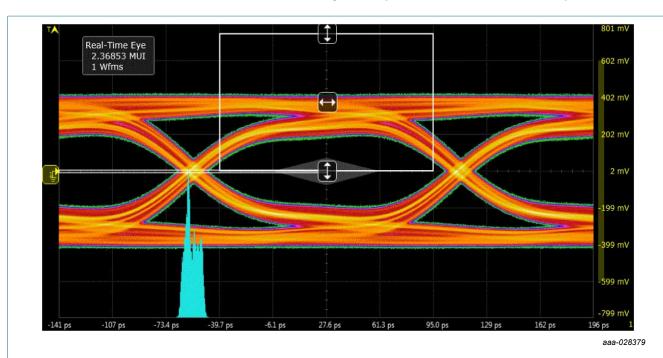


Fig. 10. HDMI2.0 TP1 eye diagram, PCB with device; typical values

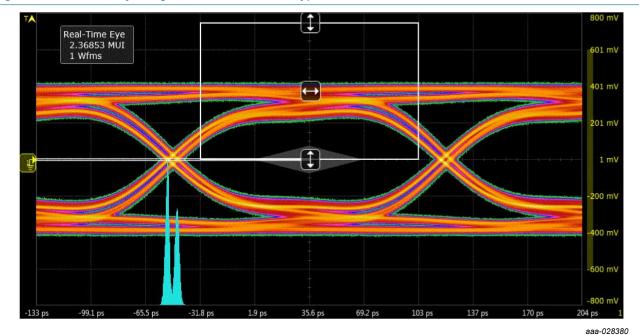


Fig. 11. HDMI2.0 TP1 eye diagram, PCB without device; typical values

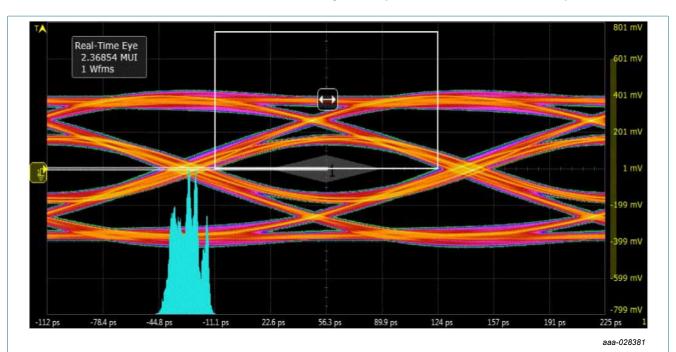


Fig. 12. HDMI2.0 TP2 eye diagram, PCB with device; typical values

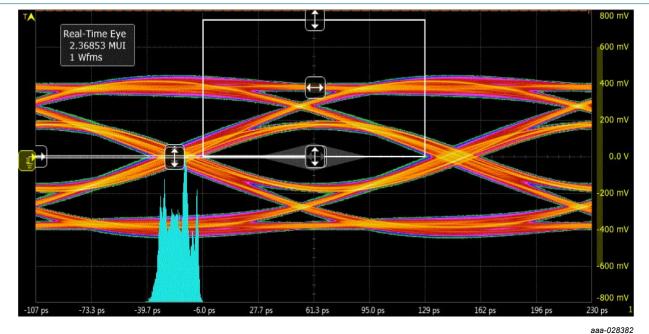


Fig. 13. HDMI2.0 TP2 eye diagram, PCB without device; typical values

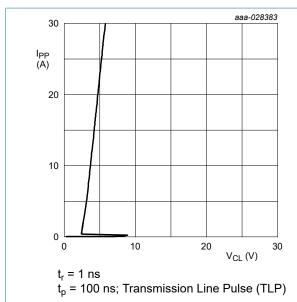


Fig. 14. Dynamic resistance with positive clamping; typical values

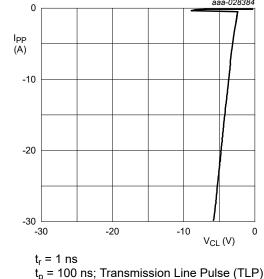


Fig. 15. Dynamic resistance with negative clamping;

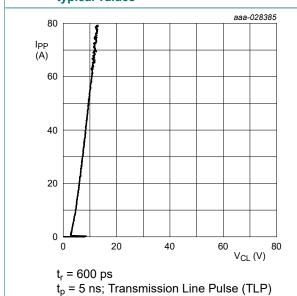
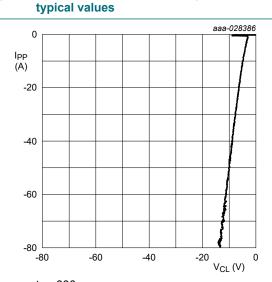


Fig. 16. Dynamic resistance with positive clamping; typical values



 $t_{\rm r}$ = 600 ps $t_{\rm p}$ = 5 ns; Transmission Line Pulse (TLP)

Fig. 17. Dynamic resistance with negative clamping; typical values

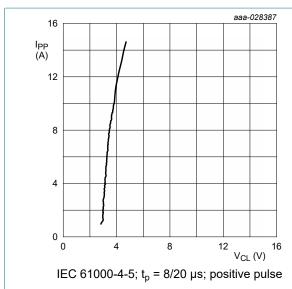
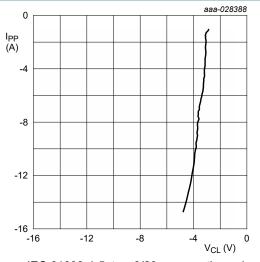
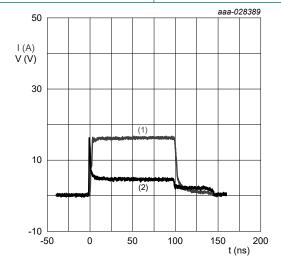


Fig. 18. Dynamic resistance with positive clamping; typical values



IEC 61000-4-5; t_p = 8/20 μ s; negative pulse

Fig. 19. Dynamic resistance with negative clamping; typical values



 $t_r = 1 \text{ ns}$

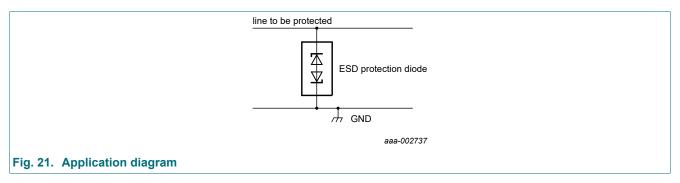
- (1) TLP current
- (2) TLP voltage

Fig. 20. TLP voltage and current over time, typical values

10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

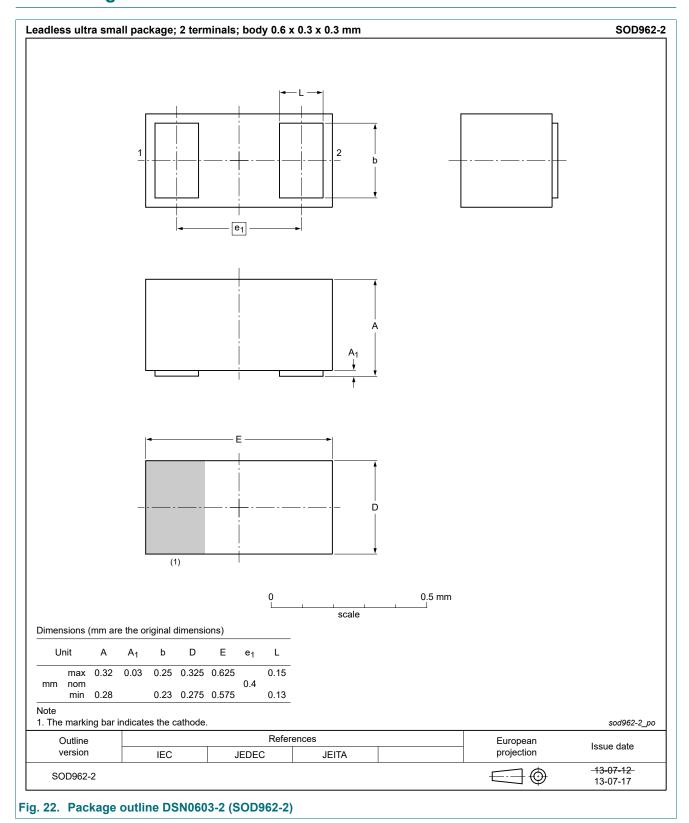


Circuit board layout and protection device placement

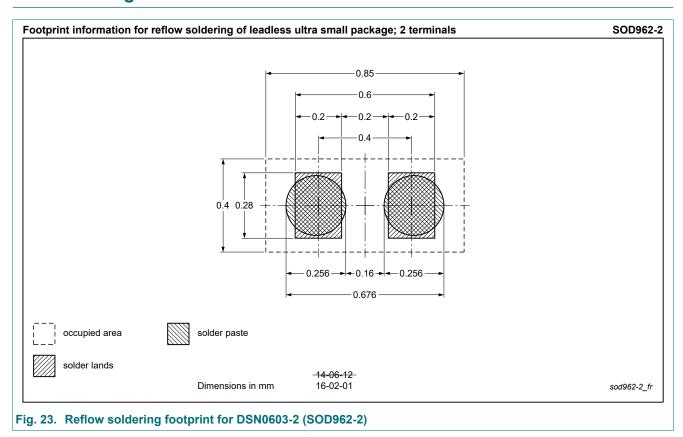
Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

- 1. Place the device as close to the input terminal or connector as possible.
- 2. Minimize the path length between the device and the protected line.
- 3. Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- **6.** Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline



12. Soldering



13. Revision history

Table 7. Revision history

Table 11 Novicion motory						
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes		
PESD4V0Z1BCSF v.2	20190329	Product data sheet	-	PESD4V0Z1BCSF v.1		
Modifications:	Updated Package	ge				
PESD4V0Z1BCSF v.1	20180702	Product data sheet	-	-		

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
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