ESD5342N

2-Lines, Uni-directional, Low Capacitance Transient Voltage Suppressor

http//:www.sh-willsemi.com

Descriptions

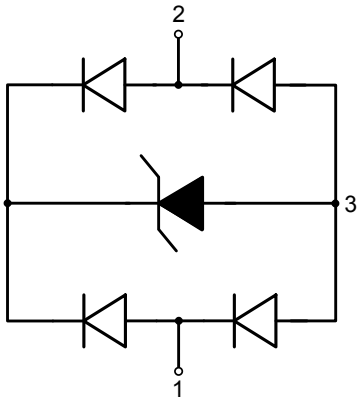
The ESD5342N is a low capacitance TVS (Transient Voltage Suppressor) designed to protect high speed data interfaces. It has been specifically designed to protect sensitive electronic components which are connected to data and transmission lines from over-stress caused by ESD (Electrostatic Discharge).

The ESD5342N incorporates two pairs of low capacitance steering diodes plus a TVS diode.

The ESD5342N may be used to provide ESD protection up to ±20kV (contact discharge) according to IEC61000-4-2, and withstand peak pulse current up to 4A (8/20μs) according to IEC61000-4-5.

The ESD5342N is available in DFN1006-3L package. Standard products are Pb-free and Halogen-free.

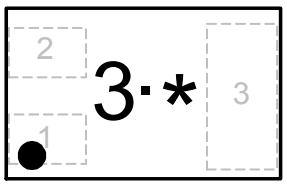
DFN1006-3L (Bottom View)



Circuit diagram

Features

- Stand-off voltage: 5V max.
- Transient protection for each line according to
  IEC61000-4-2 (ESD): ±20kV (contact discharge)
  IEC61000-4-4 (EFT): 40A (5/50ns)
  IEC61000-4-5 (surge): 4A (8/20μs)
- Low capacitance: C_J = 1.0pF typ.
- Ultra-low leakage current: I_R <1nA typ.
- Low clamping voltage: V_{CL} = 17.5V @ I_{PP} = 16A (TLP)
- Solid-state silicon technology



3 = Device code
* = Month code (A~Z)

Marking (Top View)

Applications

- USB Interface
- HDMI Interface
- DVI
- Portable Electronics
- Notebooks

Order information

Device	Package	Shipping
ESD5342N-3/TR	DFN1006-3L	10000/Tape&Reel

Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Peak pulse power (t_p = 8/20μs)	P_{pk}	60	W
Peak pulse current (t_p = 8/20μs)	I_{PP}	4	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	±20	kV
ESD according to IEC61000-4-2 contact discharge		±20	
Junction temperature	T_J	125	°C
Operating temperature	T_{OP}	-40~85	°C
Lead temperature	T_L	260	°C
Storage temperature	T_{STG}	-55~150	°C

Electrical characteristics (T_A = 25°C, unless otherwise noted)

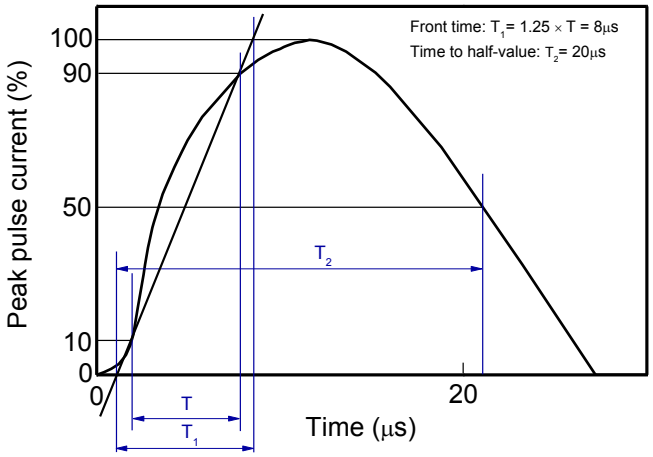
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reverse maximum working voltage	V_{RWM}				5.0	V
Reverse leakage current	I_R	V_{RWM} = 5V		<1	100	nA
Reverse breakdown voltage	V_{BR}	I_T = 1mA	7.0	8.0	9.0	V
Forward voltage	V_F	I_T = 10mA	0.6	0.9	1.2	V
Clamping voltage 1)	V_{CL}	I_{PP} = 16A, t_p = 100ns		17.5		V
Dynamic resistance 1)	R_{DYN}			0.55		Ω
Clamping voltage 2)	V_{CL}	I_{PP} = 1A, t_p = 8/20μs			11	V
		I_{PP} = 4A, t_p = 8/20μs			15	V
Junction capacitance	C_J	V_R = 0V, f = 1MHz Pin1 or 2 to Pin3		1.0	1.4	pF
		V_R = 0V, f = 1MHz Between Pin1 and Pin2		0.5	0.7	pF

Notes:

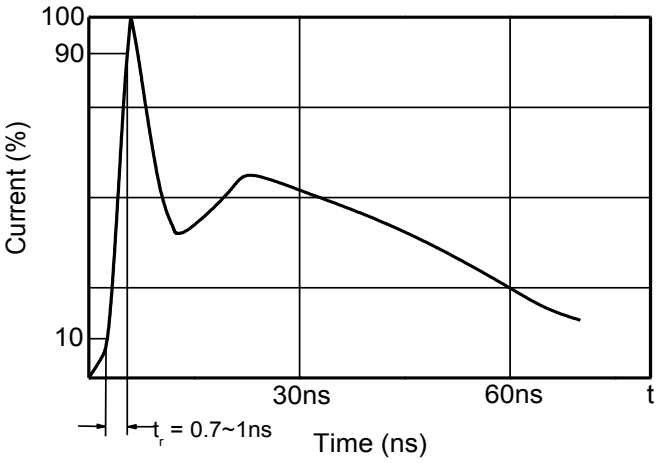
1) *TLP parameter: Z_0 = 50Ω, t_p = 100ns, t_r = 2ns, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.*

2) *Non-repetitive current pulse, according to IEC61000-4-5.*

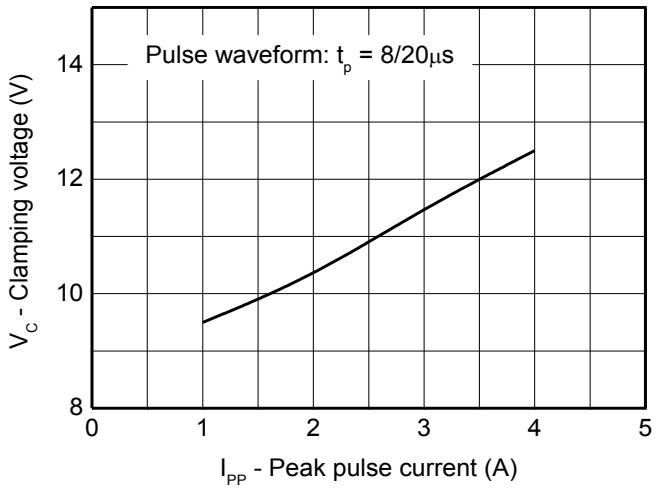
Typical characteristics (T_A = 25°C, unless otherwise noted)



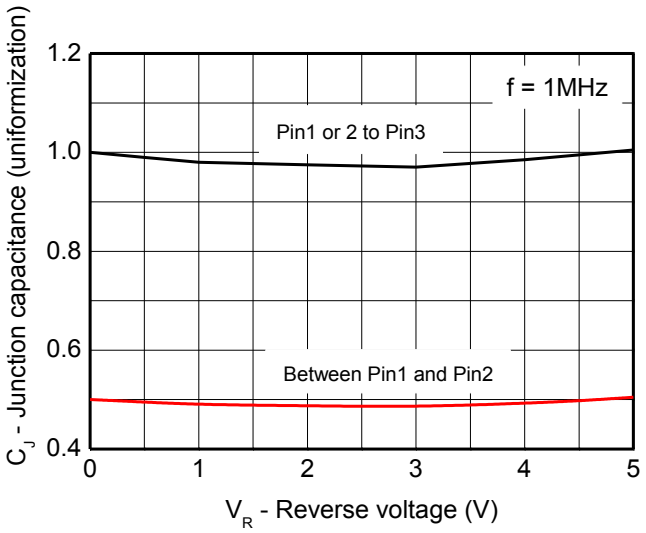
8/20μs waveform per IEC61000-4-5



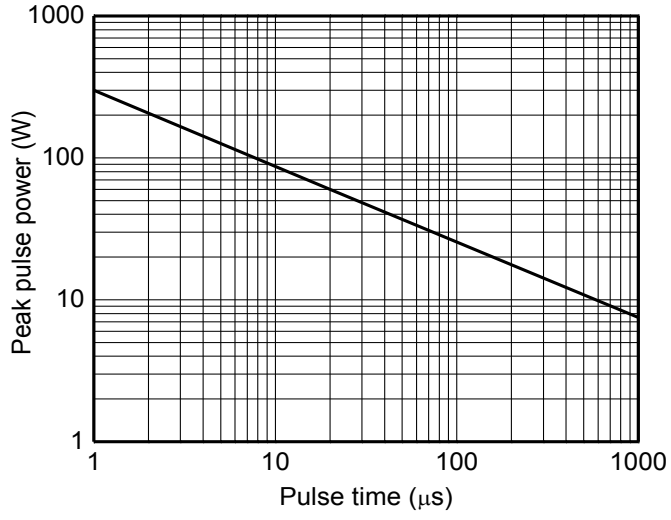
Contact discharge current waveform per IEC61000-4-2



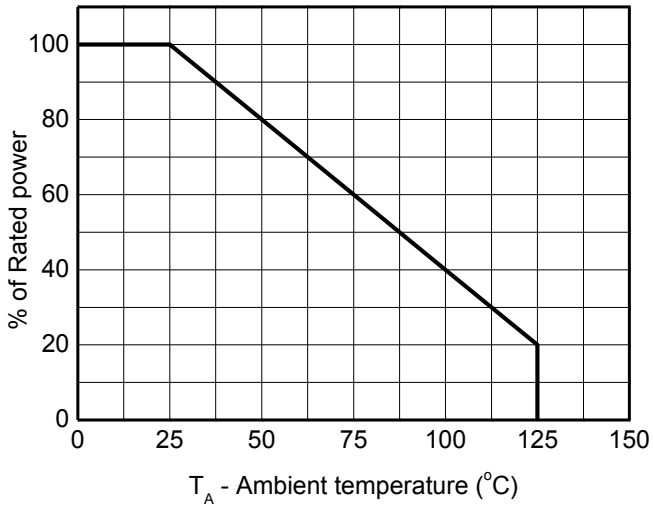
Clamping voltage vs. Peak pulse current



Capacitance vs. Reverse voltage

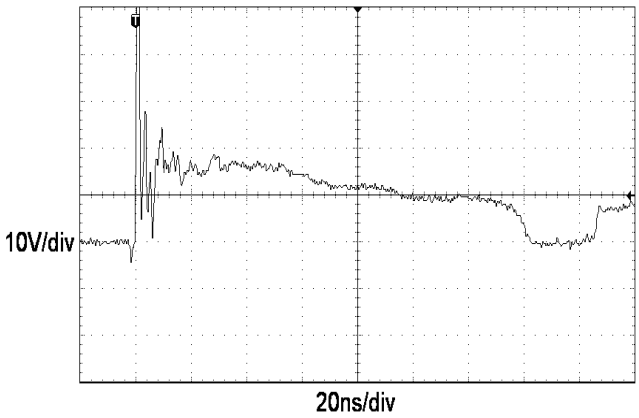


Non-repetitive peak pulse power vs. Pulse time



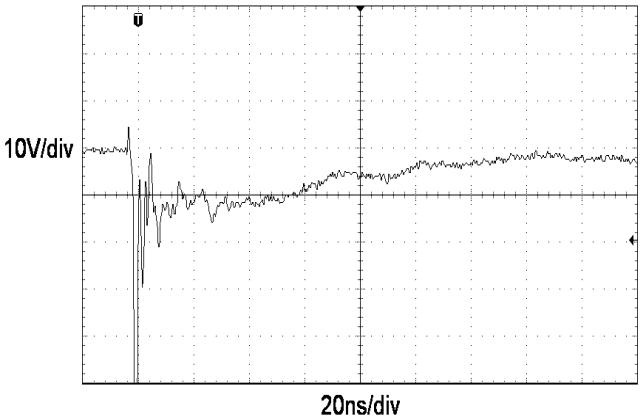
Power derating vs. Ambient temperature

Typical characteristics (T_A = 25°C, unless otherwise noted)



ESD clamping

(+8kV contact discharge per IEC61000-4-2)



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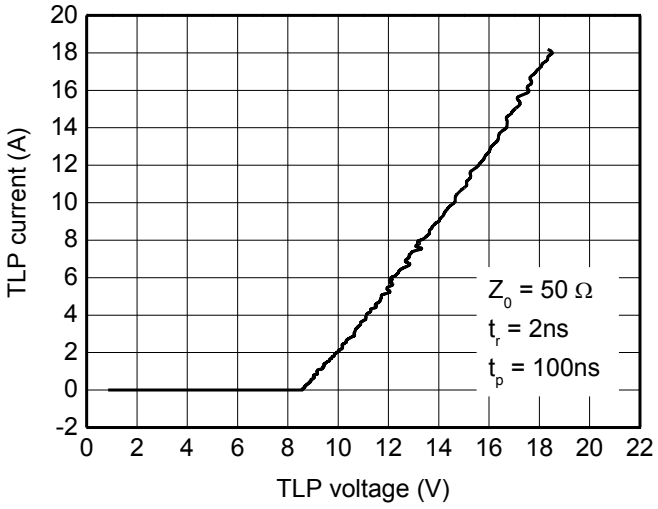


TLP Measurement

Application Information

The ESD5342N is designed to protect two high speed lines against ESD. Fig1 is shown the connection and Fig2 is shown PCB Layout guide for USB interface ESD protection

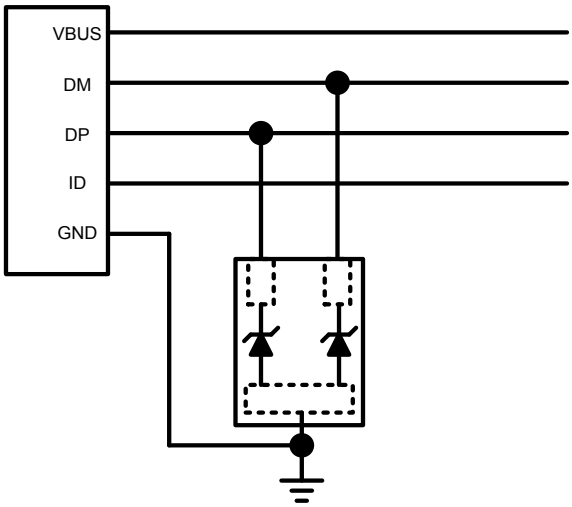


Fig1

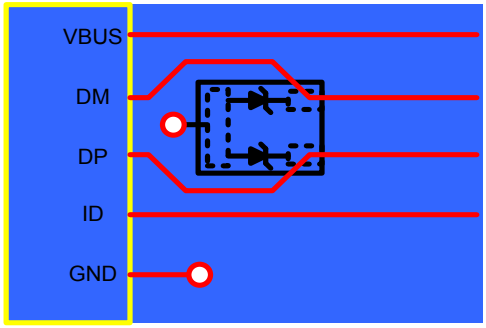
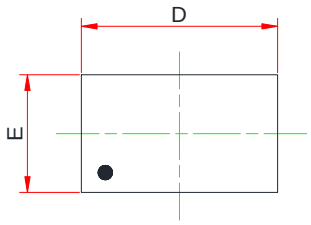


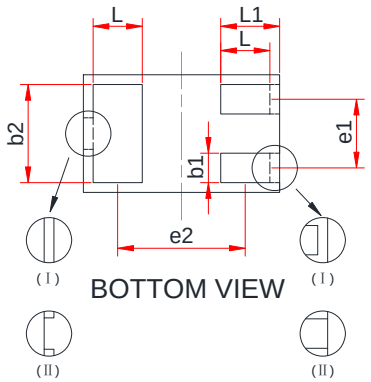
Fig2

PACKAGE OUTLINE DIMENSIONS

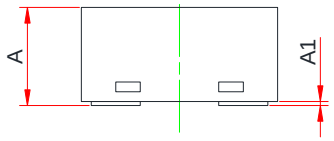
DFN1006-3L



TOP VIEW



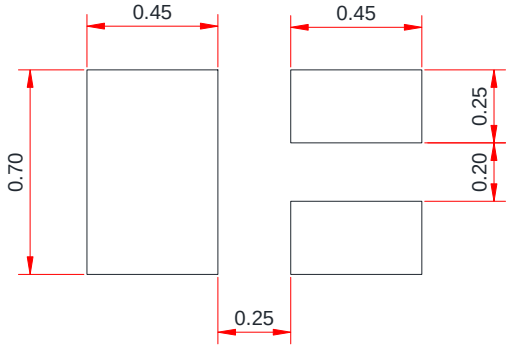
BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.36	-	0.50
A1	0.00	-	0.05
D	0.95	1.00	1.05
E	0.55	0.60	0.65
b1	0.10	0.15	0.20
b2	0.40	0.50	0.60
L	0.20	0.25	0.30
L1	0.20	0.30	0.40
e1	0.35 BSC		
e2	0.65 BSC		

Recommend PCB Layout (Unit: mm)

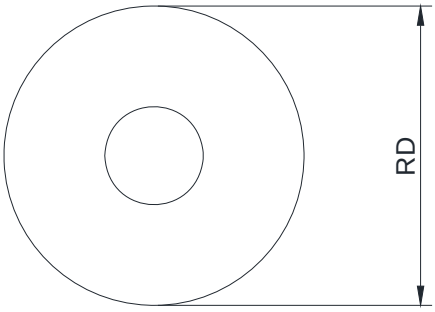


Notes:

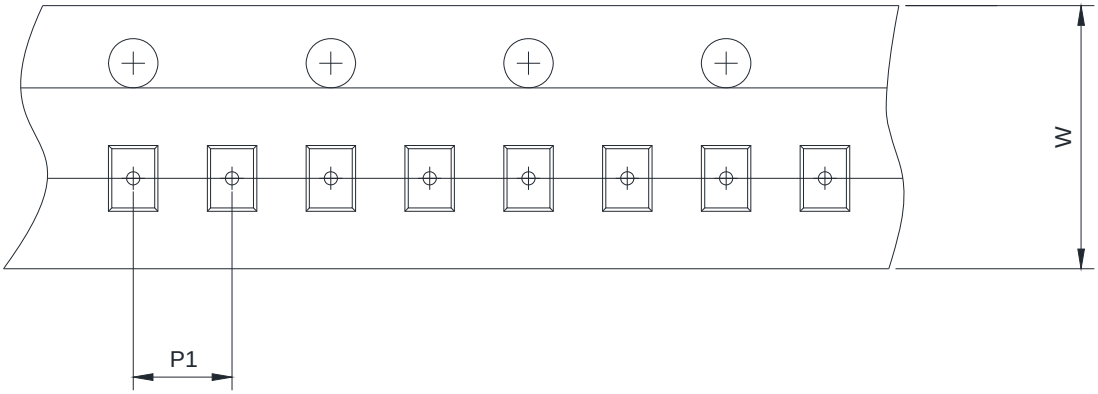
This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

TAPE AND REEL INFORMATION

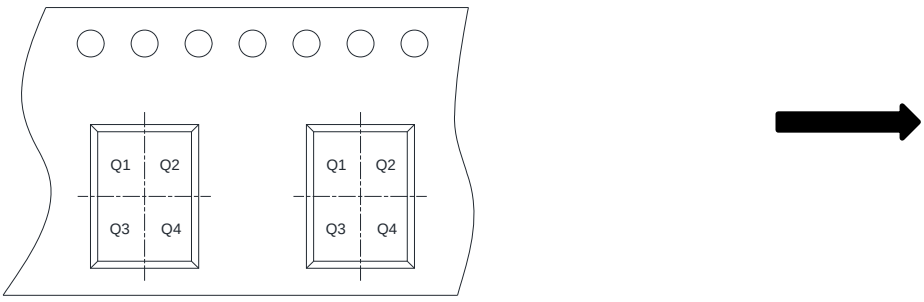
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑ 7inch ☐ 13inch
W	Overall width of the carrier tape	☑ 8mm ☐ 12mm ☐ 16mm
P1	Pitch between successive cavity centers	☑ 2mm ☐ 4mm ☐ 8mm
Pin1	Pin1 Quadrant	☑ Q1 ☐ Q2 ☐ Q3 ☐ Q4