

DS90LV028AQ Automotive LVDS Dual Differential Line Receiver

 Check for Samples: [DS90LV028AQ](#), [DS90LV028AQ-Q1](#)

FEATURES

- AECQ-100 Grade 1
- -40°C to +125°C Operating Temperature Range
- >400 Mbps (200 MHz) Switching Rates
- 50 ps Differential Skew (Typical)
- 0.1 ns Channel-to-Channel Skew (Typical)
- 2.5 ns Maximum Propagation Delay
- 3.3V Power Supply Design
- Flow-Through Pinout
- Power Down High Impedance on LVDS Inputs
- Low Power design (18mW @ 3.3V static)
- LVDS Inputs Accept LVDS/CML/LVPECL Signals
- Conforms to ANSI/TIA/EIA-644 Standard
- Available in SOIC Package

DESCRIPTION

The DS90LV028AQ is a dual CMOS differential line receiver designed for applications requiring ultra low power dissipation, low noise and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV028AQ accepts low voltage (350 mV typical) differential input signals and translates them to 3V CMOS output levels. The DS90LV028AQ has a flow-through design for easy PCB layout.

The DS90LV028AQ and companion LVDS line driver DS90LV027AQ provide a new alternative to high power PECL/ECL devices for high speed point-to-point interface applications.

Connection Diagram

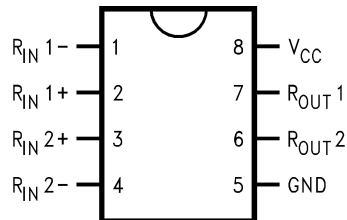
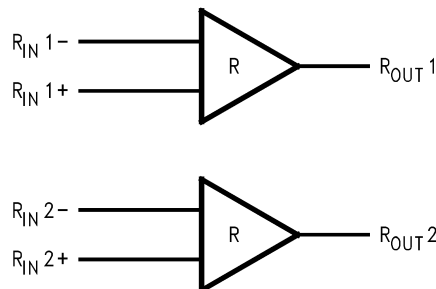


Figure 1. SOIC
See Package Number D0008A

Functional Diagram



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Truth Table

INPUTS	OUTPUT
$[R_{IN+}] - [R_{IN-}]$	R_{OUT}
$V_{ID} \geq 0.1V$	H
$V_{ID} \leq -0.1V$	L



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾⁽²⁾

Supply Voltage (V_{CC})	-0.3V to +4V
Input Voltage (R_{IN+} , R_{IN-})	-0.3V to +3.9V
Output Voltage (R_{OUT})	-0.3V to $V_{CC} + 0.3V$
Maximum Package Power Dissipation @ +25°C	
D Package	1068 mW
Derate D Package	9.71 mW/°C above +25°C
Package Thermal Resistance (4-Layer, 2 oz. Cu, JEDEC)	
θ_{JA}	103.0°C/W
θ_{JC}	41.0°C/W
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range Soldering	
(4 sec.)	+260°C
Maximum Junction Temperature	+135°C
ESD Rating	
HBM ⁽³⁾	≥ 8 kV
MM ⁽⁴⁾	≥ 250 V
CDM ⁽⁵⁾	≥ 1250 V

- (1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. Electrical Characteristics specifies conditions of device operation.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human Body Model, applicable std. JESD22-A114C
- (4) Machine Model, applicable std. JESD22-A115-A
- (5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+3.0	+3.3	+3.6	V
Receiver Input Voltage	GND		3.0	V
Operating Free Air				
Temperature (T_A)	-40	25	+125	°C

Electrical Characteristics

 Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. ⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units	
V _{TH}	Differential Input High Threshold	V _{CM} = +1.2V, 0V, 3V	R _{IN+} , R _{IN-}			+100	mV	
V _{TL}	Differential Input Low Threshold			-100			mV	
I _{IN}	Input Current	V _{IN} = +2.8V		V _{CC} = 3.6V or 0V	-10	±1	+10	µA
		V _{IN} = 0V			-10	±1	+10	µA
		V _{IN} = +3.6V	V _{CC} = 0V		-20		+20	µA
V _{OH}	Output High Voltage	I _{OH} = -0.4 mA, V _{ID} = +200 mV	R _{OUT}	2.7	3.1		V	
		I _{OH} = -0.4 mA, Inputs terminated		2.7	3.1		V	
		I _{OH} = -0.4 mA, Inputs shorted		2.7	3.1		V	
V _{OL}	Output Low Voltage	I _{OL} = 2 mA, V _{ID} = -200 mV			0.3	0.5	V	
I _{OS}	Output Short Circuit Current	V _{OUT} = 0V ⁽³⁾			-15	-50	-100	mA
V _{CL}	Input Clamp Voltage	I _{CL} = -18 mA			-1.5	-0.8		V
I _{CC}	No Load Supply Current	Inputs Open	V _{CC}		5.4	9	mA	

- (1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified (such as V_{ID}).
- (2) All typicals are given for: V_{CC} = +3.3V and T_A = +25°C.
- (3) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.

Switching Characteristics

 Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. ⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t _{PHLD}	Differential Propagation Delay High to Low	C _L = 15 pF	1.0	1.6	2.5	ns
t _{PLHD}	Differential Propagation Delay Low to High	V _{ID} = 200 mV	1.0	1.7	2.5	ns
t _{SKD1}	Differential Pulse Skew t _{PHLD} - t _{PLHD} ⁽⁴⁾	(Figure 2 and Figure 3)	0	50	650	ps
t _{SKD2}	Differential Channel-to-Channel Skew-same device ⁽⁵⁾		0	0.1	0.5	ns
t _{SKD3}	Differential Part to Part Skew ⁽⁶⁾		0		1.0	ns
t _{SKD4}	Differential Part to Part Skew ⁽⁷⁾		0		1.5	ns
t _{TLH}	Rise Time			325	800	ps
t _{THL}	Fall Time			225	800	ps
f _{MAX}	Maximum Operating Frequency ⁽⁸⁾			250		MHz

- (1) All typicals are given for: V_{CC} = +3.3V and T_A = +25°C.
- (2) C_L includes probe and jig capacitance.
- (3) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r and t_f (0% to 100%) ≤ 3 ns for R_{IN}.
- (4) t_{SKD1} is the magnitude difference in differential propagation delay time between the positive-going-edge and the negative-going-edge of the same channel.
- (5) t_{SKD2} is the differential channel-to-channel skew of any event on the same device. This specification applies to devices having multiple receivers within the integrated circuit.
- (6) t_{SKD3}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
- (7) t_{SKD4}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over the recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max - Min| differential propagation delay.
- (8) f_{MAX} generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, differential (1.05V to 1.35 peak to peak). Output criteria: 60%/40% duty cycle, V_{OL} (max 0.4V), V_{OH} (min 2.7V), load = 15 pF (stray plus probes).

Parameter Measurement Information

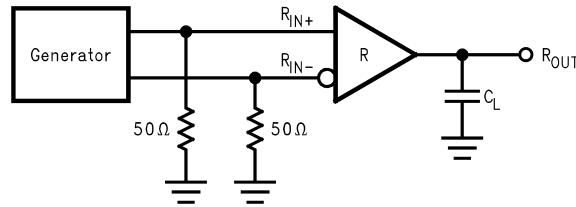


Figure 2. Receiver Propagation Delay and Transition Time Test Circuit

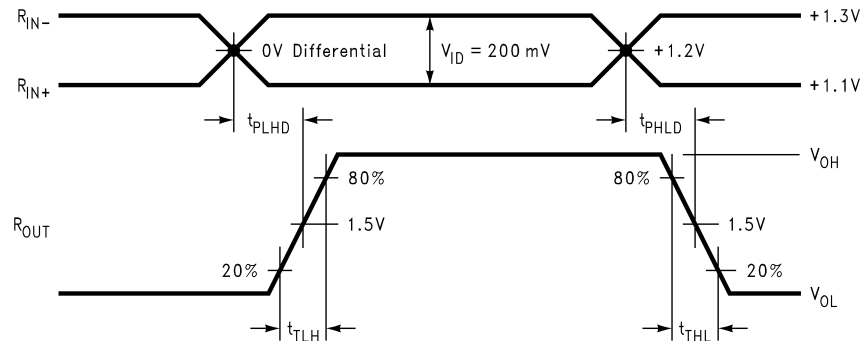


Figure 3. Receiver Propagation Delay and Transition Time Waveforms

Typical Application

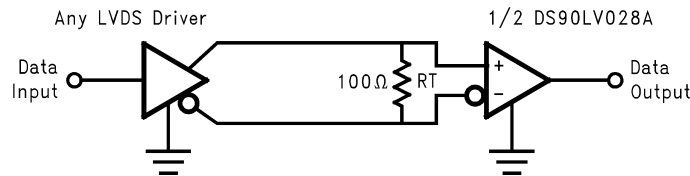


Figure 4. Balanced System Point-to-Point Application

APPLICATION INFORMATION

General application guidelines and hints for LVDS drivers and receivers may be found in the following application notes: LVDS Owner's Manual at www.ti.com.

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 4. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90LV028AQ differential line receiver is capable of detecting signals as low as 100 mV, over a $\pm 1V$ common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift $\pm 1V$ around this center point. The $\pm 1V$ shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. The AC parameters of both receiver input pins are optimized for a recommended operating input voltage range of 0V to +2.4V (measured from each pin to ground). The device will operate for receiver input voltages up to V_{CC} , but exceeding V_{CC} will turn on the ESD protection circuitry which will clamp the bus voltages.

POWER DECOUPLING RECOMMENDATIONS

Bypass capacitors must be used on power pins. Use high frequency ceramic (surface mount is recommended) 0.1 μ F and 0.01 μ F capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10 μ F (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board between the supply and ground.

PC BOARD CONSIDERATIONS

Use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL signals may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

DIFFERENTIAL TRACES

Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10mm long). This will help eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result! (Note that the velocity of propagation, $v = c/E_r$ where c (the speed of light) = 0.2997mm/ps or 0.0118 in/ps). Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

TERMINATION

Use a termination resistor which best matches the differential impedance or your transmission line. The resistor should be between 90 Ω and 130 Ω . Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work correctly without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice.

Surface mount 1% - 2% resistors are the best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be < 10mm (12mm MAX).

INPUT FAILSAFE BIASING

External pull up and pull down resistors may be used to provide enough of an offset to enable an input failsafe under open-circuit conditions. This configuration ties the positive LVDS input pin to VDD thru a pull up resistor and the negative LVDS input pin is tied to GND by a pull down resistor. The pull up and pull down resistors should be in the 5k Ω to 15k Ω range to minimize loading and waveform distortion to the driver. The common-mode bias point ideally should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry. Please refer to application note AN-1194, "Failsafe Biasing of LVDS Interfaces" ([SNLA051](#)) for more information.

PROBING LVDS TRANSMISSION LINES

Always use high impedance (> 100k Ω), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will give deceiving results.

CABLES AND CONNECTORS, GENERAL COMMENTS

When choosing cable and connectors for LVDS it is important to remember:

Use controlled impedance media. The cables and connectors you use should have a matched differential impedance of about 100 Ω . They should not introduce major impedance discontinuities.

Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation a common-mode (not differential mode) noise which is rejected by the receiver.

For cable distances < 0.5M, most cables can be made to work effectively. For distances $0.5M \leq d \leq 10M$, CAT 3 (category 3) twisted pair cable works well, is readily available and relatively inexpensive.

PIN DESCRIPTIONS

Pin Number	Name	Description
1, 4	R _{IN-}	Inverting receiver input pin
2, 3	R _{IN+}	Non-inverting receiver input pin
6, 7	R _{OUT}	Receiver output pin
8	V _{CC}	Power supply pin, +3.3V \pm 0.3V
5	GND	Ground pin

Typical Performance Curves

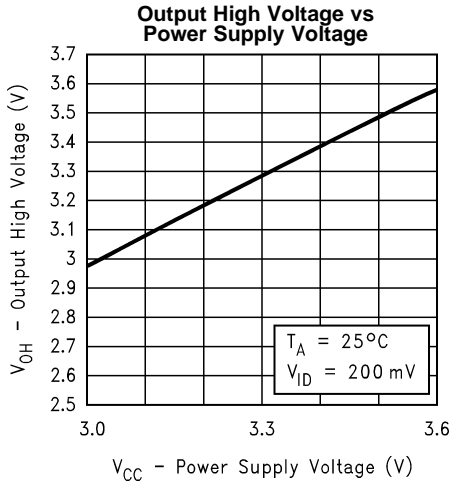


Figure 5.

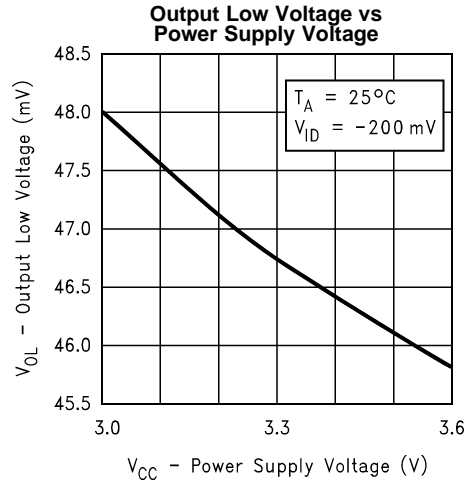


Figure 6.

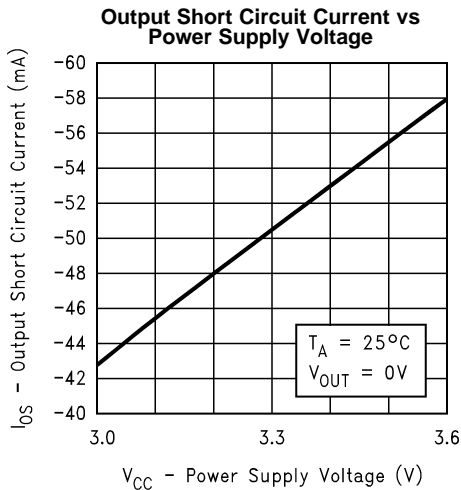


Figure 7.

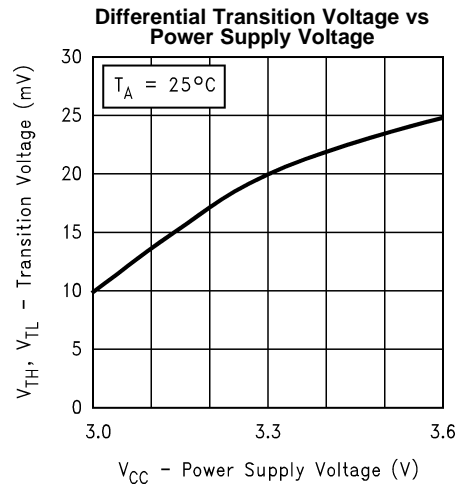


Figure 8.

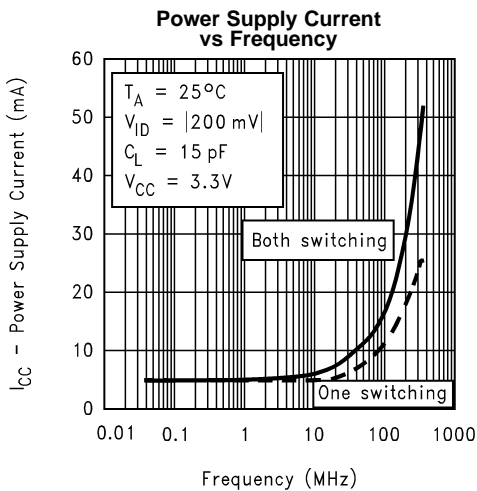


Figure 9.

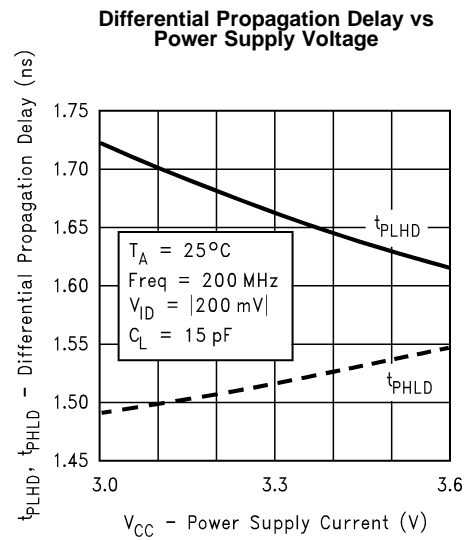


Figure 10.

Typical Performance Curves (continued)

Differential Propagation Delay vs Differential Input Voltage

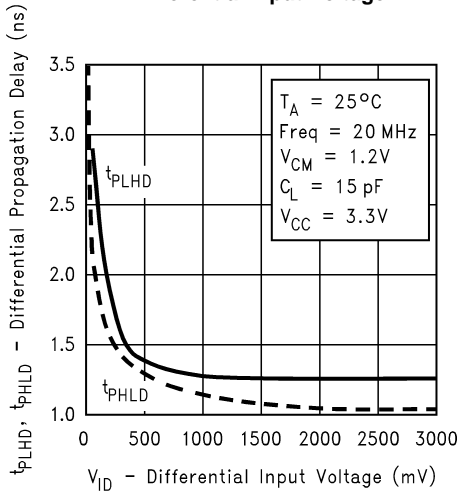


Figure 11.

Differential Propagation Delay vs Common-Mode Voltage

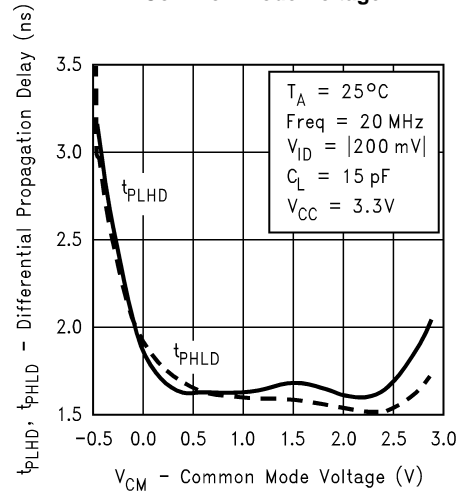


Figure 12.

Transition Time vs Power Supply Voltage

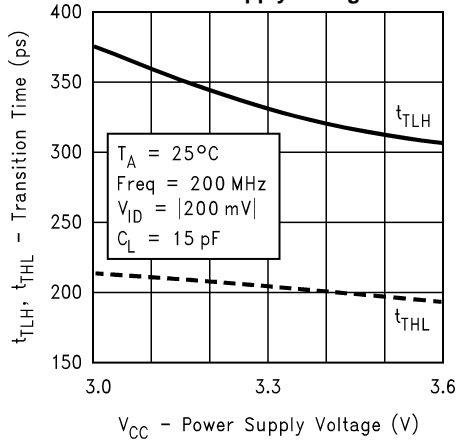


Figure 13.

Differential Skew vs Power Supply Voltage

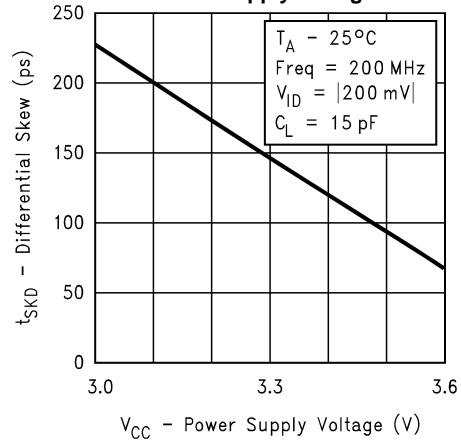


Figure 14.

Differential Propagation Delay vs Load

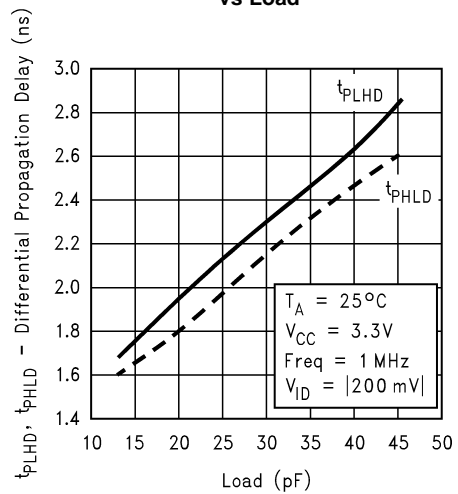


Figure 15.

Differential Propagation Delay vs Load

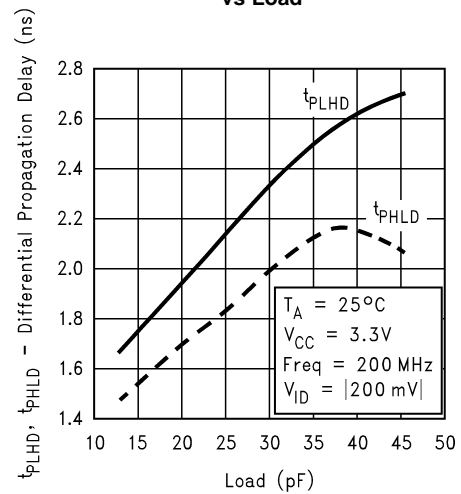
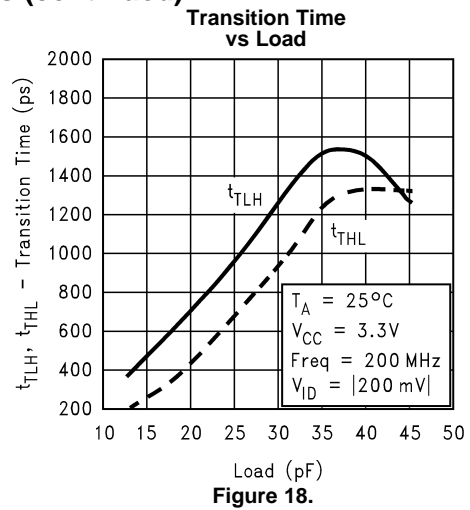
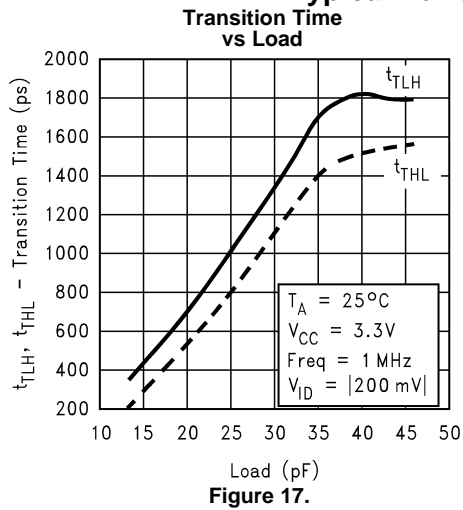


Figure 16.

Typical Performance Curves (continued)



REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90LV028AQMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	90LV0 28AQM	Samples
DS90LV028AQMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	90LV0 28AQM	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV028AQM/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV028AQMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

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Products

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