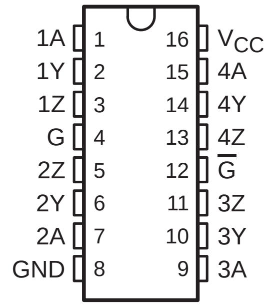
- **Switching Rates up to 32 MHz**
- **Operates From a Single 3.3-V Supply**
- **Propagation Delay Time . . . 8 ns Typ**
- **Pulse Skew Time . . . 500 ps Typ**
- **High Output-Drive Current . . . ±30 mA**
- **Controlled Rise and Fall Times . . . 3 ns Typ**
- **Differential Output Voltage With 100-Ω Load . . . 1.5 V Typ**
- **Ultra-Low Power Dissipation**
  - **dc, 0.3 mW Max**
  - **32 MHz All Channels (No Load), 385 mW Typ**
- **Accepts 5-V Logic Inputs With a 3.3-V Supply**
- **Low-Voltage Pin-to-Pin Compatible Replacement for AM26C31, AM26LS31, MB571**
- **High Output Impedance in Power-Off Condition**
- **Driver Output Short-Protection Circuit**
- **Package Options Include Plastic Small-Outline (D, NS) Packages**

D OR NS PACKAGE
(TOP VIEW)



The D package is available taped and reeled. The NS package is only available taped and reeled. Add the suffix R to device type (e.g., AM26LV31CDR).

description

The AM26LV31 is a BiCMOS quadruple differential line driver with 3-state outputs. It is designed to be similar to TIA/EIA-422-B and ITU Recommendation V.11 drivers with reduced supply-voltage range.

The device is optimized for balanced-bus transmission at switching rates up to 32 MHz. The outputs have very high current capability for driving balanced lines such as twisted-pair transmission lines and provide a high impedance in the power-off condition. The enable function is common to all four drivers and offers the choice of active-high or active-low enable inputs. The AM26LV31 is designed using Texas Instruments (TI™) proprietary LinIMPACT-C60™ technology, facilitating ultra-low power consumption without sacrificing speed. This device offers optimum performance when used with the AM26LV32 quadruple line receivers.

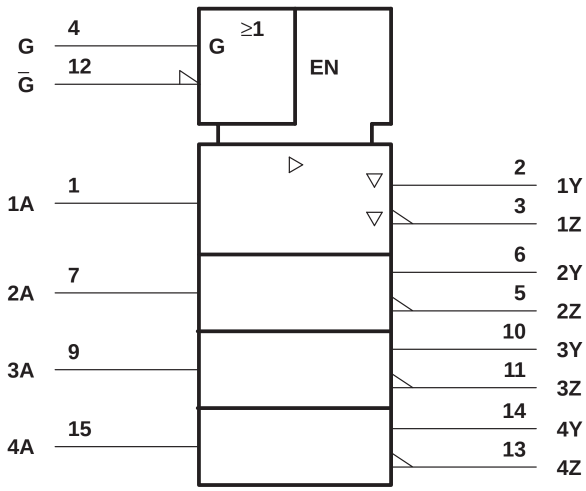
The AM26LV31C is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUT A	ENABLES		OUTPUTS	
	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

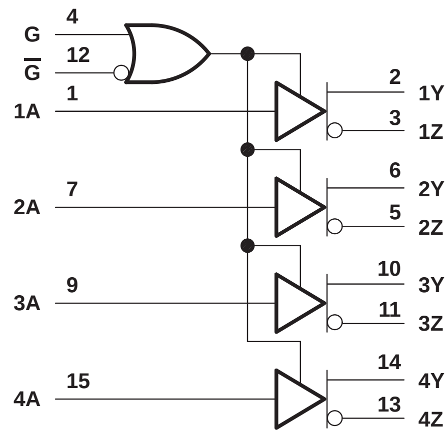
H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

logic symbol†

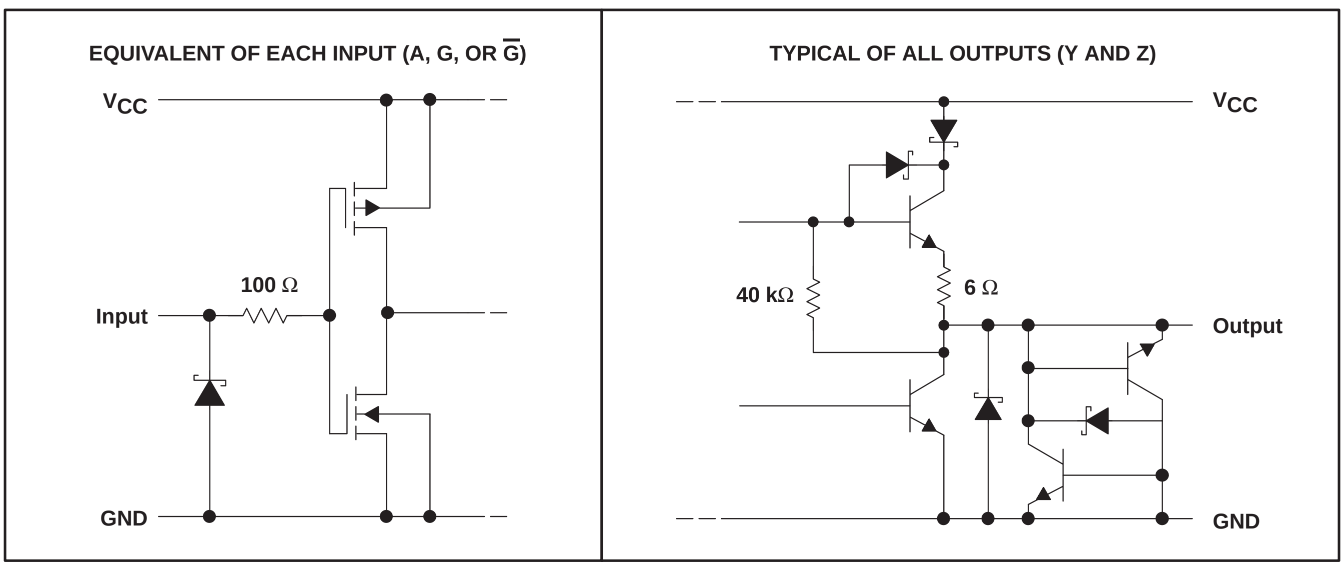


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each driver)



All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . –0.3 V to 6 V
Input voltage range, V_I . . . . –0.3 V to 6 V
Output voltage range, V_O . . . . –0.3 V to 6 V
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . 73°C/W
NS package . . . . 64°C/W
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			–30	mA
Low-level output current, I_{OL}			30	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating supply-voltage and free-air temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V,	I_{OH} = –12 mA	1.85	2.3		V
V_{OL}	Low-level output voltage	V_{IL} = 0.8 V,	I_{OH} = 12 mA		0.8	1.05	V
$\|V_{OD}\|$	Differential output voltage‡	R_L = 100 Ω		0.95	1.5		V
V_{OC}	Common-mode output voltage	R_L = 100 Ω		1.3	1.55	1.8	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡	R_L = 100 Ω				±0.2	V
I_O	Output current with power off	V_O = –0.25 V or 6 V,	V_{CC} = 0			±100	µA
I_{OZ}	Off-state (high-impedance state) output current	V_O = –0.25 V or 6 V,	G = 0.8 V or $\overline{G}$ = 2 V			±100	µA
I_{IH}	High-level input current	V_{CC} = 0 or 3 V,	V_I = 5.5 V			10	µA
I_{IL}	Low-level input current	V_{CC} = 3.6 V,	V_I = 0			–10	µA
I_{OS}	Short-circuit output current	V_{CC} = 3.6 V,	V_O = 0			–200	mA
I_{CC}	Supply current (all drivers)	V_I = V_{CC} or GND,	No load			100	µA
C_{pd}	Power dissipation capacitance (all drivers)§	No load			160		pF

† All typical values are at V_{CC} = 3.3 V and T_A = 25°C.
‡ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§ C_{pd} determines the no-load dynamic current consumption. $I_S = C_{pd} \times V_{CC} \times f + I_{CC}$

switching characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 2		4	8	12	ns
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 2		4	8	12	ns
t_t	Transition time (t_r or t_f)	See Figure 2			3		ns
SR	Slew rate, single-ended output voltage	See Note 3 and Figure 2			0.3	1	V/ns
t_{PZH}	Output-enable time to high level	See Figure 3			10	20	ns
t_{PZL}	Output-enable time to low level	See Figure 4			10	20	ns
t_{PHZ}	Output-disable time from high level	See Figure 3			10	20	ns
t_{PLZ}	Output-disable time from low level	See Figure 4			10	20	ns
$t_{sk(p)}$	Pulse skew	f = 32 MHz,	See Note 4		0.5	1.5	ns
$t_{sk(o)}$	Skew limit	f = 32 MHz,	See Note 5			1.5	ns
$t_{sk(lim)}$	Skew limit (device to device)	f = 32 MHz,	See Note 6			3	ns

NOTES: 3. Slew rate is defined by:

$$SR = \frac{90\%\left(V_{OH} - V_{OL}\right) - 10\%\left(V_{OH} - V_{OL}\right)}{t_r},$$ the differential slew rate of V_{OD} is 2 × SR.

4. Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
5. Skew limit is the difference between any two outputs of the same device switching in the same direction.
6. Skew limit (device to device) is the maximum difference in propagation delay times between any two channels of any two devices.

PARAMETER MEASUREMENT INFORMATION

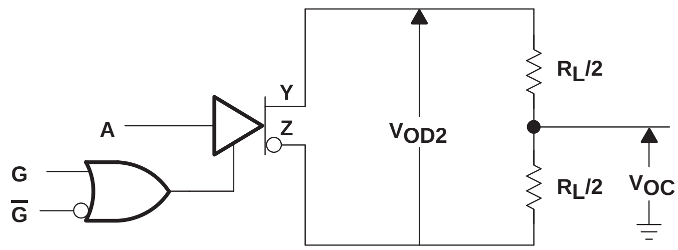
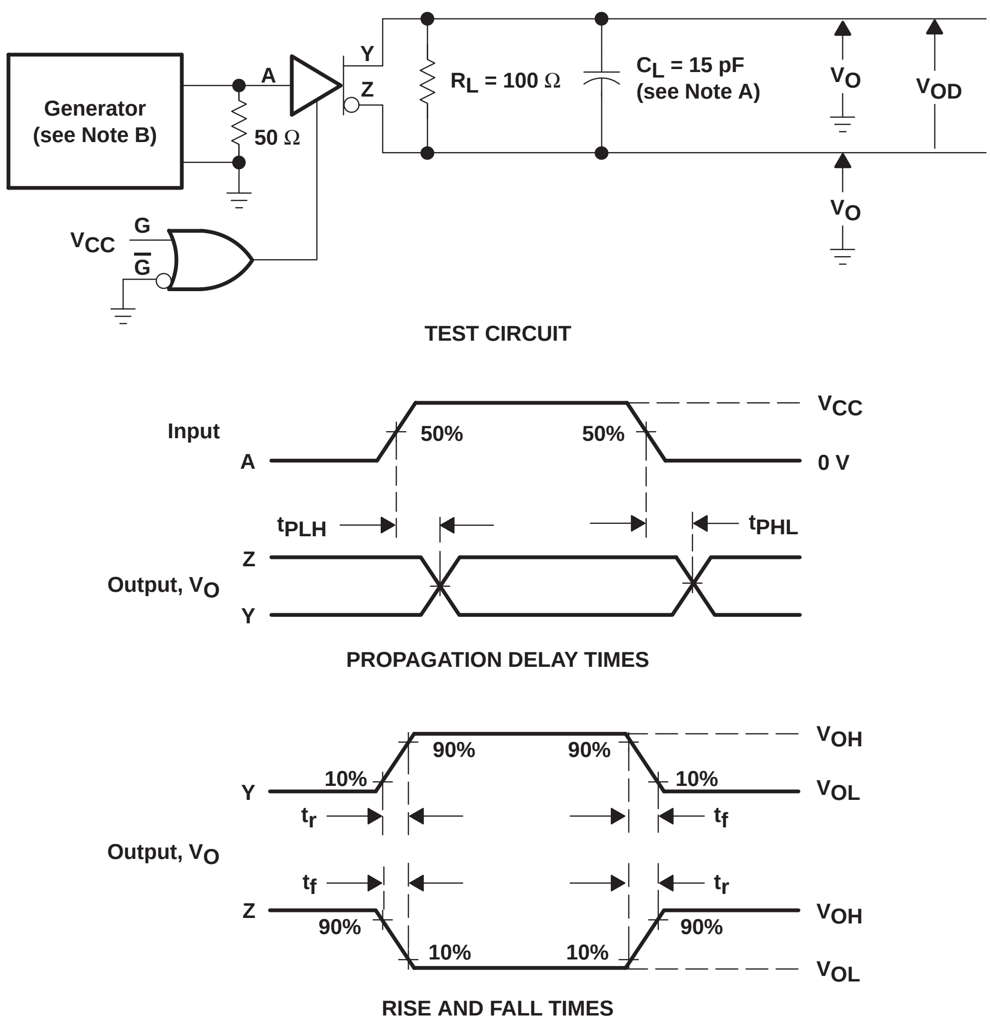


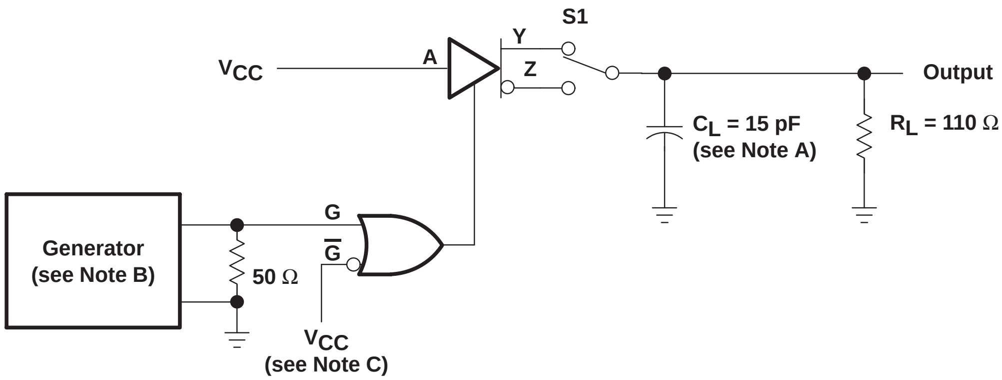
Figure 1. Differential and Common-Mode Output Voltages



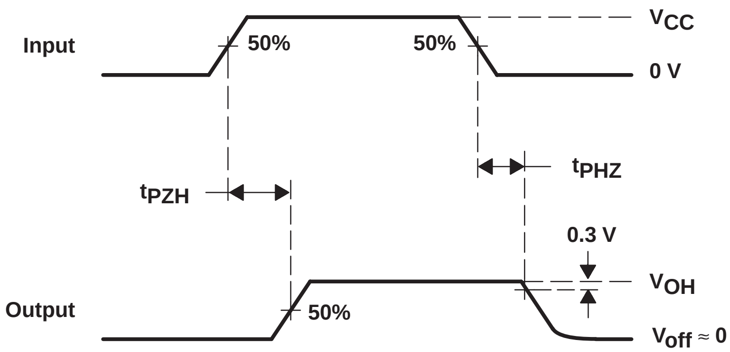
NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 32 MHz, $Z_O \approx 50\ \Omega$, 50% duty cycle, t_r and $t_f \leq 2$ ns.

Figure 2. Test Circuit and Voltage Waveforms, t_{PHL} and t_{PLH}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

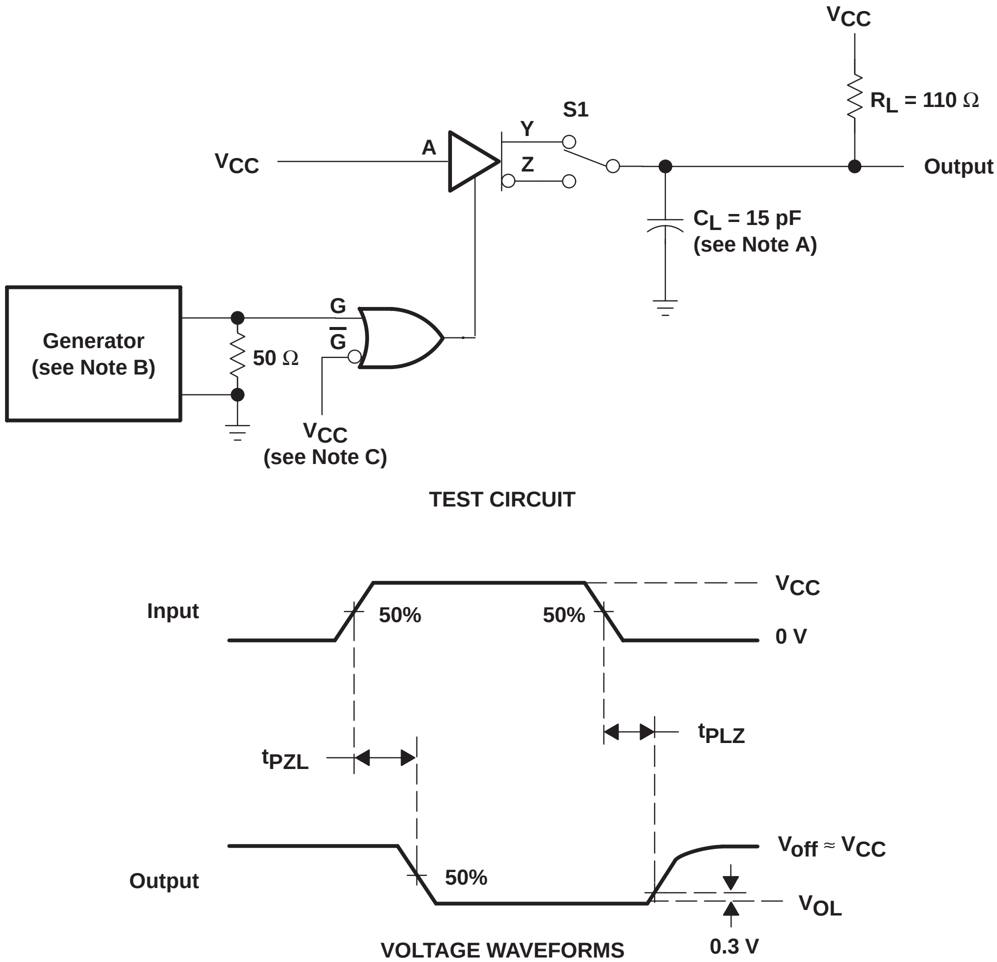


VOLTAGE WAVEFORMS

NOTES:
A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, 50% duty cycle, t_r and t_f (10% to 90%) ≤ 2 ns.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

Figure 3. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, 50% duty cycle, t_r and t_f (10% to 90%) ≤ 2 ns.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

Figure 4. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}