LX3005

2A STEP-DOWN CONVERTER

PRODUCTION DATASHEET

DESCRIPTION

The LX3005 is a 420kHz fixed frequency PWM buck (step-down) DC-DC converter, capable of driving a 2A load with high efficiency, low ripple and excellent line and load regulation. The device operates over a wide input voltage range of 4.75V to 25V, and the output voltage can be externally set from 0.8V to a voltage near VIN, as the PWM control circuit is able to adjust the duty ratio linearly from 0% to close to 100%.

The LX3005 device integrates a high-side low RDS_{ON} PMOS for a low cost and high efficiency solution. An internal transconductance error amplifier is used in the control loop allowing flexibility to compensate the system using an all ceramic capacitor system.

The LX3005 also features an enable function, internal circuitry for soft start, and protection schemes such as thermal shutdown, over-current protection, and short-circuit protection. When OCP or SCP is triggered, the device operating frequency will be reduced from typically 420kHz to typically 40kHz, limiting the output power capability.

The LX3005 serves as an ideal power supply device for portable devices, especially for chipset power in portable systems. It's widely used for PDVD, LCD monitor and DPF chipset power sources.

The LX3005 is available in SOIC8 package and is functional from an ambient temperature range of 0˚C to 85˚C.

IMPORTANT: : For the most current data, consult *MICROSEMI*'s website: http://www.microsemi.com

Patents Pending

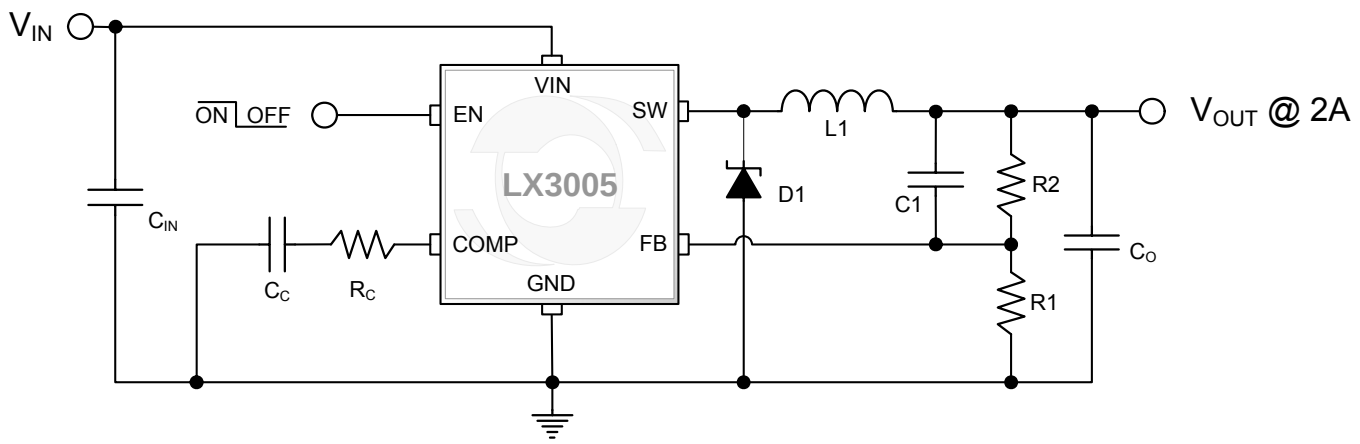
KEY FEATURES

- 2A Constant Output Current
- 130mΩ R_{DSON} Internal Power MOSFET
- Up to 94% Efficiency
- Fixed 420kHz Frequency
- Wide 4.75V to 25V Input Voltage Range
- Output Voltage Adjustable from 0.8V to 21V
- Built-in Thermal Shutdown Function
- Built-in Current Limit Function
- Built-in Soft-start Function
- Support Ceramic or Electrolytic Capacitors
- Pb-free and RoHS Compliant

APPLICATIONS

- Portable DVD
- LCD Monitor/LCD TV
- Digital Photo Frame
- ADSL
- Set-Top Box

PRODUCT HIGHLIGHT



PACKAGE ORDER INFO

T_A (°C)		
	DM	**Plastic SOIC 8-pin**
	RoHS Compliant / Pb-free	
0 to 85	**LX3005CDM**	

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX3005CDM-TR)

THERMAL DATA

θ_{JA} = 100°C/W

THERMAL RESISTANCE-JUNCTION TO AMBIENT

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$. The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

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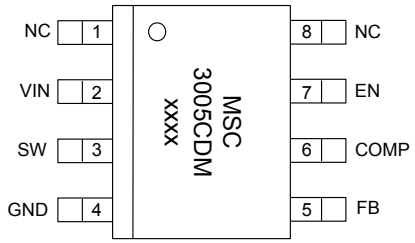
ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage (V_{IN}) ..... -0.3V to 30V
FB Pin Voltage (V_{FB}) ..... -0.3V to 6V
EN Pin Voltage (V_{EN}) ..... -0.3V to V_{IN}
COMP Pin Voltage (V_{COMP}) ..... -0.3V to 6V
SW Pin Voltage (V_{SW}) ..... -0.3V to V_{IN}
Power Dissipation (P_D) ..... Internally limited
Maximum Operating Junction Temperature ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 260°C

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

PACKAGE PIN OUT



DM PACKAGE
(Top View)
xxxx = date/lot code
RoHS / Pb-free 100% Matte Tin Pin Finish

FUNCTIONAL PIN DESCRIPTION

Name	Pin #	Description
NC	1	Pin not used.
VIN	2	Supply Voltage Pin. The LX3005 operates from a 4.75V to 25V DC voltage. Bypass VIN to GND with a suitable large capacitor to eliminate noise on the input.
SW	3	Power Switch Output Pin. SW is the switch node that supplies power to the output.
GND	4	Ground for IC.
FB	5	Feedback Pin. Through an external resistor divider network, FB senses the output voltage and regulates it. To prevent current limit run away in a short circuit fault condition, the frequency feedback comparator lowers the oscillator frequency to 40kHz when the FB voltage is below 0.52V. The feedback threshold voltage is 0.8V.
COMP	6	Compensation Pin. This pin is the output of the error amplifier. Frequency compensation is done at this pin by connecting a series RC to ground(parallel a capacitor if necessary)
EN	7	Enable Pin. Drive EN pin high to turn on the device, drive it low to turn off. Default of this pin is high level.
NC	8	Pin not used.

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ELECTRICAL CHARACTERISTICS

Unless otherwise listed, the following specifications at the operating ambient temperature 25°C and VIN = 12V, VOUT = 5V.

Parameter	Symbol	Test Conditions / Comment	Min	Typ	Max	Units
VIN						
Recommended Voltage Range	V_{IN}		4.75		25	V
Shut-Down Quiescent Current	I_{SHDN}	VEN = 0.4V		44	60	µA
Operating Quiescent Current	I_Q	VEN = 2V, V_{FB} = 1.3V		1.3	2	mA
ENABLE						
EN Pin Threshold	V_H		1.5			V
	V_L				0.7	
EN Pin Input Leakage Current	I_{FB}	V_{EN} = 2.5V		-5	-10	µA
FB VOLTAGE						
Internal FB Voltage	V_{FB}	VIN = 5V to 25V	0.784	0.8	0.816	V
Input Bias Current	I_{FB}	V_{FB} = 1.3V		-0.1	-0.5	µA
ERROR AMP						
Error Amplifier Voltage Gain	G_V			1000		V/V
Error Amplifier Transconductance	G_S			700		µA/V
OSCILLATOR						
Operating Frequency	f_{OSC}		336	420	504	kHz
HIGH SIDE DRIVER						
Internal PMOS ON Resistance	R_{DSON}	V_{FB} = 065V, V_{EN} = 12V, I_{OUT} = 2A, T_C = 25°C		130	150	ohm
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.65V, ISW = 0.1A			100	%
CURRENT LIMIT						
Switch Current Limit	I_{LIM}	T_C = 25°C	2.5	3.4		A
Frequency of Current Limit or Short Circuit Protection	GS			40		kHz
THERMAL SHUTDOWN						
Threshold	T_{OTSD}	NOTE1		155		°C
Hysteresis	T_{HYS}			20		°C

NOTE1: This parameter is guaranteed by design but not tested in production (GBNT).

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FUNCTIONAL BLOCK DIAGRAM

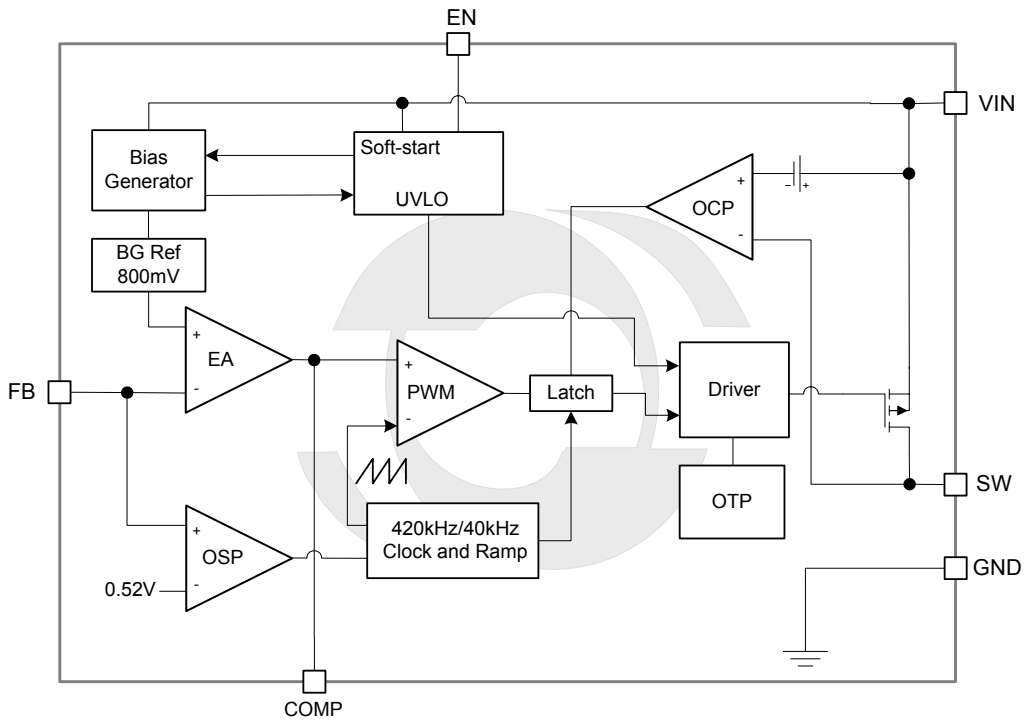

Figure 1. Block Diagram

TYPICAL APPLICATION

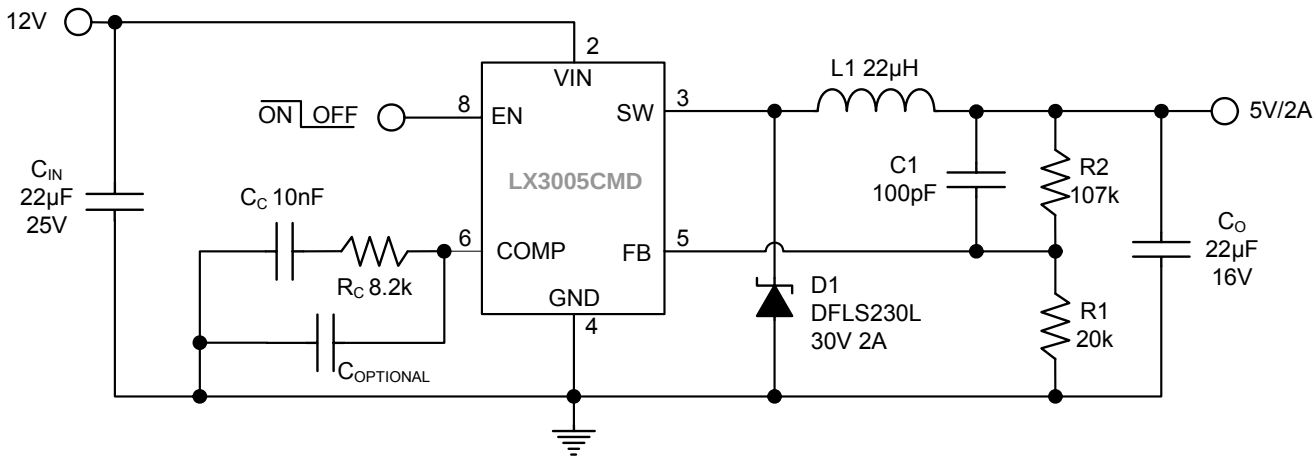

Figure 2. V_{IN} = 12V, V_{OUT} = 5V, Ceramic Capacitors Input & Output

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TYPICAL APPLICATION

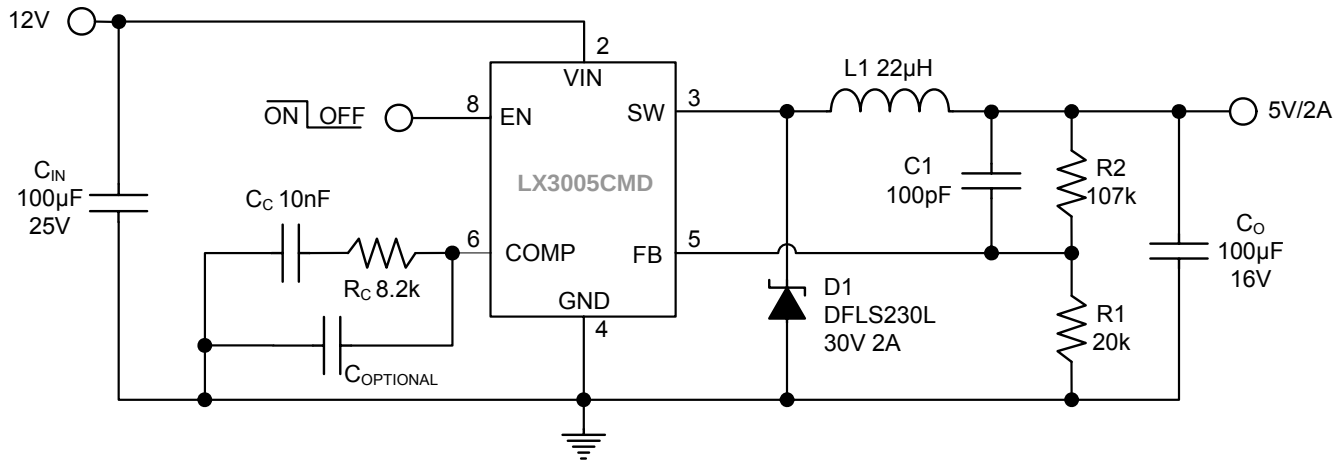
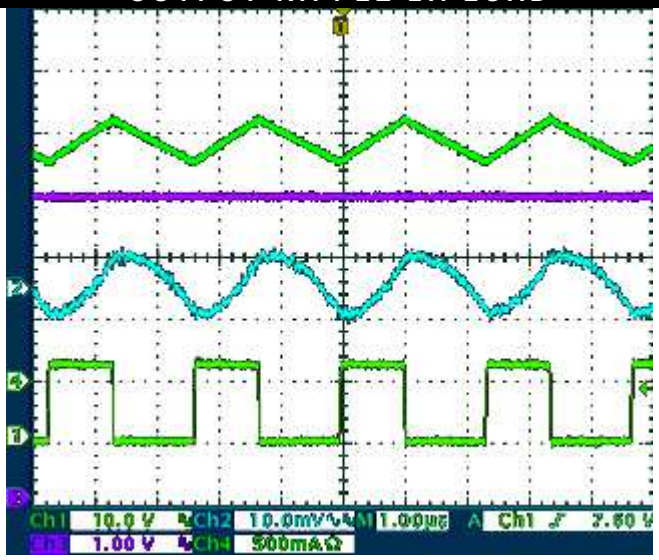


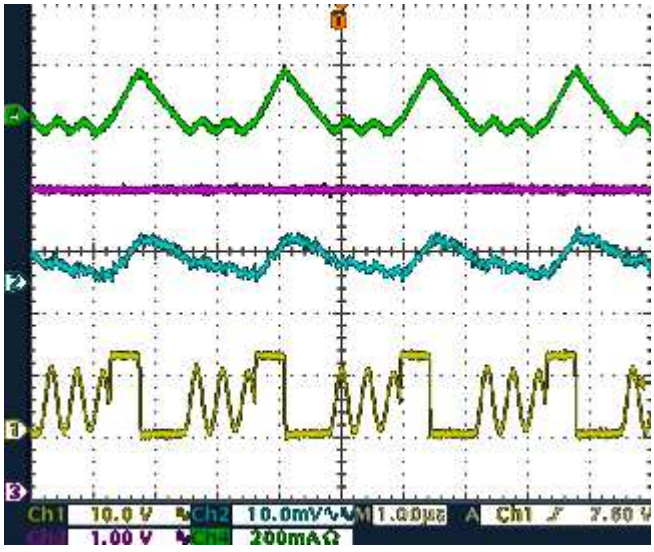
Figure 3. V_{IN} = 12V, V_{OUT} = 5V, Electrolytic Capacitors Input & Output

OUTPUT RIPPLE 2A LOAD



V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 2A, 10mVpp
22uF Ceramic Output Capacitor and a 22µH Inductor
Channel 1 – Switch Node
Channel 2 – VOUT AC Coupled
Channel 3 – VOUT
Channel 4 – Inductor Current

OUTPUT RIPPLE DISCONTINOUS MODE



V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 50mA
22uF ceramic output capacitors and a 22µH inductor
Channel 1 – Switch Node
Channel 2 – VOUT AC Coupled
Channel 3 – VOUT
Channel 4 – Inductor Current

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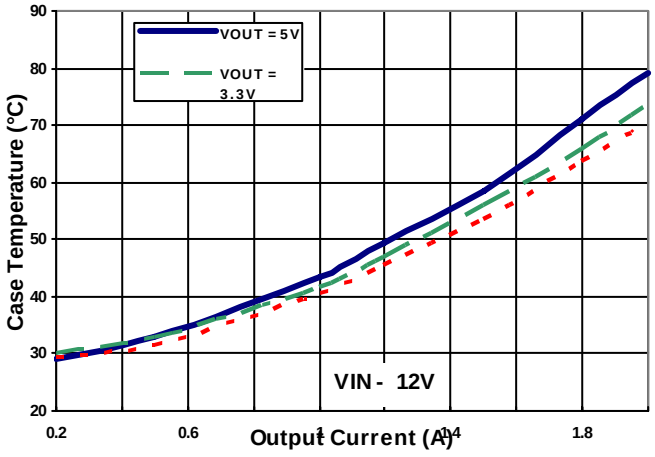
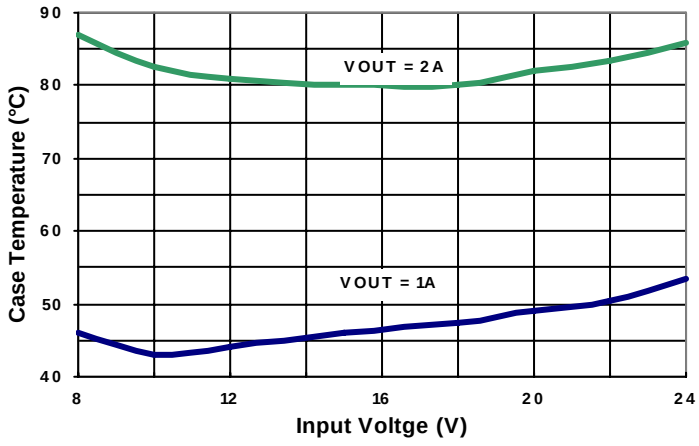
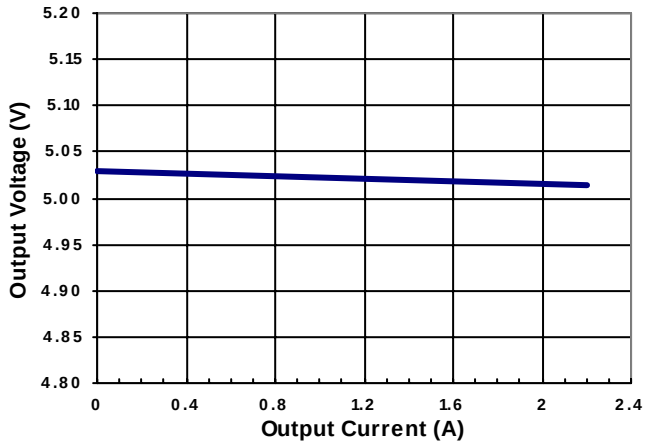
CASE TEMPERATURE VS IOUT & VOUT



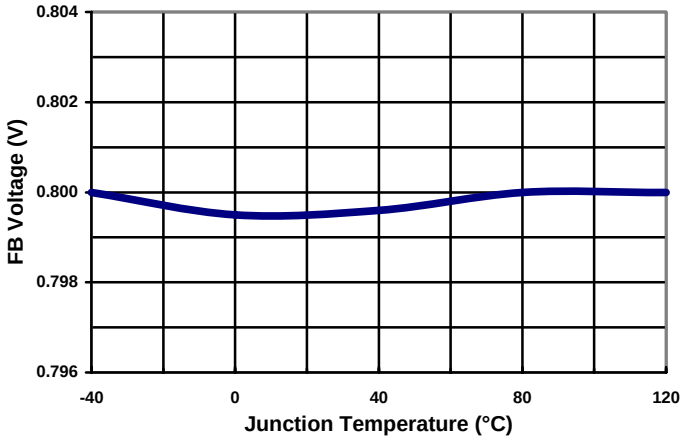
CASE TEMPERATURE VS VIN & IOUT



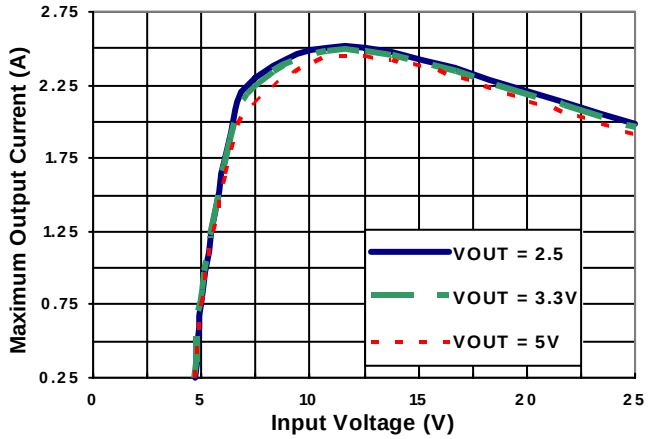
OUTPUT VOLTAGE V OUTPUT CURRENT



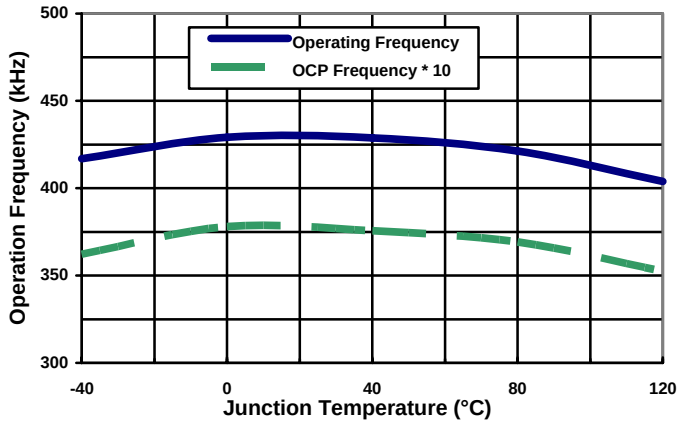
FB VOLTAGE VS TEMPERATURE



MAXIMUM IOUT VS INPUT VOLTAGE



OP & OCP FREQUENCY VS TEMPERATURE



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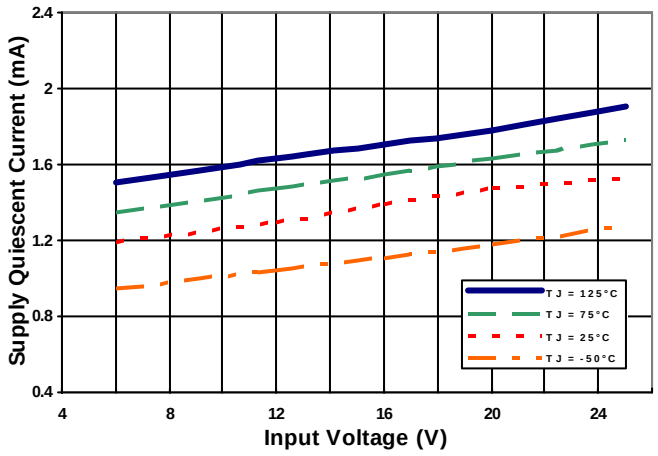
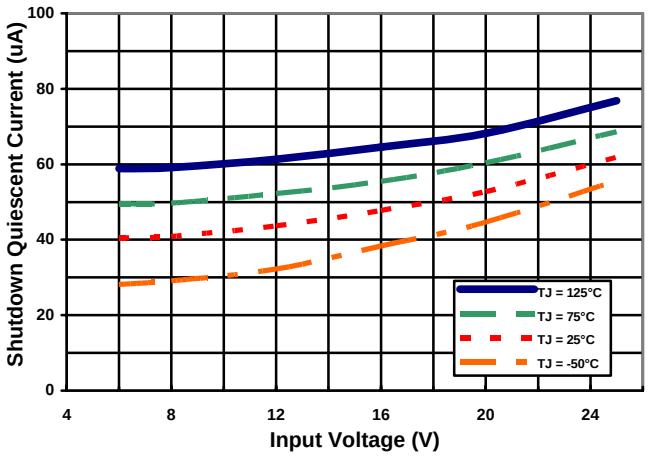
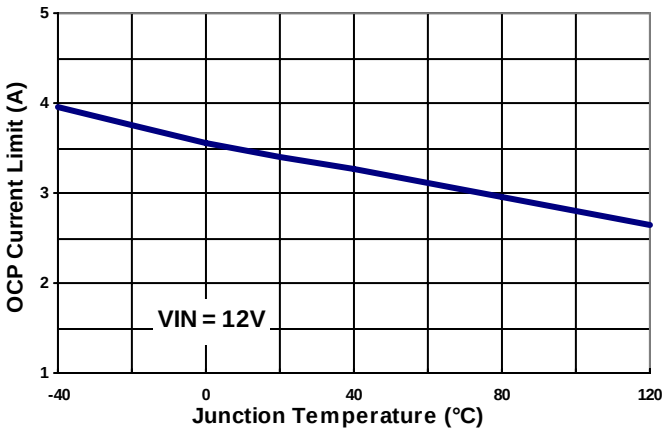
SUPPLY QUIESCENT CURRENT



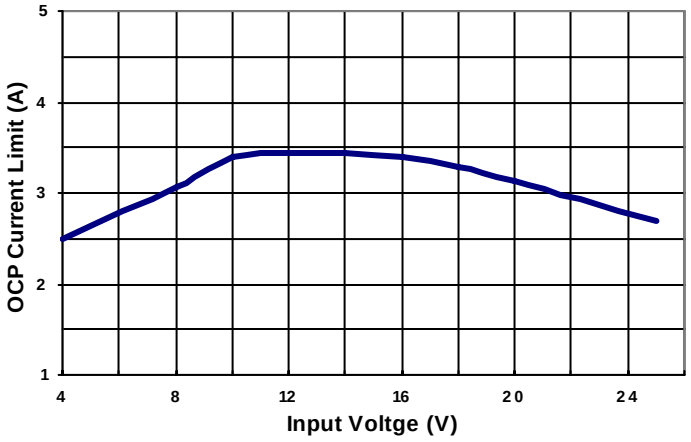
SHUTDOWN QUIESCENT CURRENT



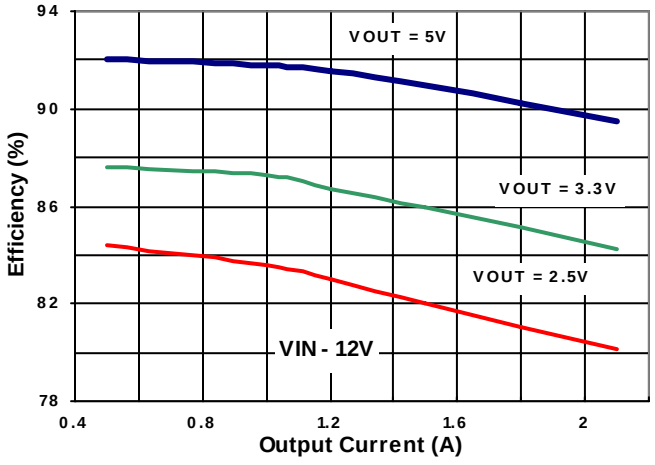
OCP CURRENT LIMIT VS TEMPERATURE



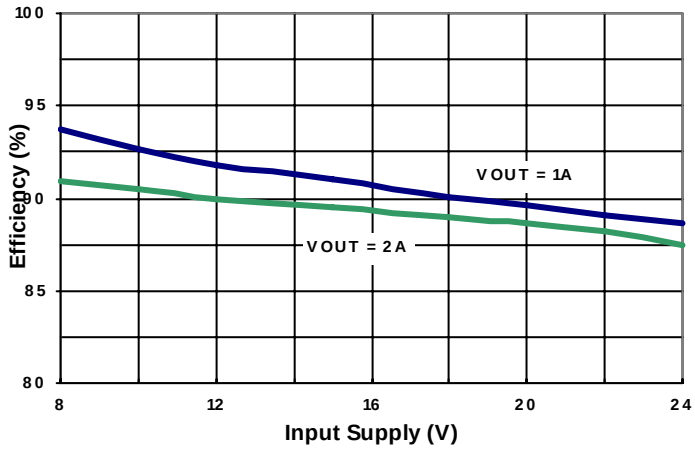
OCP CURRENT LIMIT VS INPUT SUPPLY



EFFICIENCY VS VOUT & IOUT



EFFICIENCY VS VIN & IOUT



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APPLICATION INFORMATION

SETTING THE OUTPUT VOLTAGE

To set the output voltage, connect a resistive divider from the output to the FB pin to signal ground. Note that the feedback voltage is 0.8V. For the desired output voltage VOUT, R2 is calculated by the following equation:

$$R2 = R1 \times \left(\frac{VOUT}{VFB} - 1 \right)$$

R1 is selected to be 10kΩ to 20kΩ and VFB=0.8V. Refer to Figure 2 or Figure 3.

OUTPUT INDUCTOR SELECTION

The value of inductor is decided by the input and output voltage, inductor ripple current and operating frequency. A larger inductor value means smaller ripple current. However if the inductance is chosen too large, it results in a slower response and possibly lower efficiency if the losses from the increased DCR outweigh the losses eliminated from a smaller ripple current. Likewise, a smaller inductor reduces the inductor size and cost, improves large signal response, but increases inductor ripple current which leads to lower efficiency and also an increase output ripple voltage. The magnitude of ripple current is a design freedom which can be decided by the design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L = \frac{(VIN - VOUT) \times VOUT}{VIN \times F_S \times k \times I_{LOAD}}$$

$$I_{RIPPLE} = k \times I_{LOAD}$$

The inductor ripple current can be calculated by:

$$I_{RIPPLE} = \frac{(VIN - VOUT) \times VOUT}{VIN \times F_S \times L}$$

Where F_S is the switching frequency (420kHz), I_{LOAD} is the output load current; k is percentage of output current.

A good design rule is to choose the inductor value such that k=0.3, which means that the inductor ripple current is 30% of the nominal output load current.

OUTPUT CAPACITOR SELECTION

The output capacitor value is basically decided by the amount of the output voltage ripple allowed during the steady state (DC) load condition as well as the load transient response requirement. The optimum design may require a couple of iterations to satisfy both conditions.

The output ripple voltage is due to the ESR of the output capacitor and the output capacitor charge and discharge. For aluminum electrolytic capacitors, the output ripple is largely caused by the capacitor ESR, where the output ripple is:

$$V_{RIPPLE} = ESR \times I_{RIPPLE}$$

However, if ceramic capacitors are used, the output ripple voltage is a combination of both the ESR and the capacitor charge and discharge, and can be approximated by:

$$V_{RIPPLE} = ESR \times I_{RIPPLE} + \left(\frac{I_{RIPPLE}}{8 \times C_{OUT} \times F_S} \right)$$

C_{OUT} is the output capacitance used, and F_S is the switching frequency.

The desirable output voltage change during a load transient dictates the output capacitance requirement. For a given output voltage change ΔVOUT, the output capacitance can be calculated by:

$$COUT = \frac{L \times \left(I_{LOAD} + \frac{\Delta I_{LOAD}}{2} \right)^2}{(\Delta VOUT + VOUT)^2 - VOUT^2}$$

Where ΔI_{LOAD} is the amount of change in the load current.

Based on the desired output ripple voltage and output voltage deviation during load transients, the output capacitance and its ESR can be approximated by the equations listed above.

INPUT CAPACITOR SELECTION

Input capacitors are usually a mix of high frequency ceramic capacitors and bulk capacitors. Ceramic capacitors bypass the high frequency noise, and bulk capacitors supply switching current to the MOSFET while keeping the DC input voltage steady. Usually a 1µF ceramic capacitor is chosen to decouple the high frequency noise. The bulk input capacitor is selected to support the input voltage rating and input RMS current rating, and can be a ceramic type.

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DEVICE POWER DISSIPATION

The LX3005 will enter thermal shutdown when the die temperature reaches close to 150˚C. The device junction temperature is a function of the device's total power dissipation, the junction to ambient thermal resistance, and the ambient temperature:

$$T_J = T_A + \left(P_{TOTAL} \times \theta_{JA}\right)$$

The total power dissipated by the LX3005 device, P_{TOTAL}, is comprised of the power dissipated by the RMS current flowing through the internal high-side FET, the switching or transitioning of the FET, and the power dissipated by the device quiescent supply current

The power dissipated due to the RMS input current flowing through the high side FET during the ON time is:

$$P_{RDSON} = I_{RMS} \times RDS_{ON}$$

$$IRMS = \sqrt{D\left(IOUT^2 + \frac{I_{RIPPLE}^2}{12}\right)}$$

The power dissipated during the switching or transition of the internal FET is:

$$P_{SW} = \frac{VIN \times IOUT \times (t_R + t_F)}{4} \times F_S$$

Where t_R and t_F are the rise and fall time of the switch node or the internal FET source node.

Finally, the power dissipated due to the device switching supply current is:

$$P_{IQ} = VIN \times IQ$$

where IQ, the device supply current when the device is switching, can be approximated by the device's supply quiescent current.

The total power dissipated by the device is therefore:

$$P_{TOTAL} = P_{RDSON} + P_{SW} + P_{IQ}$$

Based on the device total power dissipation, the ambient temperature, thermal resistance θ_{JA}, the device junction temperature can be determined.

COMPENSATION

The LX3005 uses external compensation components that allow for flexibility in designing the converter, since the compensation can be optimized after the output filter components (i.e. inductor and output capacitor) are selected for the required application. Normally for low cost applications, electrolytic capacitors that have high ESR are used. For applications where board space is critical, ceramics capacitors which have very low ESR are used.

The LX3005 incorporates a transconductance amplifier in its feedback control path. The inverting input to the amplifier is at the FB pin, and the output of the amplifier at the COMP pin. For compensating the device, a simple zero – pole pair can be used if the frequency of the zero created by the output capacitor and its ESR is lower than the chosen unity gain cross-over frequency F_C. This is known as Type II compensation. See Figure 2. If the zero of the output capacitor is located above the cross-over frequency F_C, as with ceramic capacitors that have very low ESR, use a 2 zero 2 pole compensation, or a Type III compensation network. For the LX3005, set the cross-over frequency to be approximately 20kHz to 40kHz.

TYPE II COMPENSATION

If the output capacitor zero is located below the cross-over frequency, use the following procedure for Type II compensation. The following is an explanation of how to design a TYPE II compensation network for the LX3005 converter:

Estimate the LC output filter double pole and zero:

$$f_{LC} = \frac{1}{2\pi\sqrt{L \times COUT}}$$

$$f_{ZESR} = \frac{1}{2\pi \times ESR \times COUT}$$

Next, select the cross-over frequency of the closed loop bandwidth to be 40kHz or below.

In order for the overall closed loop bandwidth to cross over at the desired frequency F_C, the gain of the error or transconductance amplifier should be adjusted such that at the cross-over frequency F_C, the product of the error amplifier gain and the gain of the feed-forward modulator path equals to 1. The feed-forward modulator gain consists of the internal PWM modulator gain, the LC output filter response, and the external resistive divider gain. This feed-forward modulator response can be approximated by the following equation:

APPLICATION INFORMATION

$$G_{MOD} = \frac{VIN}{V_{RAMP}} \times \frac{VFB}{VOUT} \times \left(\frac{ESR}{2\pi \times F_C \times L}\right)$$

The gain of the transconductance amplifier near the cross over frequency is:

$$G_{EA} = gm \times R_C$$

The product of the modulator gain and error amplifier gain should equal to 1 at the cross-over frequency. Thus, $G_{MOD}xG_{EA} = 1$ and solve for R_C.

$$R_C = \frac{V_{RAMP} \times VOUT \times 2\pi \times F_C \times L}{gm \times VIN \times VFB \times ESR}$$, where $V_{RAMP} \approx 1.2V$.

Type II compensation places a zero at or below the frequency of the LC double pole, and a high frequency pole at ½ the switching frequency or lower. The zero is created by R_C and C_C while the pole is from R_C and $C_{OPTIONAL}$. See Figure 2.

Where $f_Z = \frac{1}{2\pi \times R_C \times C_C}$ and $fp = \frac{1}{2\pi \times R_C \times C_{OPT}}$

Based on the calculated R_C value, we can solve for C_C such that the zero is placed at or below the double pole frequency.

$$f_{LC} \geq \frac{1}{2\pi \times C_C \times R_C} = f_Z$$, with R_C and f_{LC}, solve for C_C

Place a pole at high frequency at or below ½ the switch frequency, and solve for C_{OPT}.

$$\frac{1}{2} \times F_S \geq \frac{1}{2\pi \times C_{OPT} \times R_C} = f_P$$

Note that the high frequency pole is optional. The purpose of the high frequency pole is to close or attenuate the overall loop response rejecting high frequency noise. If the high frequency pole is not used, the overall loop at high frequency will be determined by the high frequency response of the error amplifier.

A good rule of thumb in terms of placing the zero-pole pair for approximately 60 degrees phase margin is to satisfy the following condition:

$$\frac{F_C}{f_Z} = \frac{f_P}{F_C} = 5$$

However, while satisfying this condition, it is important that the zero is placed at or below the double frequency pole to ensure stability.

TYPE III COMPENSATION

When using low ESR ceramic output capacitors, the frequency of the zero produced by the output capacitor is usually above the cross-over frequency. In this case Type III compensation should be used. In traditional Type III compensation, two zeros and two poles, in addition to the pole at the origin, are introduced by the error amplifier, and the overall amplifier response is set via a feedback network from the COMP output to the non-inverting input FB.

A cost effective method minimizing the number of compensation components is to directly place a second zero f_{Z2}, at the frequency of the double pole. This zero is created by R2 and C1 as shown in Figure 2.

$f_{LC} = \frac{1}{2\pi \times C_1 \times R_2}$ and solve for C_1. Note that in this case, the second zero is added by C_1 and R_2 in addition to the zero already introduced by R_C and C_C and also the pole from R_C and C_{OPT} as defined in Type II compensation.

GENERAL LAYOUT GUIDELINES

The following are general but good practices for PCB layout to prevent noise related issues, and achieve stable operation of the converter:

1) Place all filtering capacitors as close to the IC as possible. Use a power ground plane for the input (C_{IN}) and output (C_{OUT}) capacitors. All other capacitors such as for compensation should use signal ground.
2) While having separate power ground and signal ground planes, the two grounds should be connected at one common point near the input bypass capacitor ground.
3) Make high current traces short and wide. This includes the input current path and the inductor current path. Minimize the loop path that consist of the switch node (SW), the output filter components, and the input capacitor.
4) Keep the switch node (SW), which is noisy, away from sensitive analog paths to prevent noise coupling onto sensitive signals such as at FB and COMP pins.
5) Place all compensation components and feedback resistors as close to the IC as possible, minimizing trace lengths.

Note that a LX3005 evaluation board or demo board is available. Please contact the factory for availability.

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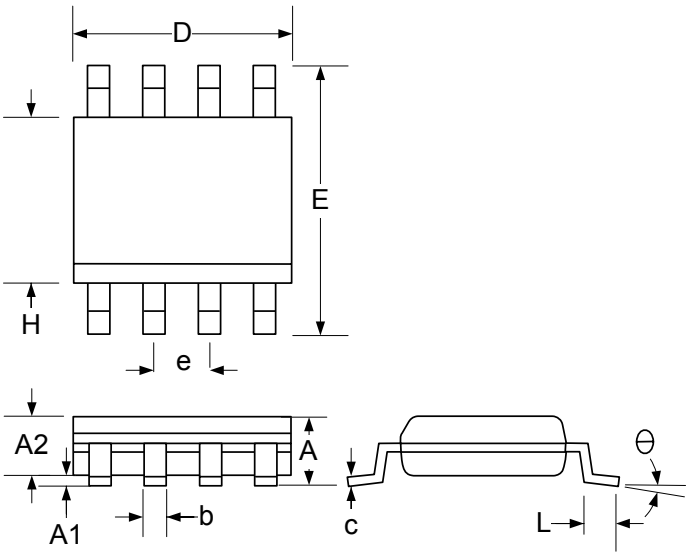
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 800-8776458, 714-898-8121, Fax: 714-893-2570

PACKAGE DIMENSIONS

DM 8-Pin Plastic SOIC



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A1	0.10	0.30	0.004	0.012
A2	1.25	1.45	0.049	0.057
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.007	0.010
D	4.70	5.10	0.185	0.201
E	5.79	6.20	0.228	0.244
e	1.27 BSC		0.050 BSC	
H	3.80	4.01	0.150	0.158
L	0.40	1.27	0.016	0.050
θ	0	8	0	8
*LC		.010		0.004

*Lead Coplanarity

Note:

1. Controlled dimensions are in mm, inches are for reference only.
2. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.