Superior Multi-touch Capacitive Touch Screen Controller AP386X

General Description

The AP386X is a low-cost high-resolution single chip solution for APA (All point addressable) capacitive touch screen. It is an 8-bit single cycle 8051 microcontroller with ICP Interface. The chip includes 12-bit successive approximation analog-to-digital converters with an I^2C interface and multiplexer-switcher circuits for flexible measurement of analog signal from APA panel. An accurate switched-capacitor integrator is built-in and it can auto calibrate the pixel parameters for a wide range of capacitance on the touch screen (1pF to 32pF). This touch screen controller (TSC) with CMOS integration circuit provides an ideal choice for APA touch panel. The AP386X is specified over the temperature range of -40°C to 85°C.

The AP386X is available in QFN-5×5-40 (for AP3860) and QFN-6×6-48 (for AP3861) packages.

Features

- Mutual Capacitive Touch Sensing
- Single Power Supply: 2.8V to 3.6V Operation Voltage; LDO inside to Support 1.6V to 2.0V Operation Voltage
- Up to 17/23 Drive Lines and 10/12 Sense Lines
- Charge Pump Support up to 6V, Doubling SNR
- Internal Two-wire Serial Control Bus I^2C
- Single-end Integrator with Programmable Gain Control
- Multiplexed Analog Digitization with 12-bit Resolution Scan SAR ADCs and Its Dedicated 2X to 8X Accumulator XSRAM Buffers

Features (Continued)

- Single Cycle 8051 CPU Core, Maximum Operating Clock up to 28MHz from IOSC (Zero Wait State)
  4 to 28MHz Internal Oscillator (IOSC)
  32k-byte Flash ROM
  6k-byte Internal SRAM
  Two 16-bit Timers T0/T1
  Configurable I^2C Slave Controller and SPI Slave Controller Shared with the Same Ports
  - With Asynchronous I^2C Slave Address Detection Logic Design

  4 General Purpose GPIO Pins
  One External Interrupt Pin
- ISP/IAP via I²C Port
- Operation Temperature Range: -40°C to 85°C
- Package Type Alternatives: QFN-5×5-40 and QFN-6×6-48
- RoHS Compliance
- Operating Mode:

Mode	Description
Power-down	No scan with power-down mode
Idle	While only 8051 CPU core is idle, all peripherals remain active
Standard	Higher scan rate when fingers are on panel, IOSC can up to 4MHz to 28MHz

Applications

- Mobile Phones
- Personal Digital Assistants
- Smart Hand-held or Gaming Devices

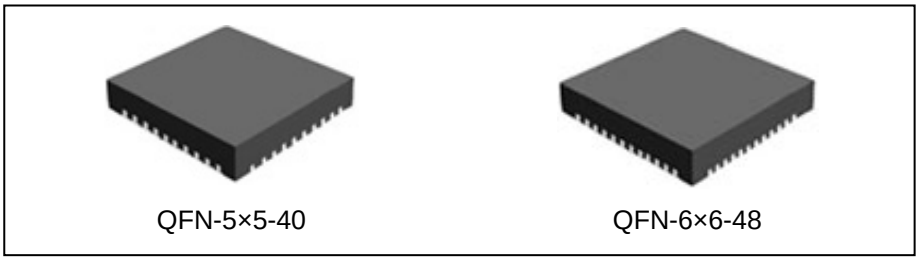


Figure 1. Package Types of AP386X

Pin Configuration

FN Package
(QFN-5×5-40)

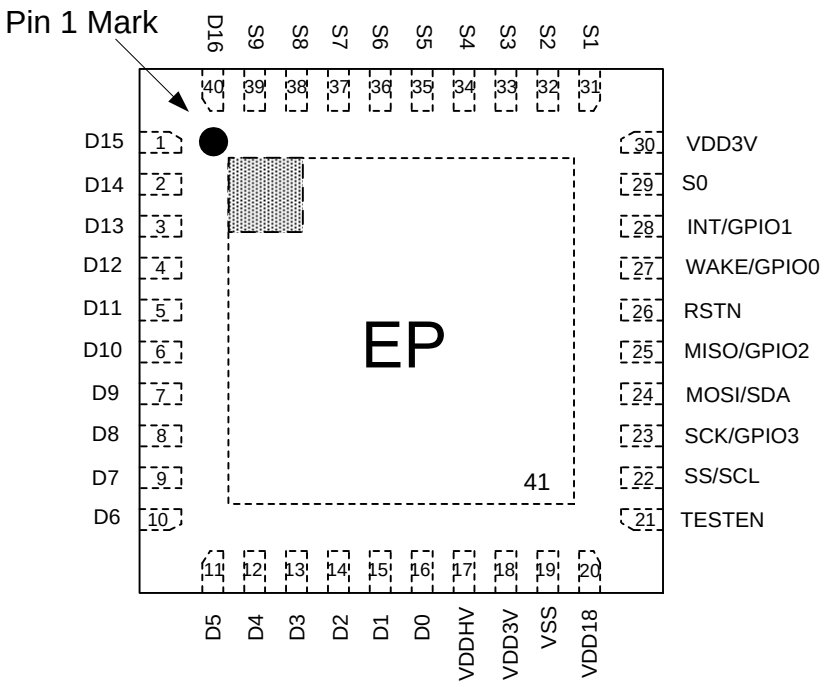


Figure 2. Pin Configuration of AP3860 (Top View)

Pin Configuration (Continued)

FN Package
(QFN-6×6-48)

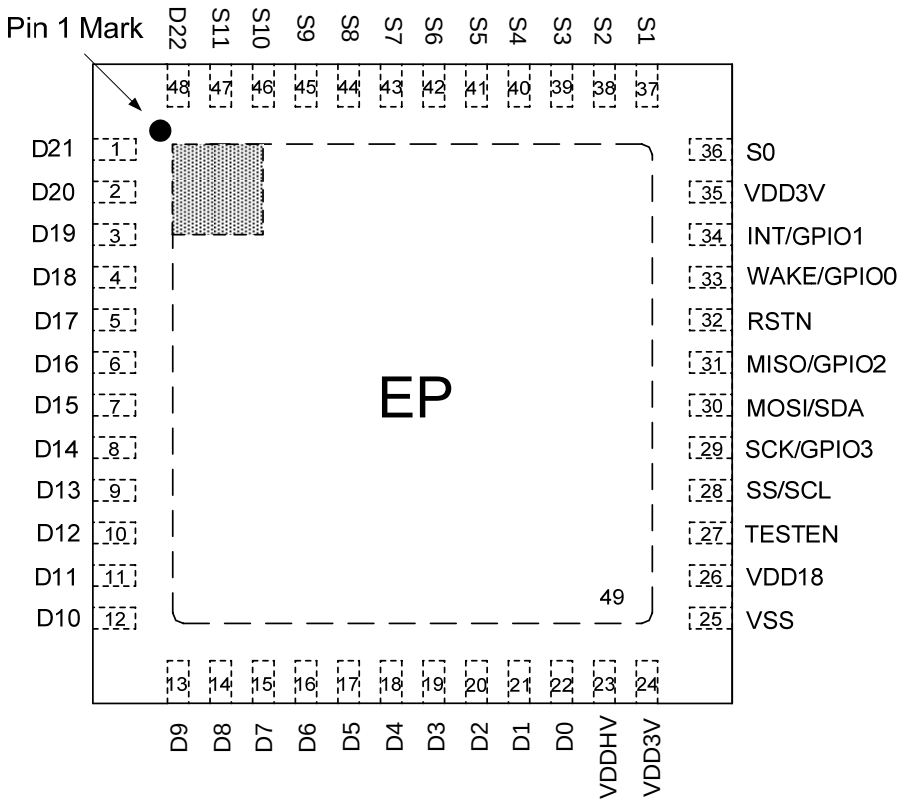


Figure 3. Pin Configuration of AP3861 (Top View)

Pin Description

Pin Number		Pin Name	Pin Type	Pin Function
QFN-5×5-40 AP3860	QFN-6×6-48 AP3861			
40, 1 to 16	6 to 22	D16 to D0	I/O, A	**Driving Lines 16 to 0** These pins can also be configured as I/O bi-directional ports for test
-	48, 1 to 5	D22 to D17	I/O, A	**Driving Lines 22 to 17** These pins can also be configured as I/O bi-directional ports for test
17	23	VDDHV	O	**High Voltage. 6V** Charge pump high Voltage. This output pin can be configured as VDD3V or 6V accordingly
18, 30	24, 35	VDD3V	P	**Supply Voltage. 2.8V to 3.6V** A good decoupling capacitor between VDD3V and VSS pins is critical for good performance
19	25	VSS	P	**Ground Voltage. 0V**
20	26	VDD18	O	**Internal Regulator Output. 1.6V to 2.0V** Typical decoupling capacitors of 0.1μF and 10μF should be connected between VDD18 and VSS
21	27	TESTEN	I	**Test Mode Enable High Active** This pin has an internal weakly pull low resistor connected. If it is connected high, the chip enters into Test Mode condition
22	28	SS/SCL	I/O	**SS/SCL** This pin can be configured as the SCL signal of the I^2C master or I^2C slave controller. When I^2C is enabled, the pin is configured as an open-collector. While in SPI mode, this pin is configured as the slave chip select pin
23	29	SCK/ GPIO3	I/O	**Port 1.3 GPIO** 8051 P1.3 GPIO. This pin can also be configured as the serial clock from SPI master while SPI interface is activated
24	30	MOSI/ SDA	I/O	**SDA** This pin can be configured as the SDA signal of the I^2C master or I^2C slave controller. In this operation mode, this pin should also be configured as open-collector. While SPI interface is selected, the pin serves as the data port from SPI master to SPI slave
25	31	MISO/ GPIO2	I/O	**Port 1.2 GPIO** 8051 P1.2 GPIO. This pin can also be configured as the output data pin from slave to master for SPI interface

Pin Description (Continued)

Pin Number		Pin Name	Pin Type	Pin Function
QFN-5×5-40 AP3860	QFN-6×6-48 AP3861			
26	32	RSTN	I	**Reset Low Active** Typically connect a resistor to VDD3V and a capacitor to VSS. Low asserted and threshold at 0.5*V_{DD}. When forced low, the chip enters into reset condition. This pin should not be connected to any level above V_{DD}
27	33	WAKE/ GPIO0	I/O	**Port 1.0 GPIO** 8051 P1.0 GPIO. This pin can also be configured as the wakeup pin from the host
28	34	INT/ GPIO1	I/O	**Port 1.1 GPIO** 8051 P1.1 GPIO. Open Drain output. This pin can also be configured as the interrupt pin to notify the host
29, 31 to 39	36 to 45	S0 to S9	I/O, A	**Sensing Lines 0 to 9** These pins can also be configured as I/O bi-directional ports for test
-	46, 47	S10, S11	I/O, A	**Sensing Lines 10 to 11** These pins can also be configured as I/O bi-directional ports for test
41	49	EP		**Exposed Pad**

"I/O" means input/output; "I" means input; "O" means Output; "P" means power; "A" means analog.

SCL and SDA Pin Description

Pull-up Enable

The pull-up enable for SCL and SDA is activated for AP386X, meaning that AP386X always has pull-up SCL and SDA to VDD3V. During reset, SCL and SDA are as input pin. Moreover, if the pin connecting to the system is floating, the internal pull-up will tie the pin to VDD3V (10kΩ). After AP386X is reset, SCL and SDA are input until its corresponding register is configured.

Mode Selection

SCL and SDA can be used in I^2C and SPI mode. AP386X can enable I^2C mode (SCL and SDA configured as open drain pin) by register setting.

Wakeup

SCL and SDA can be used for wakeup input signals in different mode. While I^2C mode is enabled, a START protocol (SDA is low and SCL is high) on SCL and SDA is a wakeup signal to AP386X. While SPI mode is enabled, an active low on the pin of SCL (serving as a slave select in SPI) is a wakeup signal to AP386X. Moreover, a wakeup signal can be asserted by host from GPIO0.

INT/GPIO1

GPIO1 can be configured as open-drain or push-pull mode. Furthermore, GPIO1 pin has internal pull-up to VDD3V (60kΩ) or VDD18 (10kΩ) based on different register definition.

Functional Block Diagram

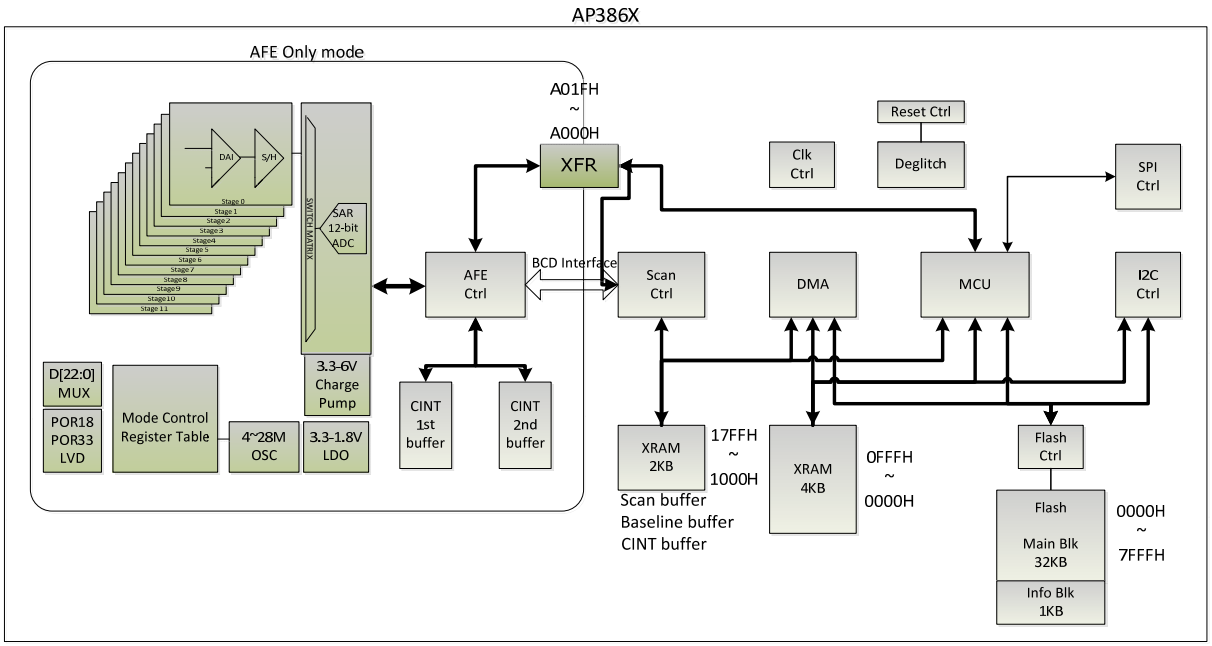
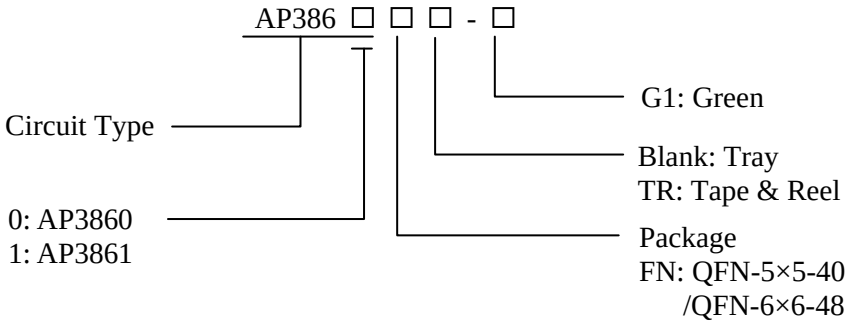


Figure 4. Functional Block Diagram of AP386X

Ordering Information



Package	Temperature Range	Part Number	Marking ID	Packing Type
QFN-5x5-40	-40 to 85°C	AP3860FNTR-G1	3860FN	Tape & Reel
QFN-6x6-48		AP3861FN-G1	3861FN	Tray
		AP3861FNTR-G1	3861FN	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "G1" in the part number, are RoHS compliant and green.

AP386X Support 3” to 8” Touch Panel, Listed Below:

PN	TX/RX	Multi-touch	Package	Panel size
AP3860	17/10	10 points 100Hz	QFN-5x5-40	3” to 7”
AP3861	23/12	10 points 100Hz	QFN-6x6-48	4” to 8”

Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Value	Unit
Supply Voltage (Pin VDD3V)	V_{DD}	0 to 4	V
Analog Input Voltage (Other pins)		-0.3 to V_{DD}+0.3	V
Logic Input Voltage		-0.3 to V_{DD}+0.3	V
Thermal Resistance (Simulation, Junction to Ambient)	θ_{JA}	TBD	°C/W
Maximum Junction Temperature	T_J	100	°C
Operating Temperature	T_{OP}	-40 to 85	°C
Storage Temperature	T_{STG}	-65 to 150	°C
ESD (Human Body Model)	ESD HBM	8000	V

Note 1: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Pin VDD3V)	V_{DD}	2.8	3.6	V
Operating Ambient Temperature	T_A	-40	85	°C

Electrical Characteristics

T_A=25°C, V_{DD}=2.8V to 3.6V, I^2C bus frequency=400kHz, 12-bit mode, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Quiescent Current		Standard mode f_{OSC}=4 to 28MHz Power-down mode Idle mode		5 60	 1 	mA μA μA
VDD18 Output Voltage	V_{DD18}		1.6	1.8	2.0	V
Charge Pump Voltage	V_{DDHV}	Charge pump enable	5.8	6	6.3	V
Internal Operating Frequency	f_{OSC}		4		28	MHz

DA/AC Characteristics for AFE

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ADC DC Accuracy						
Resolution					12	Bits
No Missing Codes		Standard modes	11	12		Bits
Integral Linearity Error	INL	Standard modes		±3		LSB
Differential Linearity Error Offset Error Gain Error	DNL			±1.5	 ±6 ±4	LSB LSB LSB
Analog Input						
Full-scale Input Span			0		V_{DD}	V
ADC Sampling Dynamics						
Throughput Rate				500		ksps
Switched-capacitor Integrator						
Output Voltage Range			0.3		V_{DD}-0.3	V
Integrator Capacitor	C_{INT}			40		pF

Electrical Characteristics (Continued)

DA/AC Characteristics for 8051 CPU Core, Digital GPIO Pins, Digital Peripherals

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
RSTN Input Voltage Threshold	V_{RSTN_H}	Low to high level	1.56		1.71	V
	V_{RSTN_L}	High to low level	1.16		1.30	
Input High Voltage	V_{IH}		0.7*V_{DD}		V_{DD}	V
Input Low Voltage	V_{IL}		-0.3		0.5	V
Output High Voltage	V_{OH}		V_{DD}-0.6			V
Output Low Voltage	V_{OL}				0.4	V
High Level Output Current	I_{OH}	@V_{OH}(Min)		1		mA
Low Level Output Current	I_{OL}	@V_{OL}(Max)		1		mA
Internal Pull-up Resistance	R_{PU}	SCL, SDA, INT		10		kΩ
		Other Pins	34		74	
Internal Pull-down Resistance	R_{PD}		29		86	kΩ
Output Rise Time	t_{RISE}	C_{LOAD}=20pF and 10% to 90%		5		ns
Output Fall Time	t_{FALL}	C_{LOAD}=20pF and 10% to 90%		5		ns
GPIO Output Operating Frequency		C_{LOAD} =20pF	0		5	MHz
SCK Frequency	f_{SCK}				2	MHz
SCL Clock Frequency	f_{SCLI2C}		0		400	kHz

Typical Application

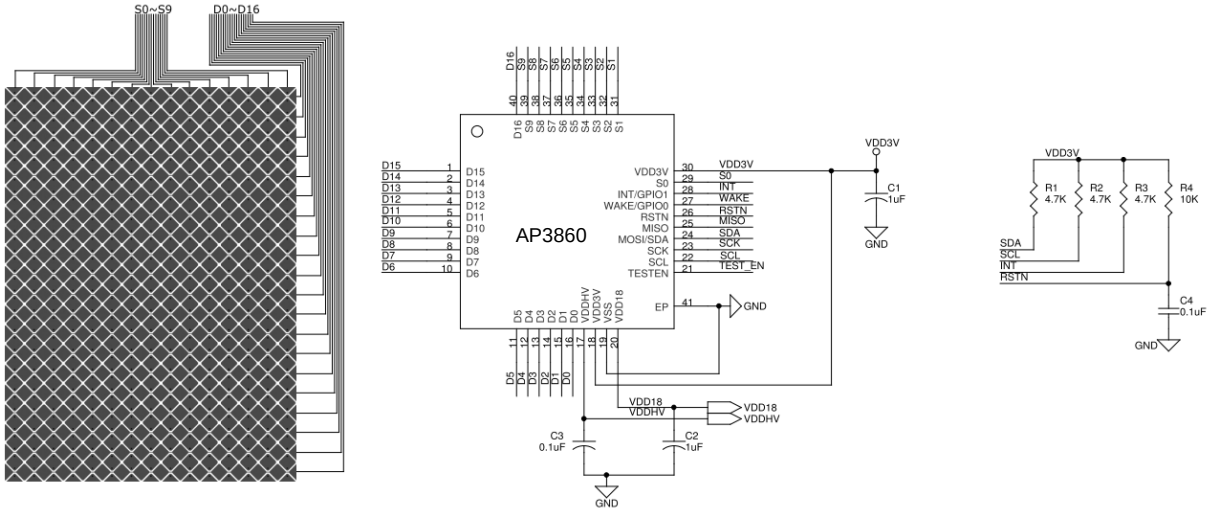


Figure 5. Typical Application Schematic of AP3860 (For QFN-5×5-40 Package)

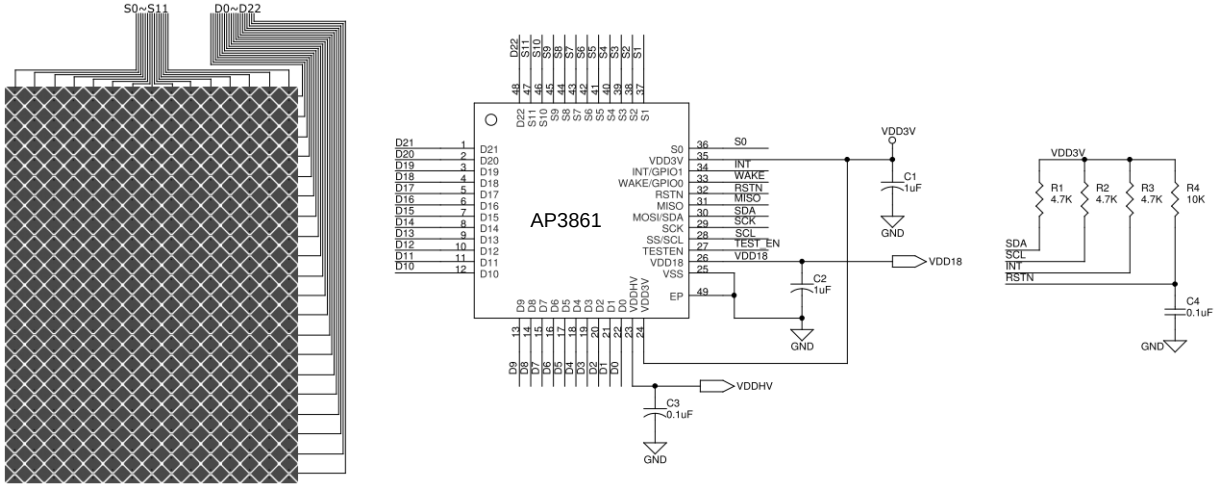
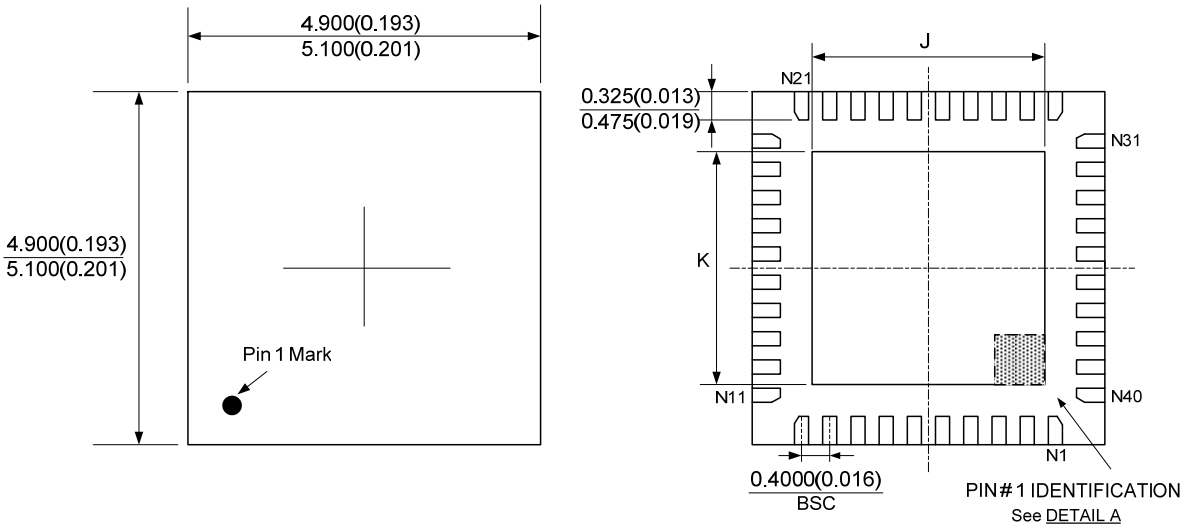


Figure 6. Typical Application Schematic of AP3861 (For QFN-6×6-48 Package)

Mechanical Dimensions

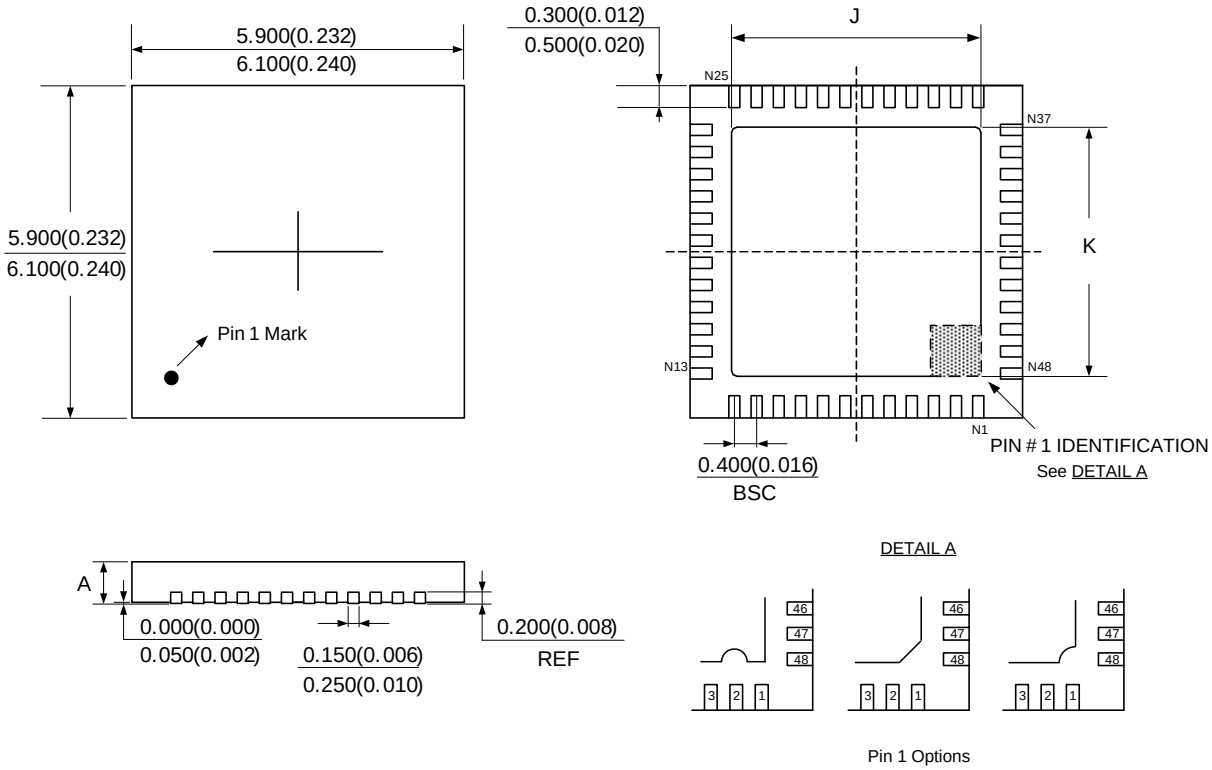
QFN-5×5-40 **Unit: mm(inch)**



Symbol	J=K			
	min(mm)	max(mm)	min(inch)	max(inch)
Option1	3.200	3.400	0.126	0.134
Option2	3.300	3.500	0.130	0.138
Option3	3.600	3.800	0.142	0.150

Mechanical Dimensions (Continued)

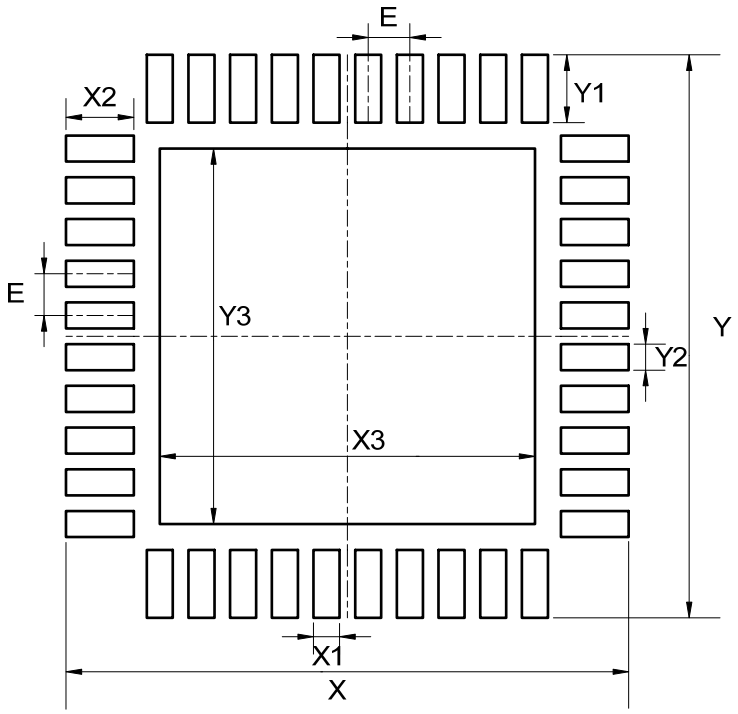
QFN-6×6-48 **Unit: mm(inch)**



Symbol	J=K				A			
	min(mm)	max(mm)	min(inch)	max(inch)	min(mm)	max(mm)	min(inch)	max(inch)
Option1	4.400	4.600	0.173	0.181	0.700	0.800	0.028	0.031
Option2	4.150	4.450	0.163	0.175	0.800	0.900	0.031	0.035

Mounting Pad Layout

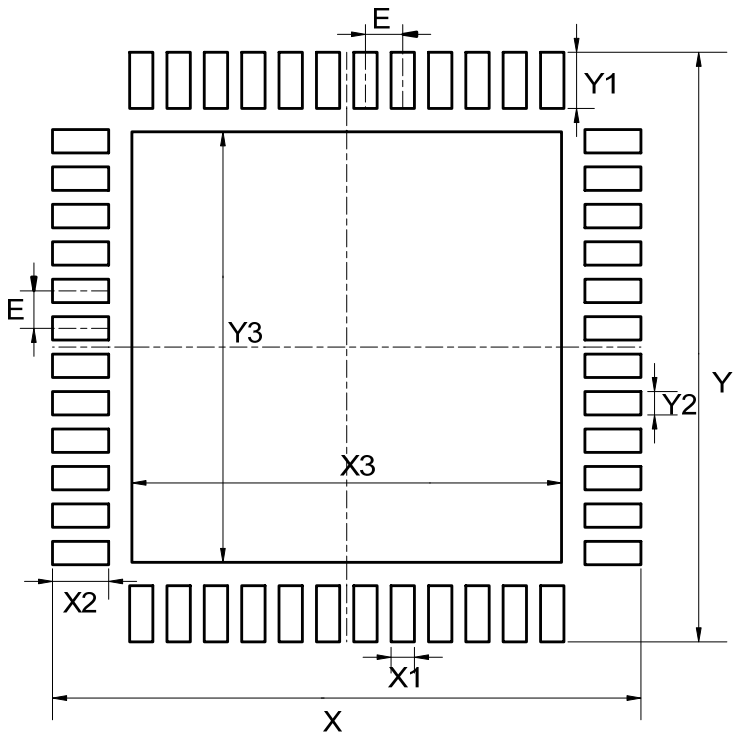
QFN-5×5-40



Dimensions	X=Y (mm)/(inch)	X1=Y2 (mm)/(inch)	Y1=X2 (mm)/(inch)	X3=Y3 (mm)/(inch)	E (mm)/(inch)
Option1	5.400/0.213	0.250/0.010	0.650/0.026	3.500/0.138	0.400/0.016
Option2	5.400/0.213	0.250/0.010	0.650/0.026	3.600/0.142	0.400/0.016
Option3	5.400/0.213	0.250/0.010	0.650/0.026	3.800/0.150	0.400/0.016

Mounting Pad Layout (Continued)

QFN-6×6-48



Dimensions	X=Y (mm)/(inch)	X1=Y2 (mm)/(inch)	Y1=X2 (mm)/(inch)	X3=Y3 (mm)/(inch)	E (mm)/(inch)
Value	6.300/0.248	0.250/0.010	0.600/0.024	4.600/0.181	0.400/0.016

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