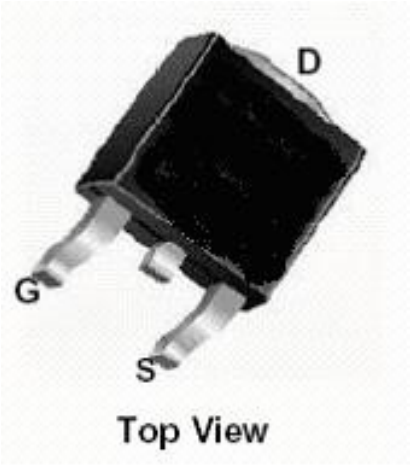
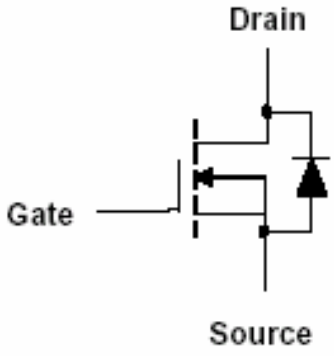
# FMDS55N25 25V N-Channel Enhancement-Mode MOSFET




Top View

**TO-252 (D-PAK)**

Internal Schematic Diagram




**N-Channel MOSFET**

## Features

Advanced trench process technology
High Density Cell Design For Ultra Low On-Resistance
Specially Designed for DC/DC Converters and Motor Drivers
Fully Characterized Avalanche Voltage and Current
Improved Shoot-Through FOM

**$V_{DS}$= 25V**
**$R_{DS(ON),}$ $V_{gs@10V}$, $I_{d@30A}$ = 6mW**
**$R_{DS(ON),}$ $V_{gs@4.5V,}$ $I_{d@30A}$ = 9mW**

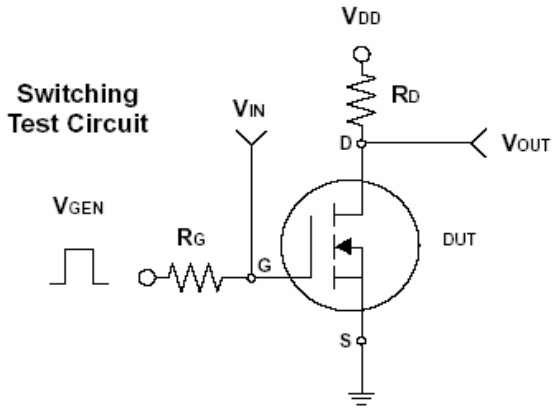
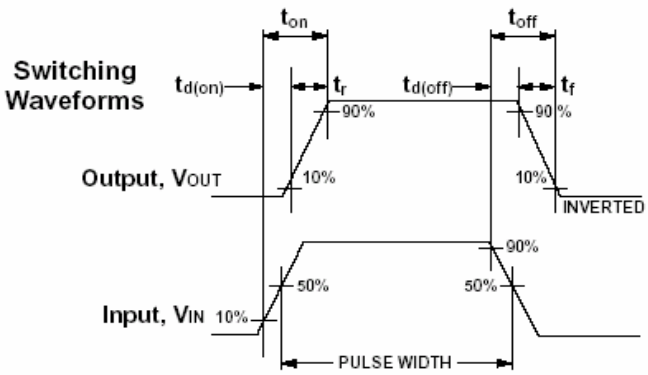
## Maximum Ratings and Thermal Characteristics ($T_A$ = 25°C unless otherwise noted)

| Parameter | | Symbol | Limit | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 25 | V |
| Gate-Source Voltage | | $V_{GS}$ | ± 20 | |
| Continuous Drain Current | | $I_D$ | 55 | A |
| Pulsed Drain Current | | $I_{DM}$ | 350 | |
| Maximum Power Dissipation | $T_A$ = 25°C | $P_D$ | 70 | W |
| | $T_A$ = 75°C | | 42 | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | -55 to 150 | °C |
| Avalanche Energy with Single Pulse<br>$I_D$=50A, $V_{DD}$=25V, L=0.5mH | | $E_{AS}$ | 300 | mJ |
| Junction-to-Case Thermal Resistance | | $R_{\theta JC}$ | 1.8 | °C/W |
| Junction-to-Ambient Thermal Resistance (PCB mounted) | | $R_{\theta JA}$ | 40 | |

Note: 1. Maximum DC current limited by the package
2. 1-in 2oz Cu PCB board

# FMDS55N25 25V N-Channel Enhancement-Mode

## ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$ = 0V, $I_D$ = 250uA | 25 | - | - | V |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 4.5V, $I_D$ = 30A | | 7.5 | 9.0 | mΩ |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10V, $I_D$ = 30A | | 4.5 | 6.0 | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ =$V_{GS}$, $I_D$ = 250uA | 1 | 1.6 | 3 | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 25V, $V_{GS}$ = 0V | | | 1 | uA |
| Gate Body Leakage | $I_{GSS}$ | $V_{GS}$ = ±20V, $V_{DS}$ = 0V | | | ± 100 | nA |
| Gate Resistance | Rg | | | | | |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 15V, $I_D$ = 15A | | | | S |
| **Dynamic** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 15V, $I_D$ = 25A<br>$V_{GS}$ = 10V | | 26 | | |
| Gate-Source Charge | $Q_{gs}$ | | | 6 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 5 | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 15V, $R_L$ = 15Ω<br>$I_D$ = 1A, $V_{GEN}$ = 10V<br>$R_G$ = 6Ω | | 17 | | ns |
| Turn-On Rise Time | $t_r$ | | | 3.5 | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 40 | | |
| Turn-Off Fall Time | $t_f$ | | | 6 | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 15V, $V_{GS}$ = 0V<br>f = 1.0 MHz | | 2134 | | pF |
| Output Capacitance | $C_{oss}$ | | | 343 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 134 | | |
| **Source-Drain Diode** | | | | | | |
| Max. Diode Forward Current | $I_S$ | | | | 20 | A |
| Diode Forward Voltage | $V_{SD}$ | $I_S$ = 20A, $V_{GS}$ = 0V | | 0.85 | 1.3 | V |

**Note**: Pulse test: pulse width <= 300us, duty cycle<= 2%