# 3/2/1+2/1-Phase Driver Embedded PWM Controller for IMVP8

General Description

The uP9507 is an IMVP8 compliant desktop CPU voltage regulator controller that integrates a 3-phase PWM controller for Vcore and a 2-phase controller for VccGT. The Vcore controller can be configured as 3/2/1-phase, and the VccGT controller can be configured as 2/1-phase for platform power design flexibility. This part integrates 3 bootstrap diode embedded 12V MOSFET drivers. For the typical 3+2-phase application, the 3-phase Vcore controller has one embedded MOSFET driver and two PWM outputs. The 2-phase VccGT controller has 2 embedded MOSFET drivers.

The uP9507 combines true differential output voltage sense, differential inductor DCR current sense, input voltage feed-forward sense and adaptive voltage positioning to provide accurately regulated power for desktop CPU. It adopts uPIs proprietary RCOT+™ (Robust Constant On-Time) topology to have fast transient response and smooth mode transition.

The uP9507 provides VR_RDY indicator and selectable VR parameters, such as SVID VR address and Vboot voltage. It also provides complete fault protection functions, including over voltage, under voltage, over current, over temperature and under voltage lockout. The uP9507 is available in VQFN7x7 - 60L package.

Pin Configuration
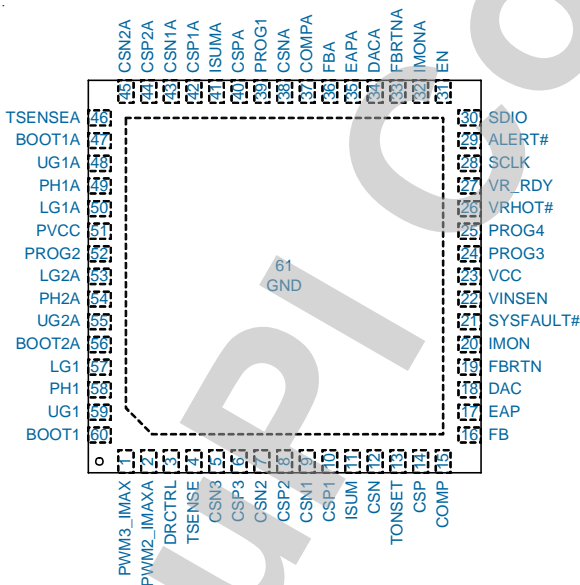
Features

- **Intel IMVP8 Compatible**
  - **Support S-Line Desktop CPU**
  - **Thermal Sense with VRHOT# Indication**
- **RCOT+™ Control Topology**
  - **Easy Setting**
  - **Smooth Mode Transition**
  - **Fast Transition Response**
- **3 Integrated 12V MOSFET Drivers**
  - **Embedded Bootstrap Diode**
  - **3+2 Phase: 1 driver for Vcore, 2 drivers for VccGT**
- **External MOSFET Driver Enable Control**
- **Support Operation Phase Disable Function**
  - **Vcore: 3/2/1-Phase**
  - **VccGT: 2/1-Phase**
- **Build-in ADC for Platform Parameter Setting**
  - **Selectable SVID VR Address**
  - **Selectable Vboot Voltage**
- **Enable Control and VR_RDY Indicator**
- **System Thermal Management**
- **Differential Remote Voltage Sense**
- **Differential Current Balance Sense Amplifier**
- **OCP/OVP/UVP/Thermal Shutdown**
- **RoHS Compliant and Halogen Free**

Applications

- **Desktop PC CPU Power Supplies**

Ordering Information

Order Number	Package	Remark
uP9507PQGZ	VQFN7x7 - 60L	

Note:

(1) Please check the sample/production availability with uPI representatives.

(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.
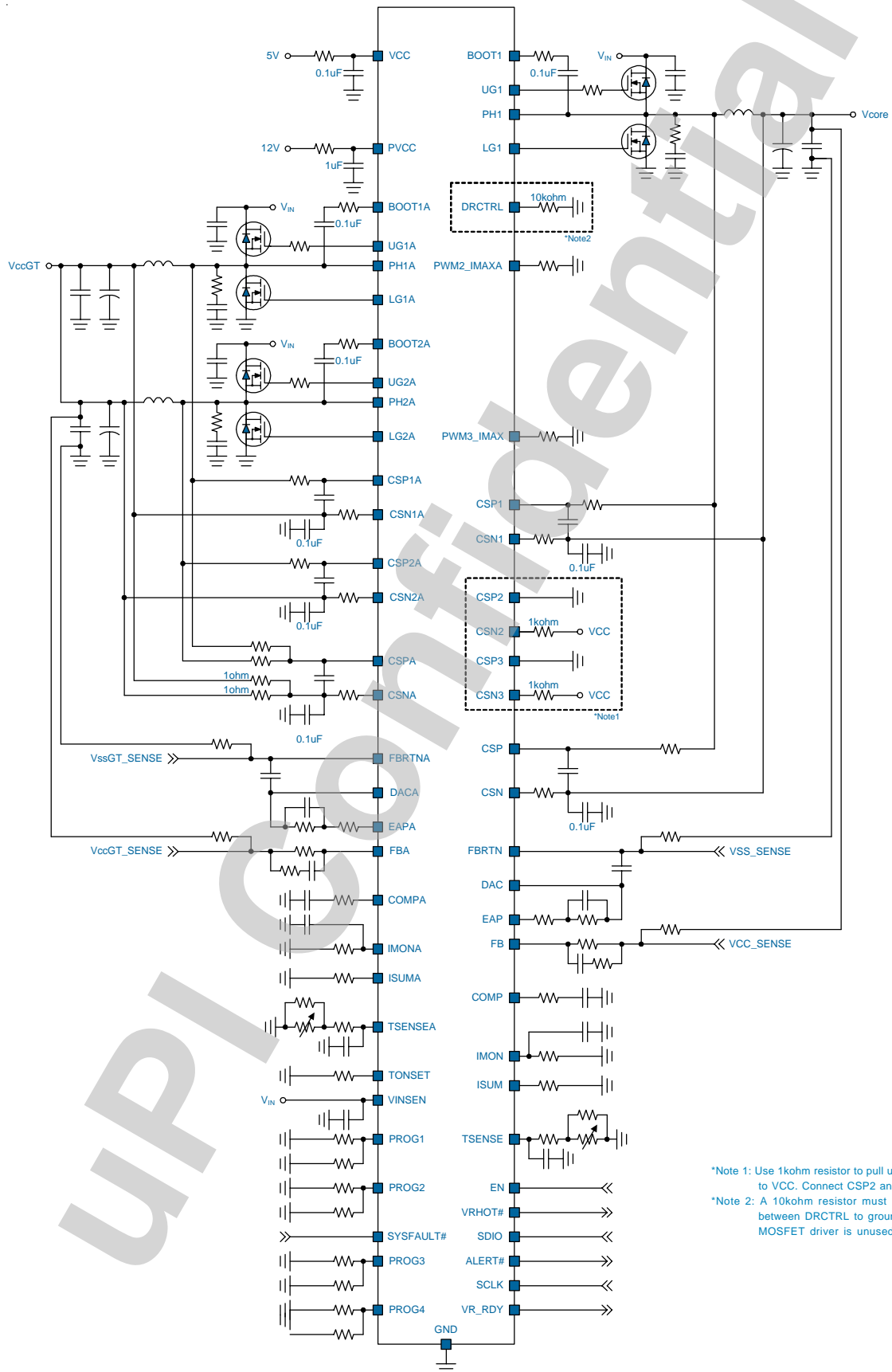
Typical Application Circuit

3+2 Phase
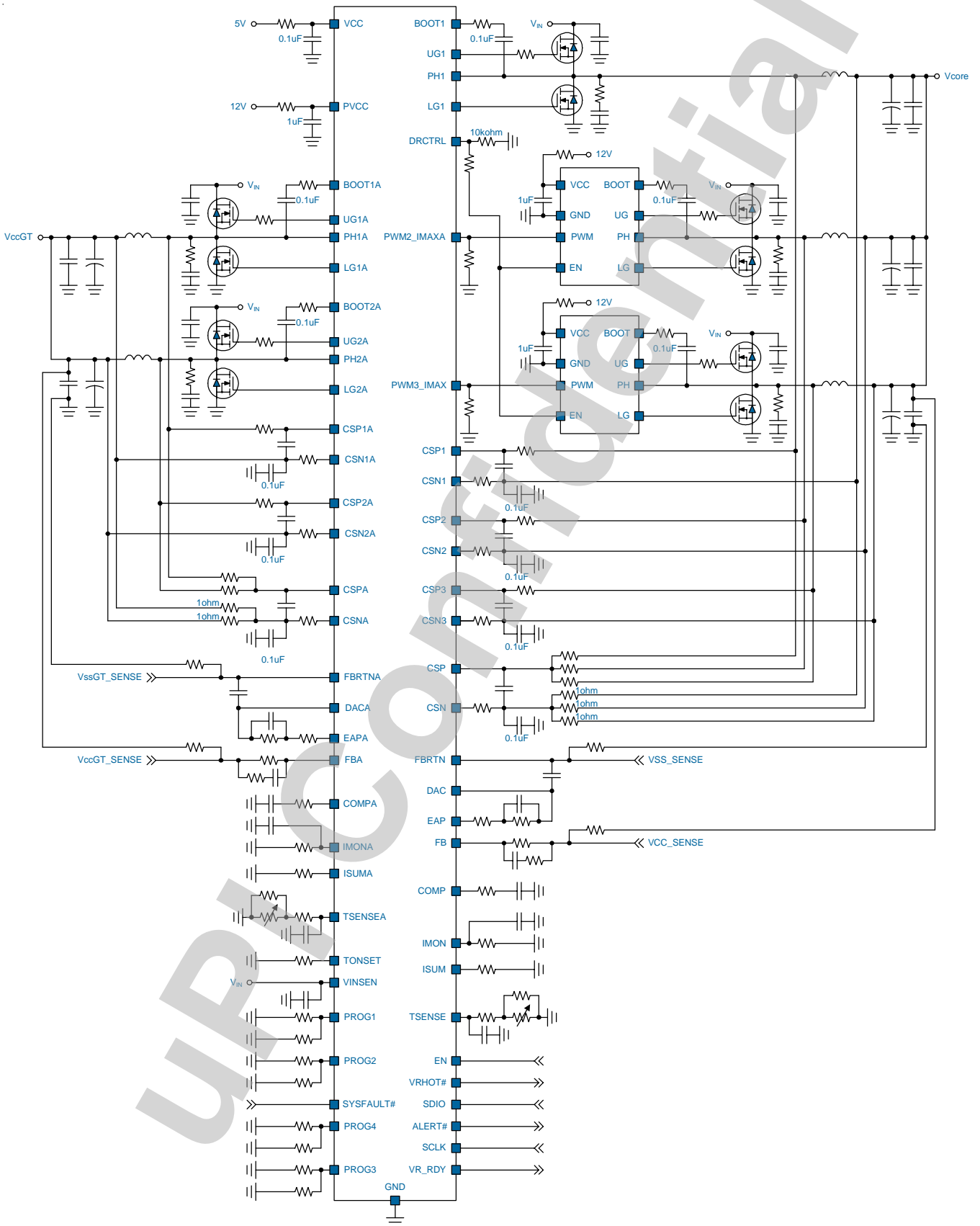
Typical Application Circuit

1+2 Phase

*Note 1: Use 1kohm resistor to pull up CSN2 and CSN3 to VCC. Connect CSP2 and CSP3 to ground.
*Note 2: A 10kohm resistor must still be connected between DRCTRL to ground even if external MOSFET driver is unused.

No.	Name	Pin Function
1	PWM3_IMAX	This pin is a multi-functional pin. It outputs a PWM logic signal for external discrete MOSFET driver for Vcore rail and it is also used to set the Vcore SVID register content. **Phase 3 PWM Output.** Connect this pin to the PWM input of external MOSFET driver. **IMAX Setting Input for Vcore.** Connect a resistor from this pin to GND to set the SVID IccMAX register (0x21h) value for Vcore rail.
2	PWM2_IMAXA	This pin is a multi-functional pin. It outputs a PWM logic signal for external discrete MOSFET driver for Vcore rail and it is also used to set the VccGT SVID register content. **Phase 2 PWM Output.** Connect this pin to PWM input of external MOSFET driver. **IMAXA Setting Input for VccGT.** Connect a resistor from this pin to GND to set the SVID IccMAX register (0x21h) value for VccGT rail.
3	DRCTRL	**MOSFET Driver Enable Control Output.** This pin is a multi-functional pin. It is used to enable/disable all external discrete MOSFET drivers. Connect a 10kΩ resistor from this pin to ground and place this resistor close to the controller. Do not use any other resistance value. Do not connect any capacitor directly to this pin. PCB trace routing of this pin has special consideration. Refer to the related section in Application Information for detail.
4	TSENSE	**Thermal Monitoring Input for Vcore.** Connect a specified negative temperature coefficient (NTC) thermistor network from this pin to GND for Vcore VR temperature sensing. Recommend to use 100kΩ/β = 4250 NTC thermistor by Murata (NCP15WF104F03RC). See the related section in Application Information for detail.
5	CSN3	**Negative Differential Current Sense Input for Vcore Phase 3.** When Vcore phase 3 is not used, pull high this pin to VCC through a 1kΩ resistor to disable PWM3 to let Vcore VR operate in 2-phase configuration.
6	CSP3	**Positive Differential Current Sense Input for Vcore Phase 3.** When Vcore phase 3 is not used, short this pin to GND when Vcore VR is configured in 2-phase configuration.
7	CSN2	**Negative Differential Current Sense Input for Vcore Phase 2.** When Vcore phase 2 is not used, pull high this pin to VCC through a 1kΩ resistor to disable PWM2 to let Vcore VR operate in single-phase configuration.
8	CSP2	**Positive Differential Current Sense Input for Vcore Phase 2.** When Vcore phase 2 is not used, short this pin to GND when Vcore VR is configured in single-phase configuration.
9	CSN1	**Negative Differential Current Sense Input for Vcore Phase 1.**
10	CSP1	**Positive Differential Current Sense Input for Vcore Phase 1.**
11	ISUM	**Over Current Protection Threshold Setting and Sensing for Vcore.** Connect a resistor from this pin to GND to set the over current protection threshold. Do not connect any capacitor to this pin. The output current of this pin is proportional to the total load current. The total load current is sensed and flows out of this pin, and a resistor from this pin to GND makes the ISUM voltage proportional to the total output current. When the voltage on ISUM pin exceeds 1.5V, only the ALERT# will be pulled low to issue the Iccmax alert through SVID interface. When the voltage on ISUM pin exceeds 1.95V (130% of 1.5V, default), the over current protection will be tripped to shutdown the controller.
12	CSN	**Inverting Input of Total Current Sense Amplifier for Vcore.**
13	TONSET	**PWM On-time Setting.** Connect a resistor from this pin to GND to set the PWM on-time. The Vcore VR and VccGT VR share the same PWM on-time setting.
14	CSP	**Non-Inverting Input of Total Current Sense Amplifier for Vcore.**

No.	Name	Pin Function
15	COMP	**Output of Control Loop Error Amplifier for Vcore.** Connect a resistor in series with a capacitor from this pin to GND for voltage control loop compensation.
16	FB	**Inverting Input of the Error Amplifier for Vcore.**
17	EAP	**Non-inverting Input of the Error Amplifier for Vcore.** Connect a resistor between this pin and DAC to set the droop (load line) function.
18	DAC	**DAC Output for Vcore.** The output voltage of this pin is the reference voltage for the Vcore rail. DAC voltage is measured with respect to FBRTN. Connect a capacitor from this pin to FBRTN.
19	FBRTN	**Output Voltage Feedback Return for Vcore.** Inverting input to the differential voltage sense amplifier. FBRTN is the reference point in DAC output voltage measurement. Connect this pin directly to the processor output voltage feedback return sense point, namely VSS_SENSE.
20	IMON	**Output Current Monitor for Vcore.** Connect a resistor from this pin to GND to implement digital output current reporting function for Vcore VR. The output current of this pin is proportional to the total load current. The total load current is sensed and flows out of this pin, and a resistor from this pin to GND makes the IMON voltage proportional to the total output current. The built-in analog-to-digital converter (ADC) converts the IMON voltage to digital content for output current reporting via SVID interface. A capacitor can be connected from IMON to GND to adjust the response time of IMON. Note that the IMON is used only for digital output current reporting. See the related section in functional description for IMON capacitor selection.
21	SYSFAULT#	**SYSFAULT# Indicator.** This pin is an open-drain output.
22	VINSEN	**Power Stage Input Voltage Sense.** Directly connect this pin to the power stage input V_{IN}. The controller senses the voltage on this pin for power stage input voltage V_{IN} detection. The VINSEN voltage is also used for PWM on-time calculation.
23	VCC	**Supply Input for Logic Control Circuit.** Connect this pin to a 5V voltage source via an RC filter. VCC is the supply input for the logic control circuit.
24	PROG3	**Function Setting Pin 3.** This pin is used to set dynamic VID transition boost and multi-phase transient boost function enable/disable control. Connect a resistor from this pin to GND to select these two parameters.
25	PROG4	**Function Setting Pin 4.** This pin is used to set internal compensation resistor (Rcomp_int) value and the PWM on-time width for multi-phase transient boost function. Connect a resistor from this pin to GND to select these two parameters.
26	VRHOT#	**SVID Thermal Indicator.** This pin is an open drain structure and it is active low. The controller asserts VRHOT# to indicate the platform that the VR temperature is higher than the threshold. The value of VRHOT# assertion is 106°C, and the value of SVID thermal alert is 103°C.
27	VR_RDY	**VR Ready Indicator.** This pin is an open drain structure and it is active high. Pull up this pin through a proper resistor to a voltage source. The controller asserts VR_RDY (goes high) to indicate that the controller is ready to accept SVID command.
28	SCLK	**SVID Clock Input.**
29	ALERT#	**SVID Alert# Line.**
30	SDIO	**SVID Data I/O.**

No.	Name	Pin Function
31	EN	**Chip Enable Control Input.** Pull this pin above 0.8V enables the chip. Pull this pin below 0.3V to disable the chip. It's typically connected to the output of the VTT voltage power rail on the mother board.
32	IMONA	**Output Current Monitor for VccGT.** Connect a resistor from this pin to GND to implement digital output current reporting function for VccGT VR. The output current of this pin is proportional to the total load current. The total load current is sensed and flows out of this pin, and a resistor from this pin to GND makes the IMONA voltage proportional to the total output current. The built-in analog-to-digital converter (ADC) converts the IMONA voltage to digital content for output current reporting via SVID interface. A capacitor can be connected from IMONA to GND to adjust the response time of IMONA. Note that the IMONA is used only for digital output current reporting. See the related section in functional description for IMONA capacitor selection.
33	FBRTNA	**Output Voltage Feedback Return for VccGT.** Inverting input to the differential voltage sense amplifier. FBRTNA is the reference point in DACA output voltage measurement. Connect this pin directly to the processor output voltage feedback return sense point, namely VSSGT_SENSE.
34	DACA	**DAC Output for VccGT.** The output voltage of this pin is the reference voltage for the VccGT rail. DACA voltage is measured with respect to FBRTNA. Connect a capacitor from this pin to FBRTNA.
35	EAPA	**Non-Inverting Input of the Error Amplifier for VccGT.** Connect a resistor between this pin and DACA to set the droop (load line) function.
36	FBA	**Inverting Input of the Error Amplifier for VccGT.**
37	COMPA	**Output of Control Loop Error Amplifier for VccGT.** Connect a resistor in series with a capacitor from this pin to GND for voltage control loop compensation.
38	CSNA	**Inverting Input of Total Current Sense Amplifier for VccGT**
39	PROG1	**Function Setting Pin 1.** This pin is used to set SVID VR address. Connect a resistor from this pin to GND to select the SVID VR address for the two voltage regulators. The SVID VR address of [Vcore/VccGT] can be set as [00, 01], [01, 00], [00, 02] or [01, 03]. Refer to the related section in Application Information for detail and strictly follow the recommended setting.
40	CSPA	**Non-Inverting Input of Total Current Sense Amplifier for VccGT.**
41	ISUMA	**Over Current Protection Threshold Setting and Sensing for VccGT.** Connect a resistor from this pin to GND to set the over current protection threshold. Do not connect any capacitor to this pin. The output current of this pin is proportional to the total load current. The total load current is sensed and flows out of this pin, and a resistor from this pin to GND makes the ISUMA voltage proportional to the total output current. When the voltage on ISUMA pin exceeds 1.5V, only the ALERT# will be pulled low to issue the Iccmax alert through SVID interface. When the voltage on ISUMA pin exceeds 1.95V (130% of 1.5V), the over current protection will be tripped to shutdown the controller.
42	CSP1A	**Positive Differential Current Sense Input for VccGT Phase 1.** When VccGT is configured as 1-phase, short this pin to GND.
43	CSN1A	**Negative Differential Current Sense Input for VccGT Phase 1.** When VccGT is configured as 1-phase, short this pin to GND.
44	CSP2A	**Positive Differential Current Sense Input for VccGT Phase2.** To disable the MOSFET driver of this phase (BOOT2A, UG2A, PH2A, LG2A), short this pin to GND. Refer to the related section in Application Information for detail.

| No.	Name	Pin Function
45	CSN2A	**Negative Differential Current Sense Input for VccGT Phase2.** To disable the MOSFET driver of this phase (BOOT2A, UG2A, PH2A, LG2A), pull high this pin to VCC through a 1kΩ resistor to disable this phase. Refer to the related section in Application Information for detail.
46	TSENSEA	**Thermal Monitoring Input for VccGT.** Connect a specified negative temperature coefficient (NTC) thermistor network from this pin to GND for VccGT VR temperature sensing. Recommend to use 100kΩ/β = 4250 NTC thermistor by Murata (NCP15WF104F03RC). See the related section in Application Information for detail.
47	BOOT1A	**Bootstrap Supply for Upper Gate Driver for VccGT Phase 1.** This pin is the supply input for the upper MOSFET gate driver. Connect the bootstrap capacitor C_{BOOT} between BOOT1A pin and PH1A pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Use at least 0.1uF MLCC as C_{BOOT}, and make sure C_{BOOT} is placed close to the controller.
48	UG1A	**Upper Gate Driver Output for VccGT Phase 1.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when to turn on/off upper MOSFET.
49	PH1A	**Switch Node for VccGT Phase 1.** Connect this pin to the joint of upper MOSFET source, inductor and lower MOSFET drain. This pin is used as the return ground for upper MOSFET floating drive. Voltage on this pin is monitored by the shoot-through protection circuitry to determine when to turn on the lower MOSFET.
50	LG1A	**Lower Gate Driver Output for VccGT Phase 1.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when to turn on the upper MOSFET.
51	PVCC	**Supply Input for Embedded MOSFET Driver.** Connect this pin to a 12V voltage source, and bypass this pin to GND with at least 1.0uF MLCC placed very close to the PVCC pin. PVCC is the supply input for the embedded MOSFET drivers.
52	PROG2	**Function Setting Pin 2.** This pin is used to set the initial start up voltage (Vboot). Connect a resistor from this pin to GND to select Vboot. The Vboot can be set to 0V, 0.8V, 1.05V, 1.2V or 1.5V. The Vcore rail and VccGT rail share the same Vboot setting.
53	LG2A	**Lower Gate Driver Output for VccGT Phase 2.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when to turn on the upper MOSFET.
54	PH2A	**Switch Node for VccGT Phase 2.** Connect this pin to the joint of upper MOSFET source, inductor and lower MOSFET drain. This pin is used as the return ground for upper MOSFET floating drive. Voltage on this pin is monitored by the shoot-through protection circuitry to determine when to turn on the lower MOSFET.
55	UG2A	**Upper Gate Driver Output for VccGT Phase 2.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when to turn on/off upper MOSFET.
56	BOOT2A	**Bootstrap Supply for Upper Gate Driver for VccGT Phase 2.** This pin is the supply input for the upper MOSFET gate driver. Connect the bootstrap capacitor C_{BOOT} between BOOT2A pin and PH2A pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Use at least 0.1uF MLCC as C_{BOOT}, and make sure C_{BOOT} is placed close to the controller.
57	LG1	**Lower Gate Driver Output for Vcore Phase 1.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when to turn on the upper MOSFET.

No.	Name	Pin Function
58	PH1	**Switch Node for Vcore Phase 1.** Connect this pin to the joint of upper MOSFET source, inductor and lower MOSFET drain. This pin is used as the return ground for upper MOSFET floating drive. Voltage on this pin is monitored by the shoot-through protection circuitry to determine when to turn on the lower MOSFET.
59	UG1	**Upper Gate Driver Output for Vcore Phase 1.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the shoot-through protection circuitry to determine when to turn on/off upper MOSFET.
60	BOOT1	**Bootstrap Supply for Upper Gate Driver for Vcore Phase 1.** This pin is the supply input for the upper MOSFET gate driver. Connect the bootstrap capacitor C_{BOOT} between BOOT1 pin and PH1 pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Use at least 0.1uF MLCC as C_{BOOT}, and make sure C_{BOOT} is placed close to the controller.
	Exposed Pad	**Ground.** The exposed pad is the ground of embedded MOSFET drivers and logic control circuits, and it must be soldered to a large PCB and connected to GND.

Functional Block Diagram
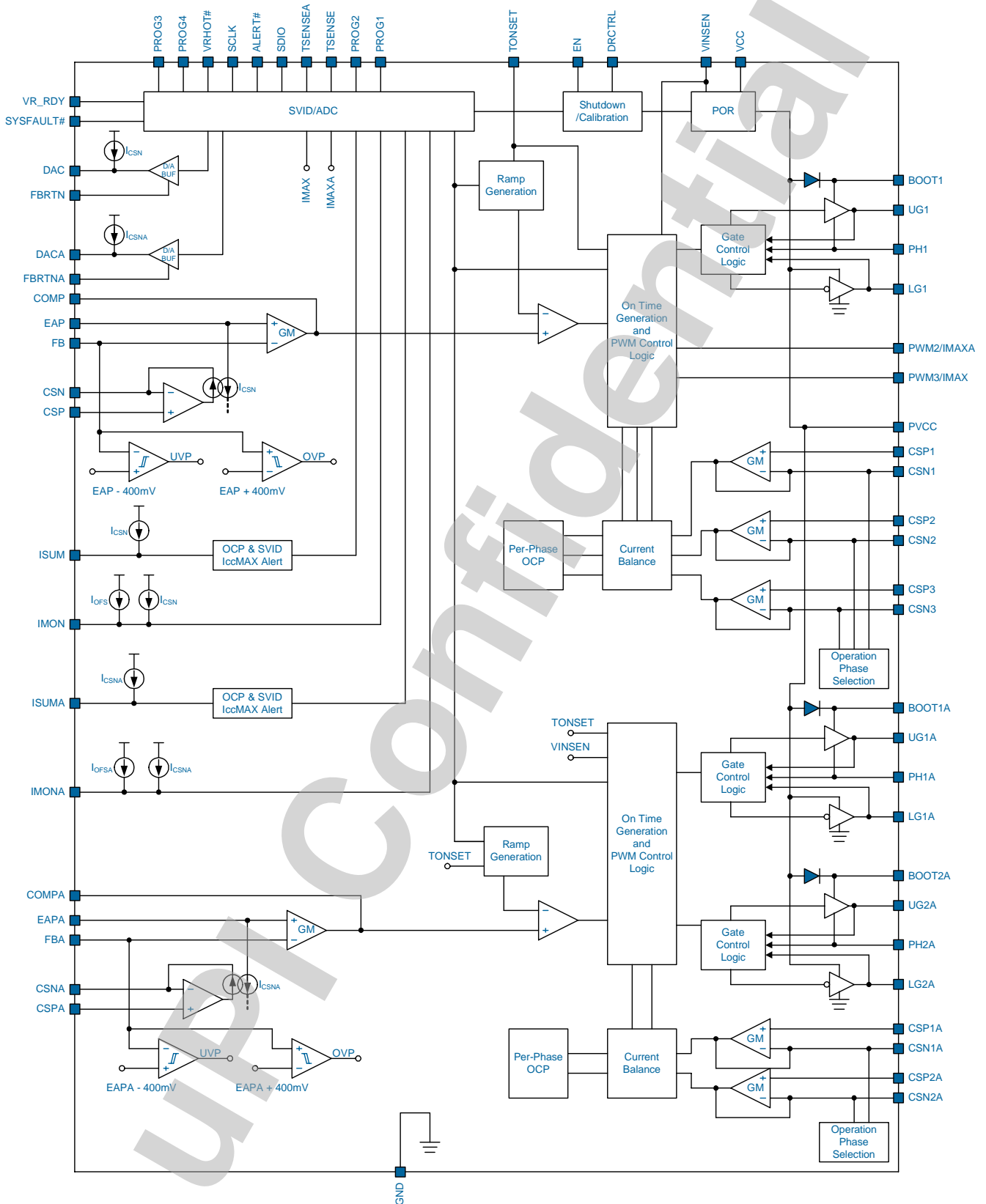
Functional Description

Power Input and Power On Reset

The uP9507 has two power inputs VCC and PVCC. VCC is the 5V supply input for control logic circuit of the controller. RC filter to VCC is required for locally bypassing this supply input. PVCC is the supply power of three integrated 12V MOSFET gate drivers. VCC and PVCC have individual power on reset (POR) function. VINSEN is the power stage input voltage sense pin, and it also has power on reset function. The controller monitors the VINSEN voltage for PWM on-time calculation. EN is the chip enable input pin. Logic high to this pin enables the controller, and logic low to this pin disables the controller. The above four inputs (VCC, PVCC, VINSEN and EN) are monitored to determine whether the controller is ready for operation.

Figure 1 shows the power ready detection circuit. The VCC voltage is monitored for power on reset with typically 4.3V threshold at its rising edge. The PVCC voltage is monitored for power on reset with typically 8V threshold at its rising edge. The VINSEN voltage is monitored for power on reset with typically 6V threshold at its rising edge. When VCC, PVCC and VINSEN are all ready, the controller waits for EN to start up. When EN pin is driven above 0.8V, the controller begins its start up sequence. When EN pin is driven below 0.3V, the controller will be turned off, and it will clear all fault states to prepare to next soft-start once the controller is re-enabled. Note that only VCC or EN toggle will clear all fault state, VINSEN or PVCC toggle is not used for clearing fault state. Anytime any one of the four inputs falls below their power on reset level will shutdown the controller.
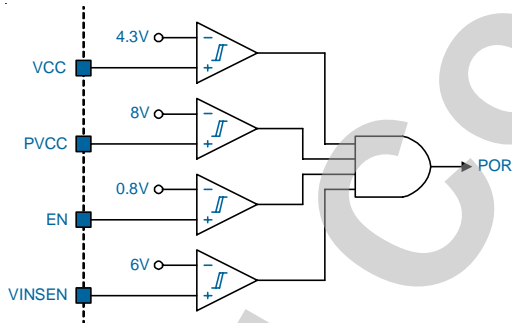
Figure 1. Circuit for Power Ready Detection

Controller Start up Sequence

When VCC, PVCC, VINSEN inputs are all ready, the controller waits for the EN signal to initiate the power on sequence. After EN goes high, the controller waits for a delay time T_A (<2.5ms) then VR_RDY goes high to indicate that the PWM controller is ready for accepting SVID command. At the same time, the output voltage starts to ramp up to Vboot with always slow slew rate for non-zero Vboot case. After output voltage settled to Vboot, the controller assert ALERT#. Then the start up sequence is over. Figure 2 shows the typical start up sequence for non-zero Vboot case. Time interval T_B is determined by the Vboot voltage and the slow slew rate. Figure 3 shows the typical start up sequence of zero-Vboot case. For the zero Vboot case, the output voltage slew rate is determined by the SetVID command. Note that VR_RDY goes high after delay time T_A in both cases.

Figure 2. Start up Sequence and Enable Timing with Non-zero Vboot

Figure 3. Start up Sequence and Enable Timing with Zero Vboot

Initial Parameter Setting

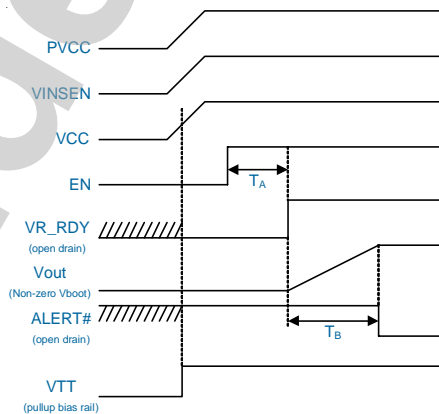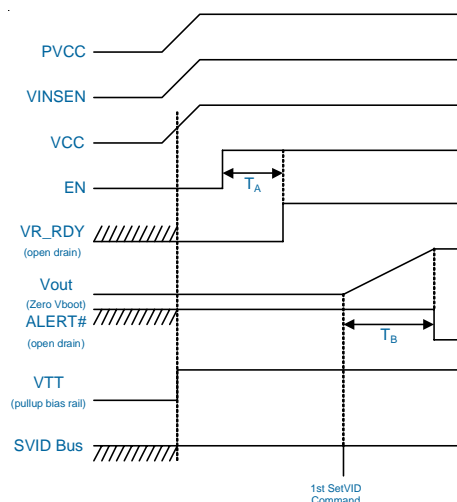There are four essential VR initial parameters that need to be determined such as Vcore SVID register 0x21h value, VccGT SVID register 0x21h value, SVID VR address and output initial start up voltage Vboot. They are programmed by PWM3_IMAX, PWM2_IMAXA, PROG1 and PROG2 as shown in Figure 4. Each parameter setting is detailed in the following sections.
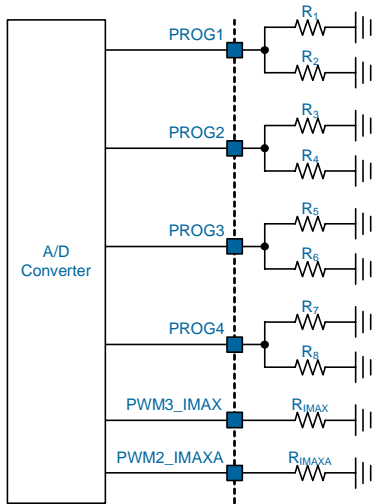

Figure 4. Initial Parameter Setting

Vcore SVID Register (Iccmax) Value Setting (PWM3_IMAX)

The PWM3_IMAX is a multi-functional pin, which is used to set specific SVID register value and outputs PWM signal for external MOSFET driver. Refer to Figure 4, a resistor R_{IMAX} connected from this pin to ground sets the Vcore SVID register 0x21h (Iccmax) value. During the initial setting period, a 10uA current source is turned on for a period of time to flow out of this pin through R_{IMAX} to create voltage drop on this pin. This voltage is digitized by an internal 8-bit A/D converter and stored in Vcore SVID register 0x21h (Iccmax). The A/D converter scales 2.56V into 256 levels, which means 10mV represents 1A. For example, if the SVID register 0x21h (Iccmax) value to be set to 100A (64h), the voltage should be 10mV x 100 = 1V. Therefore the resistor R_{IMAX} is 1V / 10uA = 100kΩ. The programmable range is from 00h to FFh (0A to 256A). If the pin voltage is greater than 2.56V, the SVID register 0x21h value will still be FFh. Note that this setting is only for determining SVID register value, and is not used for over current protection or SVID Iccmax alert function.

VccGT SVID Register (Iccmax) Value (PWM2_IMAXA)

The PWM2_IMAXA is a multi-functional pin, which is used to set specific SVID register value and outputs PWM signal for external MOSFET driver. Refer to Figure 4, a resistor R_{IMAXA} connected from this pin to ground sets the VccGT SVID register 0x21h (Iccmax) value. During the initial setting period, a 10uA current source is turned on for a period of time to flow out of this pin through R_{IMAXA} to create voltage drop on this pin. This voltage is digitized by an internal 8-bit A/D converter and stored in VccGT SVID register 0x21h (Iccmax). The A/D converter scales 2.56V into 256 levels, which means 10mV represents 1A. For example, if the SVID register 0x21h (Iccmax) value to be set to 60A (3Ch), the voltage should be 10mV x 60 = 0.6V. Therefore the resistor R_{IMAXA} is 0.6V / 10uA = 60kΩ. The programmable range is from 00h to FFh (0A to 256A). If the pin voltage is greater than 2.56V, the SVID register 0x21h value will still be FFh. Note that this setting is only for determining SVID register value, and is not used for over current protection or SVID Iccmax alert function.

SVID VR Address (PROG1)

The uP9507 features selectable SVID VR address for maximized flexibility in platform design. PROG1 is a function setting pin, which is used to set this essential parameter. Refer to Figure 4, resistors R_1 and R_2 connected in parallel from this pin to ground sets the SVID VR address. The SVID VR address of [Vcore/ VccGT] can be set as [00, 01], [01, 00], [00, 02] or [01, 03]. This makes the SVID VR address interchangeable/selectable, and provides more design flexibility per different power requirement. Table 1 shows the recommended resistance value for PROG1 function setting. Strictly follows the recommended resistor value in PROG1 setting. Note that for the rail with SVID address being set to 02h or 03h, its Vboot voltage will be fixed at 1.05V, regardless of the PROG2 pin setting. See Initial Start up Voltage (Vboot) (PROG2) section for detail.

Table 1. SVID VR Address Setting

No.	SVID Address (Vcore, VccGT)	PROG1 Recommended Resistor Value (kΩ) in Parallel	
		R_1	R_2
1	00h, 01h	0	Open
2	01h, 00h	13	12
3	00h, 02h	24	24
4	01h, 03h	47	43

Note: Strictly follow the recommended resistor value to avoid catastrophic system fault. Resistance value greater than 56kΩ is FORBIDDEN.

Operation Phase Disable Function

The uP9507 supports operation phase disable function to further increase the design flexibility. Platform designer can choose to disable some phases to meet their design requirement. Both Vcore and VccGT rail support operation phase disable function. The minimum operation phase number is 1+1-phase. In general, to disable a specific phase, pull up CSNx to VCC through 1kΩ resistor and tie CSPx to ground for that phase. The controller detects all the CSNx and CSPx voltage at VCC power on reset to determine operation phase number.

To let VccGT in single-phase operation, pull up CSN2A to VCC through 1kΩ resistor and tie CSP1A to ground. The CSN1A and CSP1A should be remain in normal connection with no change. In this case, the embedded MOSFET driver with pin name suffix *2A* is disabled. Table 2 shows the operation phase number setting. Strictly follow Table 2 setting to disable phases. Incorrect PROG1 setting and incorrect pin CSPx/CSNx pull up/down connection will cause catastrophic fault during start up.

Table 2. Operation Phase Number Setting

Configuration	Supported Operation Phase Number	Embedded Driver Number	Pin Connection, Pull High/Low to Target							
			CSP2	CSN2	CSP3	CSN3	CSP2A	CSN2A	CSP1A	CSN1A
3+2-Phase	3+2	1+2	--	--	--	--	--	--	--	--
	2+2	1+2	--	--	GND	VCC	--	--	--	--
	1+2	1+2	GND	VCC	GND	VCC	--	--	--	--
	3+1	1+1	--	--	--	--	GND	VCC	Normal connection (Note 2)	Normal connection (Note 2)
	2+1	1+1	--	--	GND	VCC	GND	VCC	Normal connection (Note 2)	Normal connection (Note 2)
	1+1	1+1	GND	VCC	GND	VCC	GND	VCC	Normal connection (Note 2)	Normal connection (Note 2)

Note 1: "--" denotes normal connection.
Note 2: For VccGT in single phase operation, CSP1A and CSN1A should be in normal connection.
Note 3: A 10kΩ resistor must still be connected between DRCTRL to GND even if external MOSFET driver is unused.
Note 4: Use 1kΩ pull up resistor when pull up to VCC.
Note 5: Strictly follow the table for phase disable. Incorrect PROG1 setting and incorrect pin pull up/down connection will cause catastrophic fault during start up.

Initial Start up Voltage (Vboot) (PROG2)

The uP9507 features selectable initial start up voltage (Vboot). PROG2 is a function setting pin, which is used to set this essential parameter. Refer to Figure 4, resistors R_3 and R_4 connected in parallel from this pin to ground sets the initial start up voltage (Vboot). The Vboot can be set to 0V, 0.8V, 1.05V, 1.2V or 1.5V. Both the Vcore rail and VccGT rail share the same Vboot setting. Table 3 shows the recommended resistance value for PROG2 function setting.

Although Vcore and VccGT share the same Vboot setting, there is an exception for the rail with SVID address being set to 02h and 03h. For the rail with SVID address being set to 02h or 03h, its Vboot voltage will be fixed at 1.05V, regardless of the PROG2 pin setting. The Vboot voltage of other rail (SVID address = 00h or 01h) still follows PROG2 pin setting. In this case, the Vboot voltage for SVID address [00, 02], or [01, 03] will be different. For example, when Vboot is set to 0V (PROG2 pin short to GND) and SVID address is set to [00, 02], the Vboot voltage for the rail with address = 00 and address = 01 is 0V and 1.05V, respectively.

Table 3. Vboot Voltage Setting

No.	Vboot (V)	Recommended Parallel Resistor Type (kΩ)	
		R_3	R_4
1	0	0	Open
2	0.8	4.3	33
3	1.5	13	12
4	1.2	16	20
5	1.05	24	24

Note: For the rail with SVID address being set to 02h or 03h, its Vboot voltage will be fixed at 1.05V, regardless of the PROG2 pin setting. The Vboot voltage of other rail (SVID address = 00h or 01h) still follows PROG2 pin setting.

Dynamic VID Transition Boost, Multi-Phase TB Enable Control (PROG3)

Refer to Figure 4, the PROG3 pin is used to set two VR parameters: dynamic VID transition boost and load transient boost enable control. The uP9507 provides dynamic VID transition boost function to improve the dynamic VID (D-VID) transition performance. Both the Vcore rail and VccGT rail share the same setting. In addition, this part provides load transient boost function to improve load transient response when in multi-phase operation. Similarly, both the Vcore rail and VccGT rail share the same setting. Table 4 shows the recommended resistance value for PROG3 function setting.

Table 4. D-VID Transition Boost and TB Enable Setting

No.	Load Transient Boost in Multi-Phase Operation	Dynamic VID Transition Boost	Recommended Parallel Resistor Type (kΩ)	
			R_5	R_6
1	Disable	60mV	0	Open
2		75mV	4.3	33
3		90mV	13	12
4		105mV	16	20
5		120mV	24	24
6		135mV	33	33
7		150mV	47	43
8		165mV	68	56
9	Enable	60mV	82	82
10		75mV	110	110
11		90mV	150	150
12		105mV	220	180
13		120mV	270	270
14		135mV	360	330
15		150mV	470	560
16		165mV	Open	Open

Internal Rcomp_int and Multi-Phase TB On-Time Setting (PROG4)

Refer to Figure 4, the PROG4 pin is used to set two VR parameters: internal compensation resistor Rcomp_int and PWM on-time for load transient boost function. There is an external resistor Rcomp connected to COMP pin for voltage loop compensation. The internal compensation resistor (Rcomp_int) will be in series with the external Rcomp only when the VR is in single-phase operation to improve the load transient response. When the VR is in multi-phase operation, the Rcomp_int will be short circuit. The other parameter to be set is the PWM on-time of load transient boost for load transient response improvement. This parameter is only effective when this function is enabled (set by PROG3). Table 5 shows the recommended resistance value for PROG4 function setting.

Table 5. Rcomp_int and TB On-Time Setting

No.	TB On-Time for Vcore in multi-phase	TB On-Time for VccGT in multi-phase	Rcomp_int for Vcore in single-phase	Rcomp_int for VccGT in single-phase	Recommended Parallel Resistor Type (kΩ)	
					R_1	R_2
1	600ns	600ns	+5kΩ	+5kΩ	0	Open
2				+15kΩ	4.3	33
3			+15kΩ	+5kΩ	13	12
4				+15kΩ	16	20
5		800ns	+5kΩ	+5kΩ	24	24
6				+15kΩ	33	33
7			+15kΩ	+5kΩ	47	43
8				+15kΩ	68	56
9	800ns	600ns	+5kΩ	+5kΩ	82	82
10				+15kΩ	110	110
11			+15kΩ	+5kΩ	150	150
12				+15kΩ	220	180
13		800ns	+5kΩ	+5kΩ	270	270
14				+15kΩ	360	330
15			+15kΩ	+5kΩ	470	560
16				+15kΩ	Open	Open

External MOSFET Driver Control

The DRCTRL pin is used for controlling the enable/disable of external MOSFET drivers. Make sure to connect a 10kΩ resistor from this pin to GND and place this resistor close to the controller. This resistor is used to generate the reference current for thermal sense by TSENSE and TSENSEA. Do not use any other resistance value. This 10kΩ resistor must still be connected between DRCTRL to ground even if external MOSFET driver is unused. Connect this pin to a resistor R_{ISO} and then connect to the enable control pin of the external MOSFET drivers as shown in Figure 5. The recommended resistance value of R_{ISO} is between 1kΩ to 10kΩ. The DRCTRL is a noise sensitive pin, therefore the PCB trace routing should be kept away from other nets, especially the switching signals. It is required to keep at least 20mil space to other nets.
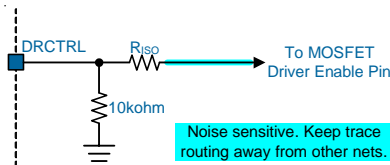

Figure 5. DRCTRL Connection

PWM On Time Setting

The PWM on-time is set by an external resistor R_{TON} connected between TONSET pin and GND. The controller senses VINSEN voltage to obtain input voltage information for PWM on-time calculation. Both the Vcore rail and VccGT rail share the same PWM on-time setting. The PWM on-time can be calculated as below equation.

$$T_{ON}(ns) = \left(\frac{V_{OUT}}{V_{IN}}\right) \times R_{TON} \times 100$$

Table 6 lists the switching frequency and the recommended resistor R_{TON} value (with condition: V_{IN} = 12V, V_{OUT} = 1.2V). For example, given V_{IN} = 12V, V_{OUT} = 1.2V, R_{TON} = 50kΩ, T_{ON} is about 500ns by above equation. The PWM frequency is about 200kHz. Note that the resistance value of R_{TON} value must be greater than 10kΩ to ensure the PWM on-time calculation circuit in normal operation.

Table 6. Switching Frequency and Resistor R_{TON}

Switching Frequency (kHz)	Recommended Resistor R_{TON} (kΩ)
200	50
300	33.3
400	25
500	20
600	16.7
Note: The minimum of resistor R_{TON} value is 10kΩ.	

Soft Start

The slew rate of output voltage during soft start operation and dynamic VID voltage change is determined internally. Place a MLCC C_{DAC} between DAC and FBRTN (DACA and FBRTNA for VccGT). The recommended capacitance of C_{DAC} is 10nF. The slew rate during soft start operation is always slow for non-zero Vboot case. The slow slew rate is determined by the processor in SVID register 2Ah.

Dynamic VID Change and Slew Rate

The controller accepts SetVID command via SVID bus for output voltage change during normal operation. This allows the output voltage to change while the DC/DC converter is running and supplying current to the load. This is commonly referred to as VID on-the-fly (VID OTF). A VID OTF event may occur under either light or heavy load condition. This voltage change direction can be upward or downward. Per SetVID command, the slew rate can be fast or slow. The slow slew rate is determined by the SVID register 2Ah, which can only be programmed by the processor. The default value of slow slew rate is 1/2 of fast slew rate. The value of fast slew rate is 12mV/us.

Output Voltage Differential Sense

The uP9507 uses differential sense by a high-gain low-offset error amplifier for output voltage differential sense as shown in Figure 6. The CPU voltage is sensed by the FB and FBRTN pins (FBA and FBRTNA for VccGT). FB pin is connected to the positive remote sense pin VCC_SENSE of the CPU via the resistor R_{FB}. FBRTN pin is connected to the negative remote sense pin VSS_SENSE of CPU directly. (VCCGT_SENSE and VSSGT_SENSE for VccGT). The error amplifier compares the V_{FB} with V_{EAP} (= V_{DAC} - I_{CSN} x R_{DRP}) to regulate the output voltage.
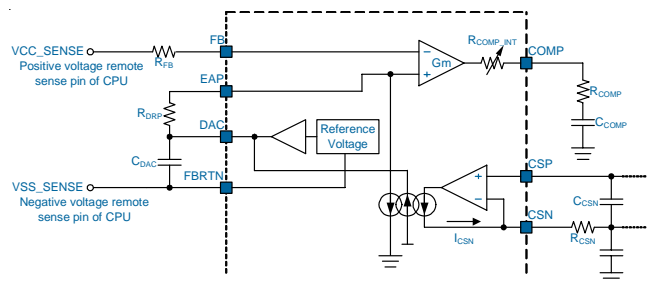

Figure 6. Output Voltage Differential Sense

Total Load Current Sense

The uP9507 uses a low input offset current sense amplifier (CSA) to sense the total load current flowing through inductors for droop function by CSP and CSN (CSPA and CSNA for VccGT) as shown in Figure 7.
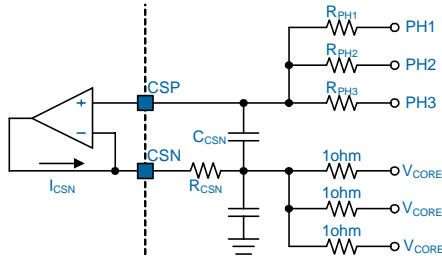

Figure 7. Total Load Current Sense

The voltage across C_{CSN} is proportional to the total load current, and the output current of CSA (I_{CSN}) is also proportional to the total load current of the voltage regulator. The sensed current I_{CSN} represents the total output current of the regulator, and it is directly used for droop function, and further internally mirrored for SVID IccMAX Alert function, total output over current protection, and output current reporting. I_{CSN} is calculated as follows.

$$I_{CSN} = \frac{I_{OUT} \times \dfrac{R_{DC}}{N}}{R_{CSN}}$$

In this inductor current sensing topology, R_{PH} and C_{CSN} must be selected according to the equation below:

$$k \times \frac{L}{R_{DC}} = \frac{R_{PH} \times C_{CSN}}{N}$$

where R_{DC} is the DCR of the output inductor L, N is the operation phase number. Theoretically, k should be equal to 1 to sense the instantaneous total load current. But in real application, k is usually between 1.2 to 1.8 for better load transient response. Note that the resistance value of R_{CSN} must be less than 2kΩ to ensure the current sensing circuit in normal operation.

Droop (Load Line) Setting

As shown in Figure 6, the current I_{CSN} denotes the sensed total load current, which is mirrored to the EAP pin. When load current increases, I_{CSN} also increases and creates a voltage drop across R_{DRP}, and makes V_{EAP} lower than the V_{DAC} as follows.

$$V_{EAP} = V_{DAC} - I_{CSN} \times R_{DRP} = V_{DAC} - \left(\frac{I_{OUT} \times R_{DC}}{R_{CSN} \times N} \right) \times R_{DRP}$$

where R_{DC} is the DCR of output inductor, N is the operation phase number, and I_{OUT} denotes the total load current.

In steady state, the output voltage is regulated to V_{EAP}. As the total load current I_{OUT} increases, I_{CSN} increases proportionally, making V_{EAP} decreases accordingly. This makes the output voltage also decreases linearly as the total output current increases, which is also known as active voltage positioning (AVP). The slope of output voltage decrease to total load current increase is referred to as load line. The load line is defined as follows

$$Load\ Line = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{R_{DC} \times R_{DRP}}{R_{CSN} \times N}$$

IccMAX Alert and Total Output Over Current Protection (OCP)

As shown in Figure 8, the sensed current I_{CSN} is mirrored internally and fed to ISUM pin (ISUMA for VccGT) as I_{SUM} for SVID IccMAX Alert function and total output over current protection (OCP). A resistor R_{ISUM} is connected from ISUM pin to GND. This current flows through the resistor R_{ISUM}, creating voltage drop across it. As the total load current increases, the voltage on ISUM pin (V_{ISUM}) increases proportionally. When the ISUM pin voltage is greater than typically 1.5V, the SVID IccMAX alert will be triggered, and then the ALERT# will be pulled low to indicate the processor that the voltage regulator is in IccMAX condition. The output current level of triggering SVID IccMAX alert is calculated as follows.

$$I_{OUT\_IccMAX} = \frac{1.5}{R_{ISUM}} \times \frac{N \times R_{CSN}}{R_{DC}}$$
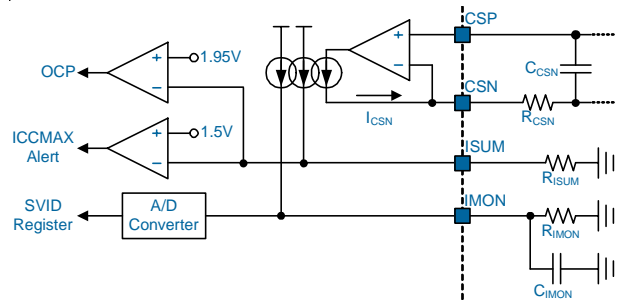
Figure 8. IccMAX Alert and Total Output OCP

When the ISUM pin voltage further increases to greater than the OCP threshold (default value is typically 130% of SVID IccMAX alert threshold of 1.5V) for a specific delay time, the total output current protection will be triggered. VR_RDY will be pulled low immediately, both UGx and LGx will be held low, and all PWM outputs will in high-impedance state to let driver turns off all MOSFETs to shutdown the regulator. The other unaffected voltage regulator will also shut down. The total output OCP is a latch-off type protection, and it can only be reset by VCC or EN toggling. Avoid adding capacitor to the ISUM pin. Additional capacitance to this pin will affect the current level of SVID IccMAX alert and the total output OCP. The default output current level of triggering total output OCP is calculated as follows.

$$I_{OUT\_OCP} = \frac{1.5}{R_{ISUM}} \times \frac{N \times R_{CSN}}{R_{DC}} \times 1.3$$

Total Output OCP and Operating Phase Number

The total output OCP level is usually designed for the voltage regulator that is operated in full phase condition by hardware setting. The actual operating phase number is controlled by the SVID SetPS command. When the operating phase number is decreased, the total output OCP level is decreased as well. The total output OCP level is changed per actual operating phase number. Table 7 shows the total output OCP ratio per actual operating phase number and the hardware configuration.

Table 7. Total Output OCP and Operating Phase Number

Total Output OCP Ratio		Operating Condition		
		3-Phase	2-Phase	1-Phase
Hardware Configuration	3-Phase	1	--	5/12
	2-Phase	--	1	2/3
	1-Phase	--	--	1

Output Current Reporting

Refer to Figure 8, the sensed current I_{CSN} is also separately mirrored and fed to IMON pin (IMONA for VccGT) as I_{IMON} for SVID output current reporting function. Connect a resistor R_{IMON} from IMON pin to GND. The current I_{IMON} flows through the resistor R_{IMON}, creating voltage drop across it. As the total load current increases, the voltage on IMON pin (V_{IMON}) increases proportionally. An internal analog-to-digital converter (ADC) converts V_{IMON} to a digital content for output current reporting through SVID interface. As V_{IMON} voltage increases, the SVID register 0x15h content increases. The IMON voltage has typically 600mV offset, which means V_{IMON} = 600mV and SVID register 0x15 = 00h. The ADC input range is typically 1.5V, which means the SVID register 0x15h = FFh when V_{IMON} = 2100mV. Further increase of V_{IMON} (>2.1V) is allowed, but the ADC results will remain at FFh. Capacitor can be added to the IMON pin to adjust the response time of current reporting. The IMON pin is for digital output current reporting only, not for SVID IccMAX alert function or OCP. The total output current level for SVID register 0x15h = FFh is calculated as follows.

$$I_{OUT_{SVID}0x15h=FFh} = \frac{1.5}{R_{IMON}} \times \frac{N \times R_{CSN}}{R_{DC}}$$

Note that the resistance value of R_{IMON} must be between 10kΩ to 60kΩ to ensure the controller in normal operation.

IMON/IMONA Capacitor Selection

The capacitor C_{IMON} connected from IMON to GND (C_{IMONA} for IMONA) is used to adjust the response time of IMON voltage change to load current change. It is recommended to add a capacitor to the IMON pin. However, too large capacitance for C_{IMON} is improper, and will affect the accuracy

in digital output current reporting. Due to the embedded A/D conversion circuit to the IMON pin, the RC time constant (tau) should be adequate to ensure correct operation and digital current reporting accuracy. Use 4 x tau = 160us as the rule of thumb to determine C_{IMON}. After resistor R_{IMON} is determined, the C_{IMON} is then calculated by

$$C_{IMON} \leq \frac{4 \times 160 \times 10^{-6}}{R_{IMON}}$$

Then choose a capacitance value that is closest to but not greater than the calculation for C_{IMON}.

Over Voltage Protection (OVP)

The controller monitors the voltage on FB pin (FBA for VccGT) for over voltage protection. The controller monitors the voltage on FB pin (FBA for VccGT) for under voltage protection. After output voltage ramps up to Vboot, the controller initiates OVP function. Once V_{FB} exceeds V_{EAP} + OVP threshold for a specific delay time, OVP is triggered. VR_RDY will be pulled low immediately, UGx will be held low, LGx will be held high, and PWM outputs will be low to let driver turns on low side MOSFET and turns off high side MOSFET to protect CPU. Since the low side MOSFET is turned on, the regulator output capacitor will be discharged and output voltage decreases as well. When FB pin voltage decreases to lower than typical 0.5V, LGx will be held low (PWM outputs turns to high impedance state) to turn off the low side MOSFET to avoid negative output voltage. The other unaffected voltage regulator will also shut down. The OVP is a latch-off type protection, and it can only be reset by VCC or EN toggling. The OVP detection circuit has a fixed delay time to prevent false trigger.

Under Voltage Protection (UVP)

The controller monitors the voltage on FB pin (FBA for VccGT) for under voltage protection. After output voltage ramps up to Vboot, the controller initiates UVP function. Once V_{FB} is lower than V_{EAP} - UVP threshold for a specific delay time, OVP is triggered. VR_RDY will be pulled low immediately, both UGx and LGx will be held low, and all PWM outputs will in high-impedance state to let driver turns off all MOSFETs to shutdown the regulator. The other unaffected voltage regulator will also shut down. The UVP is a latch-off type protection, and it can only be reset by VCC or EN toggling. The UVP detection circuit has a fixed delay time to prevent false trigger.

Per-Phase Over Current Protection

In addition to the total output current OCP, the controller provides per-phase current OCP to protect the voltage regulator. The controller uses DCR current sensing technique to sense the inductor current in each phase for per-phase over current protection and current balance as shown in Figure 9. In this inductor current sensing topology, the time constant can expressed as follows.

$$k \times \frac{L}{R_{DC}} = R_{CSPX} \times C_{CSX}$$

where L is the output inductor, R_{DC} is its parasitic resistance and k is a constant. Theoretically, if k = 1, the sensed current signal I_{CSNx} can be expressed as follows.

$$I_{CSNx} = \frac{I_{LX} \times R_{DC}}{R_{CSNx}}$$
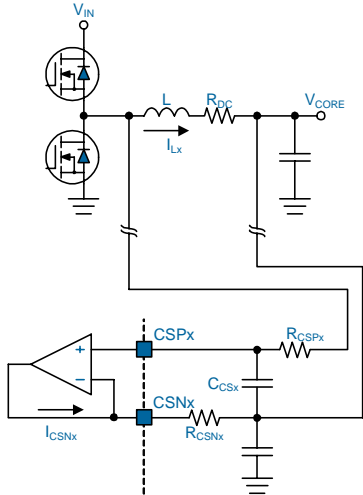
Figure 9. Phase Current Sense

The sensed current I_{CSNx} represents the current in each phase, and it is compared to a current source (typical = 100uA) for per-phase OCP. If the inductor current of any of the active operating phase exceeds the threshold for a specific delay time, the per-phase OCP is triggered. VR_RDY will be pulled low immediately, both UGx and LGx will be held low, and all PWM outputs will in high-impedance state to let driver turns off all MOSFETs to shutdown the regulator. The other unaffected voltage regulator will also shut down. The per-phase OCP is a latch-off type protection, and it can only be reset by VCC or EN toggling. Note that the resistance value of R_{CSNx} must be less than 2kΩ to ensure the current sensing circuit in normal operation. The resistance of R_{CSNx} and the default per-phase OCP level can be obtained using equation as follows.

$$R_{CSNx} = \frac{I_{OCP\_perphase} \times R_{DC}}{100uA}$$

Thermal Monitoring and VRHOT#

The TSENSE pin (TSENSEA for VccGT) is used for voltage regulator thermal monitoring. Connect a negative temperature coefficient (NTC) thermistor network from TSENSE pin to GND to implement this function as shown in Figure 10. The NTC thermistor is placed close to the hottest point of the regulator, normally close to the inductor and low-side MOSFET of phase 1. A precision current source flows out of the TSENSE pin through the temperature sense network to create a voltage drop V_{TSENSE} on this pin. As regulator temperature rises, the V_{TSENSE} decreases. Therefore the controller detects the V_{TSENSE} to obtain regulator thermal information for SVID thermal alert and VRHOT# function.

The controller asserts VRHOT# when the sensed temperature is higher than the value of SVID register 0x22h (Temp_Max), in which the default value is 6Ah (106°C). The temperature for SVID thermal alert and VRHOT# assertion is 103°C and 106°C, respectively. The curve of TSENSE (TSENSEA for VccGT) pin voltage and the sensed temperature is shown in Figure 11. Either Vcore or VccGT regulator can trigger the VRHOT# as long as the temperature of any of the two regulators exceeds the maximum temperature threshold. It is highly recommended to use 7.32kΩ as R_P, and 100kΩ/β = 4250 NTC thermistor by Murata (NCP15WF104F03RC). R_S is reserved for fine tune.
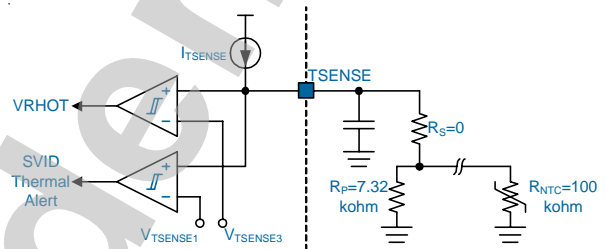
Figure 10. Regulator Temperature Sense
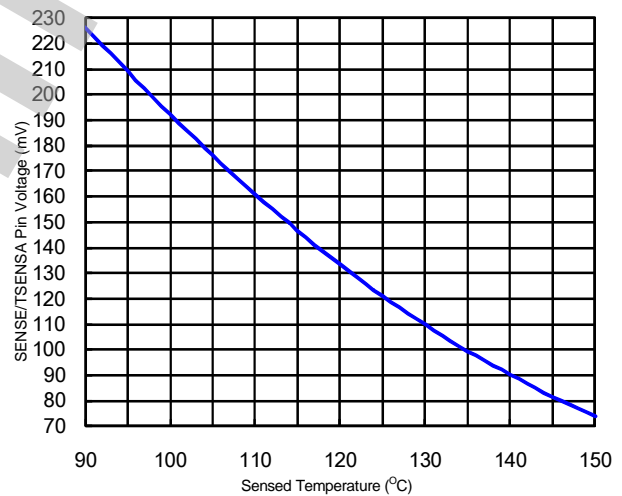
Figure 11. TSENSE/TSENSEA Pin Voltage and Sensed Temperature

Control Loop

The uP9507 adopts the uPI proprietary RCOT⁺™ control technology. The RCOT uses the constant on-time modulator. The output voltage is sensed to compare with the internal high accurate reference voltage. The reference voltage is commanded by CPU through the SVID interface. The amplified error signal V_{COMP} is compared to the internal ramp to initiate a PWM on-time. The RCOT⁺™ features easy design, fast transient response and is smooth mode transition and especially suitable for powering the microprocessor.

Functional Description

Table 8. IMVP8 VID Table

SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)
0x00	0.000	0x25	0.430	0x4A	0.615	0x6F	0.800	0x94	0.985	0xB8	1.165	0xDC	1.345
0x01	0.250	0x26	0.435	0x4B	0.620	0x70	0.805	0x95	0.990	0xB9	1.170	0xDD	1.350
0x02	0.255	0x27	0.440	0x4C	0.625	0x71	0.810	0x96	0.995	0xBA	1.175	0xDE	1.355
0x03	0.260	0x28	0.445	0x4D	0.630	0x72	0.815	0x97	1.000	0xBB	1.180	0xDF	1.360
0x04	0.265	0x29	0.450	0x4E	0.635	0x73	0.820	0x98	1.005	0xBC	1.185	0xE0	1.365
0x05	0.270	0x2A	0.455	0x4F	0.640	0x74	0.825	0x99	1.010	0xBD	1.190	0xE1	1.370
0x06	0.275	0x2B	0.460	0x50	0.645	0x75	0.830	0x9A	1.015	0xBE	1.195	0xE2	1.375
0x07	0.280	0x2C	0.465	0x51	0.650	0x76	0.835	0x9B	1.020	0xBF	1.200	0xE3	1.380
0x08	0.285	0x2D	0.470	0x52	0.655	0x77	0.840	0x9C	1.025	0xC0	1.205	0xE4	1.385
0x09	0.290	0x2E	0.475	0x53	0.660	0x78	0.845	0x9D	1.030	0xC1	1.210	0xE5	1.390
0x0A	0.295	0x2F	0.480	0x54	0.665	0x79	0.850	0x9E	1.035	0xC2	1.215	0xE6	1.395
0x0B	0.300	0x30	0.485	0x55	0.670	0x7A	0.855	0x9F	1.040	0xC3	1.220	0xE7	1.400
0x0C	0.305	0x31	0.490	0x56	0.675	0x7B	0.860	0xA0	1.045	0xC4	1.225	0xE8	1.405
0x0D	0.310	0x32	0.495	0x57	0.680	0x7C	0.865	0xA1	1.050	0xC5	1.230	0xE9	1.410
0x0E	0.315	0x33	0.500	0x58	0.685	0x7D	0.870	0xA2	1.055	0xC6	1.235	0xEA	1.415
0x0F	0.320	0x34	0.505	0x59	0.690	0x7E	0.875	0xA3	1.060	0xC7	1.240	0xEB	1.420
0x10	0.325	0x35	0.510	0x5A	0.695	0x7F	0.880	0xA4	1.065	0xC8	1.245	0xEC	1.425
0x11	0.330	0x36	0.515	0x5B	0.700	0x80	0.885	0xA5	1.070	0xC9	1.250	0xED	1.430
0x12	0.335	0x37	0.520	0x5C	0.705	0x81	0.890	0xA6	1.075	0xCA	1.255	0xEE	1.435
0x13	0.340	0x38	0.525	0x5D	0.710	0x82	0.895	0xA7	1.080	0xCB	1.260	0xEF	1.440
0x14	0.345	0x39	0.530	0x5E	0.715	0x83	0.900	0xA8	1.085	0xCC	1.265	0xF0	1.445
0x15	0.350	0x3A	0.535	0x5F	0.720	0x84	0.905	0xA9	1.090	0xCD	1.270	0xF1	1.450
0x16	0.355	0x3B	0.540	0x60	0.725	0x85	0.910	0xAA	1.095	0xCE	1.275	0xF2	1.455
0x17	0.360	0x3C	0.545	0x61	0.730	0x86	0.915	0xAB	1.100	0xCF	1.280	0xF3	1.460
0x18	0.365	0x3D	0.550	0x62	0.735	0x87	0.920	0xAC	1.105	0xD0	1.285	0xF4	1.465
0x19	0.370	0x3E	0.555	0x63	0.740	0x88	0.925	0xAD	1.110	0xD1	1.290	0xF5	1.470
0x1A	0.375	0x3F	0.560	0x64	0.745	0x89	0.930	0xAE	1.115	0xD2	1.295	0xF6	1.475
0x1B	0.380	0x40	0.565	0x65	0.750	0x8A	0.935	0xAF	1.120	0xD3	1.300	0xF7	1.480
0x1C	0.385	0x41	0.570	0x66	0.755	0x8B	0.940	0xB0	1.125	0xD4	1.305	0xF8	1.485
0x1D	0.390	0x42	0.575	0x67	0.760	0x8C	0.945	0xB1	1.130	0xD5	1.310	0xF9	1.490
0x1E	0.395	0x43	0.580	0x68	0.765	0x8D	0.950	0xB2	1.135	0xD6	1.315	0xFA	1.495
0x1F	0.400	0x44	0.585	0x69	0.770	0x8E	0.955	0xB3	1.140	0xD7	1.320	0xFB	1.500
0x20	0.405	0x45	0.590	0x6A	0.775	0x8F	0.960	0xB4	1.145	0xD8	1.325	0xFC	1.505
0x21	0.410	0x46	0.595	0x6B	0.780	0x90	0.965	0xB5	1.150	0xD9	1.330	0xFD	1.510
0x22	0.415	0x47	0.600	0x6C	0.785	0x91	0.970	0xB6	1.155	0xDA	1.335	0xFE	1.515
0x23	0.420	0x48	0.605	0x6D	0.790	0x92	0.975	0xB7	1.160	0xDB	1.340	0xFF	1.520
0x24	0.425	0x49	0.610	0x6E	0.795	0x93	0.980						

Table 9. Supported SVID Data and Configuration Register

Index	Register Name	Access	Default	Description
00h	Vender ID	RO	27h	Vender ID
01h	Product ID	RO	1Fh	Product ID
02h	Product Revision	RO	01h	Product Revision
05h	Protocol ID	RO	05h	Identifies what version of SVID protocol the controller supports.
06h	Capability	RO	81h	Bit mapped register, identifies the SVID VR capabilities and which of the optional telemetry are supported.
10h	Status_1	R-M, W-PWM	00h	Data register read after the alert# signal is asserted. Conveying the status of the VR.
11h	Status_2	R-M, W-PWM	00h	Data Register showing status_2 data. Conveying the status of the SVID bus.
15h	Output Current	R-M, W-PWM	--	Averaged output current.
1Ch	Status_2_Last Read	R-M, W-PWM	00h	This register contains a copy of the status2 data that was last read with the GETREG (status2) command.
21h	ICC_Max	RO Platform	--	Data register containing the Icc maximum the platform supports.
22h	Temp_Max	RO Platform	6Ah	Data register containing the temperature max the platform support and the level VRHOT# asserts. Binary format in °C, i.e. 6Ah = 160°C.
24h	SR_Fast	RO	0Ch	Data register containing the capability of fast slew rate the platform can sustain. Binary format in mV/us, i.e. 0Ch = 12mV/us.
25h	SR_Slow	RO	06h	Data register containing the capability of slow slew rate. Binary format in mV/us, i.e. 06h = 6mV/us.
26h	Vboot	RO Platform	--	Data register containing Vboot voltage in VID steps.
2Ah	Slow Slew Selector	RW Master	01h	Slew rate register must reflect actual slew rate.
2Bh	PS4 Exit Latency	RO	95h	This register holds an encoded value that represents the VR PS4 exit latency. 95h represents 160us
2Ch	PS3 Exit Latency	RO	45h	This register holds an encoded value that represents the VR PS3 exit latency. 45h represents 5us
2Dh	Enable to SVID Ready	RO	C9h	This register holds an encoded value that represents the VR ENABLE to Ready. C9h represents 2304us
30h	Vout Max	RW Master	FBh	This register is programmed by the master and sets the maximum VID the VR will support.

Table 9. Supported SVID Data and Configuration Register (Cont.)

Index	Register Name	Access	Default	Description
31h	VID Setting	RW Master	00h	Data register containing currently programmed VID voltage.
32h	Power State	RW Master	00h	Register containing the current programmed power state.
33h	Voltage Offset	RW Master	00h	Set offset in VID steps added to the VID setting for voltage margining.
34h	Multi VR Config	RW Master	01h	Bit mapped data register which configures multiple VRs behavior on the same bus.
35h	SetRegADR	RW Master	--	Scratch pad register for temporary storage of the SetRegADR pointer register.
42h	IVID1-VID	R/W	00h	VID associated with the max current defined in IVID1-I
43h	IVID1-I	R/W	FFh	The max current (1A/bit) expected when the VID is set as: IVID1-VID ≥ VID > IVID2-VID
44h	IVID2-VID	R/W	00h	VID associated with the max current defined in IVID2-I
45h	IVID2-I	R/W	FFh	The max current expected when the VID is set as: IVID2-VID ≥ VID > IVID3-VID
46h	IVID3-VID	R/W	00h	VID associated with the max current defined in IVID3-I
47h	IVID3-I	R/W	FFh	The max current expected when the VID is set as: IVID3-VID ≥ VID

Absolute Maximum Rating

(Note 1)

Supply Input Voltage VCC to GND -- -0.3V to +6V
Supply Input Voltage PVCC to GND -- -0.3V to +15V
VINSEN -- -0.3V to +30V
BOOTx to PHx -- -0.3V to +15V
PHx to GND
    DC --- -0.7V to +15V
    < 200ns -- -8V to +30V
BOOTx to GND
    DC --- -0.3V to (PVCC+15V)
    < 200ns -- -0.3V to +42V
UGx to PHx
    DC -- -0.3V to (BOOTx-PHx+0.3V)
    < 200ns -- -5V to (BOOTx-PHx+0.3V)
LGx to GND
    DC --- -0.3V to (PVCC+15V)
    < 200ns --- -5V to (PVCC+0.3V)
Other Pins --- -0.3V to +6V
Storage Temperature Range --- -65°C to +150°C
Junction Temperature --- 150°C
Lead Temperature (Soldering, 10 sec) --- 260°C
ESD Rating (Note 2)
    HBM (Human Body Mode) --- 2kV
    MM (Machine Mode) --- 200V

Thermal Information

Package Thermal Resistance (Note 3)
    VQFN7x7 - 60L θ_{JA} -- 31°C/W
    VQFN7x7 - 60L θ_{JC} --- 2°C/W
Power Dissipation, P_D @ T_A = 25°C
    VQFN7x7 - 60L --- 3.23W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range --- -40°C to +125°C
Operating Ambient Temperature Range -- -40°C to +85°C
Supply Input Voltage VCC --- 4.5V to 5.5V
Supply Input Voltage PVCC -- 10.8V to 13.2V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

(VCC = 5V, PVCC = 12V, T$_A$ = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VCC Supply Input						
VCC POR Threshold	POR$_{VCC}$	VCC rising	4.0	4.3	4.5	V
VCC POR Hysteresis	HYS$_{VCCPOR}$		--	0.3	--	V
Supply Current	I$_{VCC}$	EN = 5V, Vcore and VccGT VID = 0V, PWM no switching	--	7	--	mA
Shutdown Current	I$_{VCC\_SHDN}$	EN = 0V	--	50	--	uA
Supply Current in PS4	I$_{VCC\_PS4}$	EN = 5V, PS4 state	--	150	--	uA
PVCC Supply Input						
PVCC POR Threshold	POR$_{PVCC}$	PVCC rising	--	8	--	V
PVCC POR Hysteresis	HYS$_{PVCCPOR}$		--	2	--	V
Supply Current	I$_{PVCC}$	EN = 5V, Vcore and VccGT VID=0V, PWM no switching	--	250	--	uA
Shutdown Current	I$_{PVCC\_SHDN}$	EN = 0V	--	--	30	uA
Error Amplifier						
Offset Voltage	V$_{OS(EA)}$		-1	--	1	mV
Trans-Conductance	GM		--	2020	--	uA/V
Gain Bandwidth Product	G$_{BW(EA)}$	Guaranteed by Design	--	10	--	MHz
DAC Voltage Accuracy						
DAC Voltage Accuracy	V$_{DAC}$	VID = 0.75V to 1.52V, percentage to VID	-0.5	--	0.5	%
		VID = 0.5V to 0.745V	-8	--	8	mV
		VID = 0.25V to 0.495V	-10	--	10	mV
Slew Rate						
Slew Rate Fast	SR_Fast	SetVID_Fast	10	12	--	mV/us
Slew Rate Slow	SR_Slow	SetVID_Slow, SVID register 0x2Ah = 01	5	6	--	mV/us

| Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
EN Input						
Input High	V_{IH}		0.8	--	--	V
Input Low	V_{IL}		--	--	0.3	V
Pull-Low Current	I_{EN_PL}		1	2	3	uA
VIN Sense						
VINSEN POR Threshold	POR_{VINSEN_r}	VINSEN rising	--	6	--	V
VINSEN POR Threshold	POR_{VINSEN_f}	VINSEN falling	--	4.5	--	V
Input Current	I_{VINSEN}	EN = 5V, VINSEN = 12V	--	30	--	uA
PWM On-Time Setting						
PWM On-Time	T_{ON}	VINSEN = 12V, VID = 1.2V, R_{TONSET} = 50kΩ, Fsw=200kHz	--	500	--	ns
Minimum Off-Time	T_{OFF_MIN}	Single phase operation	--	300	--	ns
Current Senese Amplifier for Total Current Summing						
Offset Voltage	$V_{OS(EA)}$		-1	--	1	mV
Input Bias Current	I_{EA}	V_{CSP} = 1.2V, guaranteed by design	-10	--	10	nA
Maximum Sourcing Current	I_{MAXSRC}		100	--	--	uA
Gain Bandwidth Product	$G_{BW(EA)}$	Guaranteed by Design	--	10	--	MHz
Current Senese Amplifier for Phase Current Balance						
Offset Voltage	$V_{OS(EA)}$		-1	--	1	mV
Input Bias Current	I_{EA}	V_{CSPx} = 1.2V, guaranteed by design	-10	--	10	nA
Maximum Sourcing Current	I_{MAXSRC}		100	--	--	uA
Gain Bandwidth Product	$G_{BW(EA)}$	Guaranteed by Design	--	10	--	MHz
PWM Output						
Output Low Voltage	$V_{OL(PWM)}$	I_{SINK} = 4mA	--	--	0.2	V
Output High Voltage	$V_{OH(PWM)}$	I_{SOURCE} = 4mA	4.7	--	--	V
High Impedance State Leakage	I_{PWM_leak0}	V_{PWM} = 0V	-1	--	0	uA
	I_{PWM_leak1}	V_{PWM} = 5V	0	--	1	uA
Source Current	I_{PWM_SRC}	EN = 5V, during function setting period	--	10	--	uA
SVID IccMAX Register Setting						
A/D Accuracy		PWM3_IMAX and PWM2_IMAXA pin voltage = 1.51V, read SVID register 0x21h	147	151	155	DEC

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
SCLK, SDIO, ALERT#, VRHOT#						
Input Low Voltage (SCLK, SDIO)	V_{IL_SVID}		--	--	0.45	V
Input High Voltage (SCLK, SDIO)	V_{IH_SVID}		0.65	--	--	V
Pull Down Resistance (SDIO, ALERT#, VRHOT#)	R_{on_SVID}		4	--	13	Ω
Leakage Current (SCLK, SDIO, ALERT#, VRHOT#)	I_{L_SVID}		-1	--	1	uA
VR_RDY, SYSFAULT#						
Output Low Voltage	V_{OL}	$I_{SINK} = 4mA$	--	--	0.2	V
Output Leakage Current	I_L	Pull up to 5V	--	--	1	uA
Current Monitoring for Protection						
Current Mirror Accuracy		I_{SUM} to I_{CSN} ratio	95	100	105	%
Current Monitoring for Reporting						
Current Mirror Accuracy		I_{MON} to I_{CSN} ratio	95	100	105	%
IMON Resistance Range	R_{IMON}		10	--	60	kΩ
Offset Voltage	V_{IMON_OFS}	SVID register 0x15h readout = 00h	--	600	--	mV
Output Voltage	V_{IMON}	SVID register 0x15h readout = FFh	--	2100	--	mV
Current Monitoring for Droop						
Current Mirror Accuracy		I_{EAP} to I_{CSN} ratio	95	100	105	%
PROG1, PROG2, PROG3, PROG4						
Source Current	$I_{PROGSRC}$		--	40	--	uA
Leakage Current	I_{PROG_LEAK}	PROGx = 0V, after function setting period	--	--	1	uA
Thermal Monitoring						
Source Current	I_{TSENSE}	EN = 5V, R_{DRCTRL}=10kΩ	57	60	63	uA
Alert# Assert Threshold	$V_{TSENSE1}$	Temperature ADC result = 103°C	--	182	--	mV
Alert# De-Assert Threshold	$V_{TSENSE2}$	Temperature ADC result = 100°C	--	193	--	mV
VRHOT# Assert Threshold	$V_{TSENSE3}$	Temperature ADC result = 106°C	--	172	--	mV
VRHOT# De-Assert Threshold	$V_{TSENSE4}$	Temperature ADC result = 103°C	--	182	--	mV
External MOSFET Driver Enable Control						
Output Voltage High Level	V_{DRCTRL_ON}	EN = 5V, R_{DRCTRL} = 10kΩ	--	2.4	--	V
Output Voltage Low Level	V_{DRCTRL_L}	EN = 0V, R_{DRCTRL} = 10kΩ	--	0	--	V

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
MOSFET Gate Drivers						
Upper Gate Source	R_{UG_SRC}	Source current = 80mA, V_{BOOT} - V_{PH} = 12V	--	2	4	Ω
Upper Gate Sink	R_{UG_SNK}	Sink current = 80mA, V_{BOOT} - V_{PH} = 12V	--	1	2	Ω
Lower Gate Source	R_{LG_SRC}	Source current = 80mA	--	2	4	Ω
Lower Gate Sink	R_{LG_SNK}	Sink current = 80mA	--	0.8	1.6	Ω
Dead Time	T_{DT_UG-LG}	From UG < 1V to LG > 1V	--	30	--	ns
Dead Time	T_{DT_LG-UG}	From LG < 1V to UG > 1V	--	30	--	ns
Bootstrap Diode						
Forward Voltage	V_F	Forward bias current = 3.5mA	--	0.4	--	V
Over Voltage Protection						
OVP Threshold	V_{OVP}	V_{FB} - V_{EAP}	--	400	--	mV
OVP Delay Time	T_{OVP_DELAY}		--	5	--	us
Under Voltage Protection						
UVP Threshold	V_{UVP}	V_{EAP} - V_{FB}	--	400	--	mV
UVP Delay	T_{UVP_DELAY}		--	7.5	--	us
Over Current Protection						
ALERT# Assertion (SVID ICCMAX ALERT) Threshold	V_{ISUM_ALERT}	Measure ISUMx voltage	--	1.5	--	V
Total Current OCP Threshold	V_{ISUM_OCP}	Measure ISUMx voltage, full phase operation	--	1.95	--	V
Total Current OCP Delay	T_{OCP1_DELAY}		--	20	--	us
Per-Phase OCP Threshold	I_{OCP2}	Measure I_{CSNX} current	--	100	--	uA
Per-Phase OCP Delay	T_{OCP2_DELAY}		--	6	--	us
Thermal Shutdown Protection						
Thermal Shutdown Threshold	T_{OTP}	Guaranteed by Design	--	160	--	^{O}C

Package Information

VQFN7x7 - 60L

Pin 1 mark

Bottom View - Exposed Pad
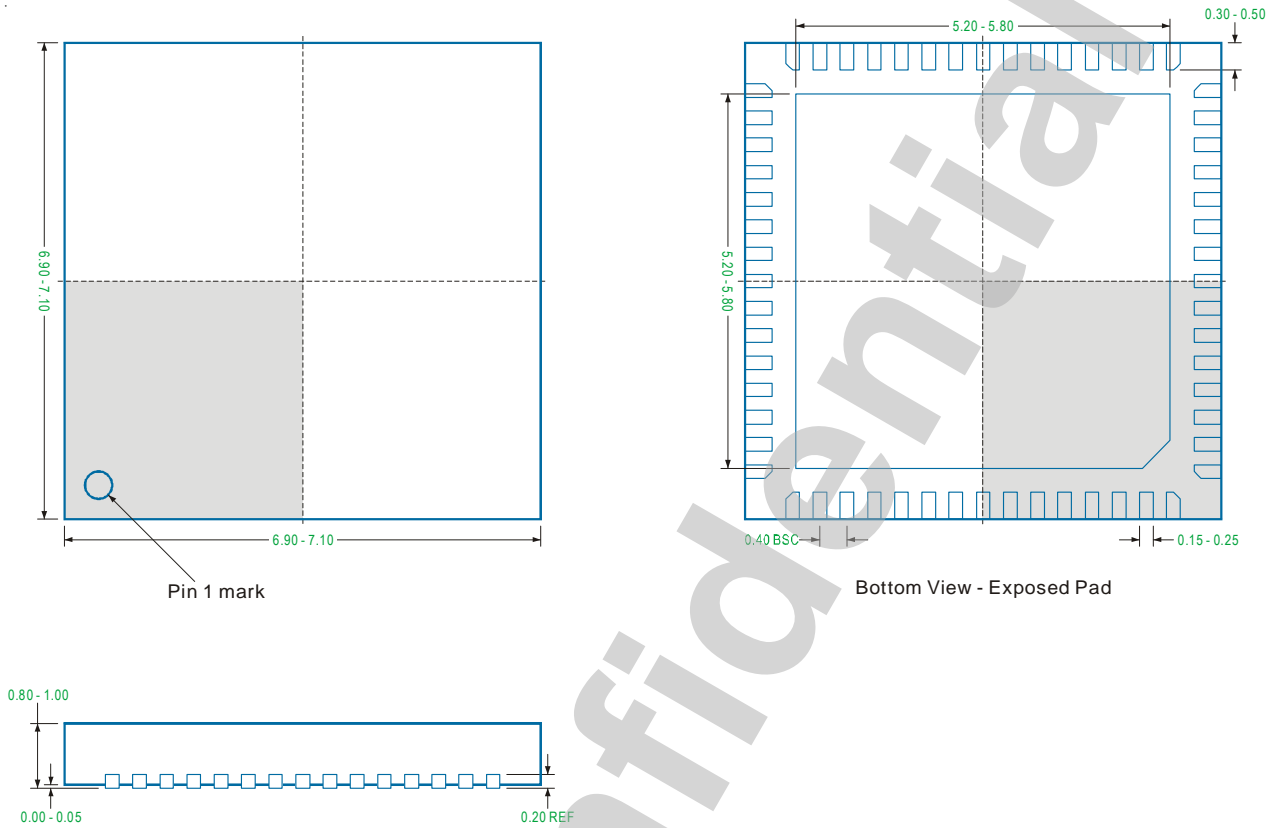
Note
1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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