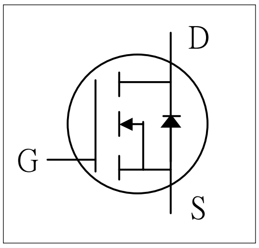
AP04N70BI-HF

Halogen-Free Product

Advanced Power Electronics Corp.

N-CHANNEL ENHANCEMENT MODE POWER MOSFET

- ▼ **100% Avalanche Test**
- ▼ **Fast Switching Characteristic**
- ▼ **Simple Drive Requirement**
- ▼ **RoHS Compliant & Halogen-Free**

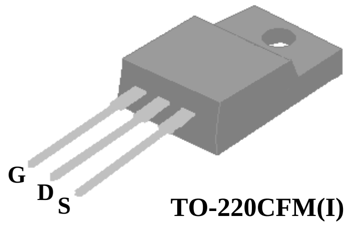


BV_{DSS}	600V
$R_{DS(ON)}$	2.4Ω
I_D [4]	4A

Description

AP04N70B series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-220CFM package is widely preferred for all commercial-industrial through hole applications. The mold compound provides a high isolation voltage capability and low thermal resistance between the tab and the external heat-sink.



TO-220CFM(I)

Absolute Maximum Ratings@T_j=25^{o}C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	600	V
V_{GS}	Gate-Source Voltage	$\pm$30	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V[4]	4	A
I_D@T_C=100℃	Drain Current, V_{GS} @ 10V[4]	2.5	A
I_{DM}	Pulsed Drain Current[1]	15	A
P_D@T_C=25℃	Total Power Dissipation	33	W
	Linear Derating Factor	0.26	W/℃
E_{AS}	Single Pulse Avalanche Energy[2]	8	mJ
I_{AR}	Avalanche Current	4	A
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	3.8	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient	65	℃/W

Electrical Characteristics@T_j=25^{o}C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=1mA	600	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25℃, I_D=1mA	-	0.6	-	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[3]	V_{GS}=10V, I_D=2A	-	-	2.4	Ω
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	2	-	4	V
g_{fs}	Forward Transconductance	V_{DS}=10V, I_D=2A	-	2.5	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=600V, V_{GS}=0V	-	-	10	uA
	Drain-Source Leakage Current (T_j=125^{o}C)	V_{DS}=480V,V_{GS}=0V	-	-	500	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=$\pm$30V, V_{DS}=0V	-	-	$\pm$100	nA
Q_g	Total Gate Charge[3]	I_D=4A	-	16.7	-	nC
Q_{gs}	Gate-Source Charge	V_{DS}=480V	-	4.1	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=10V	-	4.9	-	nC
$t_{d(on)}$	Turn-on Delay Time[3]	V_{DD}=300V	-	11	-	ns
t_r	Rise Time	I_D=4A	-	8.3	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=10Ω	-	23.8	-	ns
t_f	Fall Time	V_{GS}=10V	-	8.2	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	950	-	pF
C_{oss}	Output Capacitance	V_{DS}=25V	-	65	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	6	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current (Body Diode)	V_D=V_G=0V , V_S=1.5V	-	-	4	A
I_{SM}	Pulsed Source Current (Body Diode)[1]		-	-	15	A
V_{SD}	Forward On Voltage[3]	T_j=25℃, I_S=4A, V_{GS}=0V	-	-	1.5	V

Notes:

1.Pulse width limited by max. junction temperature

2.Starting T_j=25^{o}C , V_{DD}=50V , L=1mH , R_G=25Ω , I_{AS}=4A.

3.Pulse test

4.Ensure that the junction temperature does not exceed $T_{Jmax.}$.

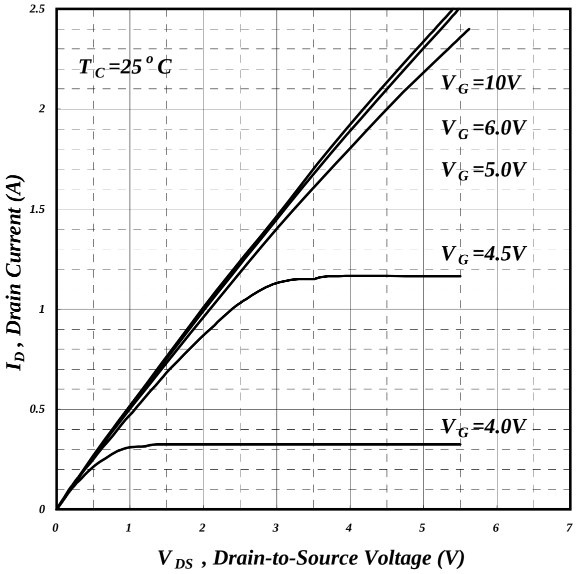


Fig 1. Typical Output Characteristics

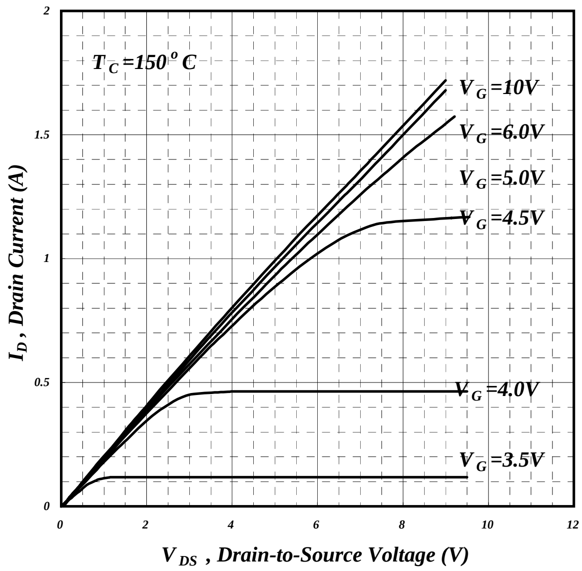


Fig 2. Typical Output Characteristics

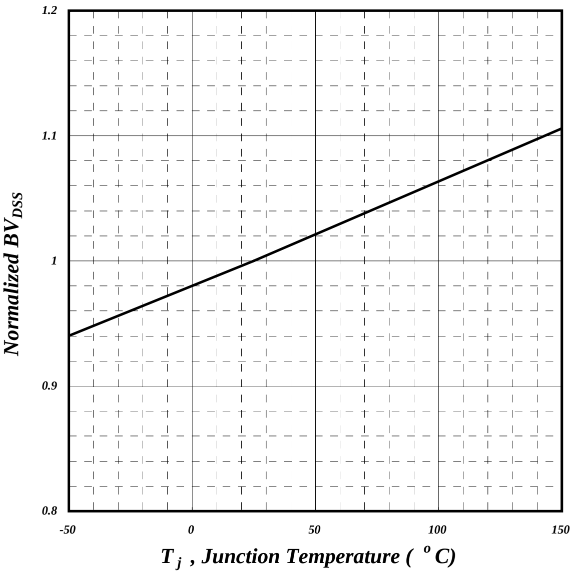


Fig 3. Normalized BV_{DSS} v.s. Junction Temperature

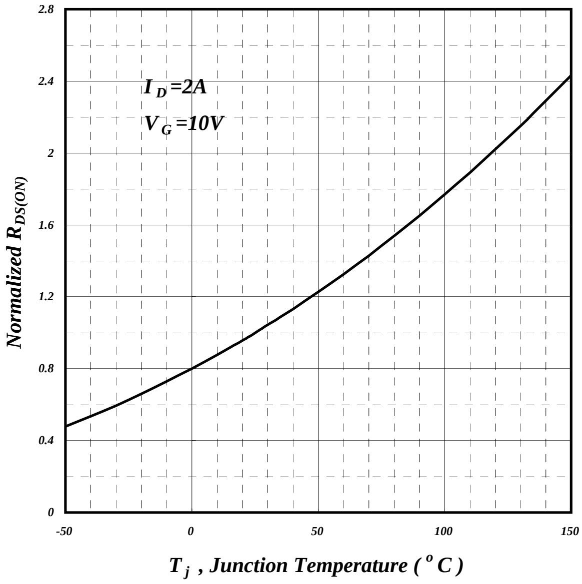


Fig 4. Normalized On-Resistance v.s. Junction Temperature

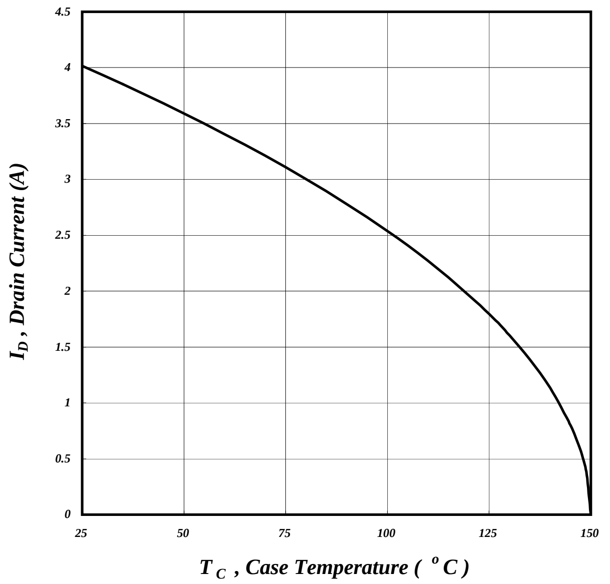


Fig 5. Maximum Drain Current v.s. Case Temperature

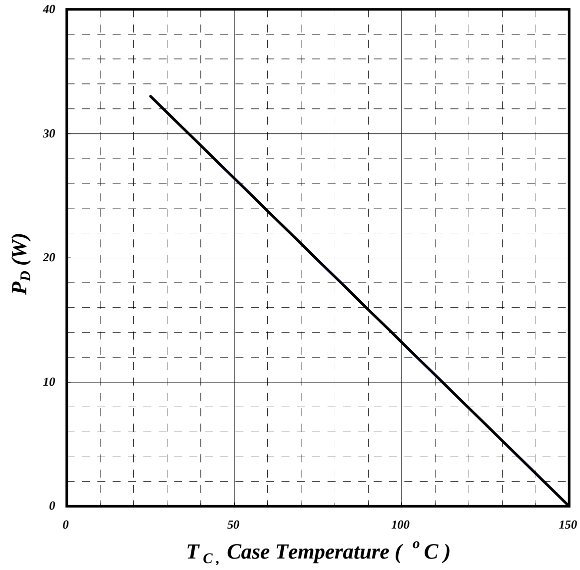


Fig 6. Typical Power Dissipation

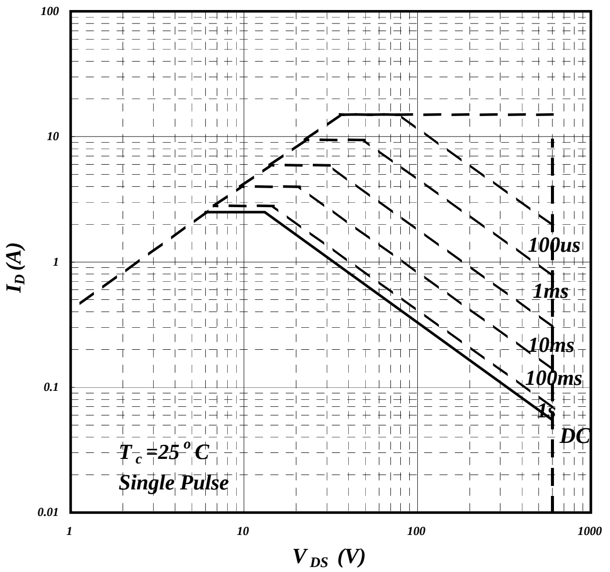


Fig 7. Maximum Safe Operating Area

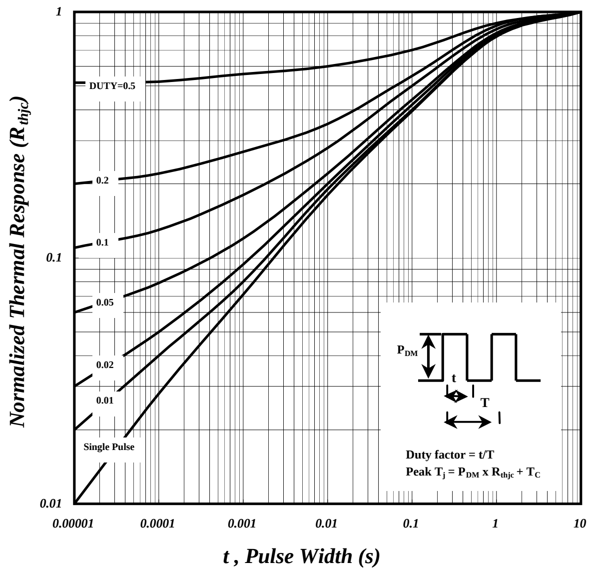


Fig 8. Effective Transient Thermal Impedance

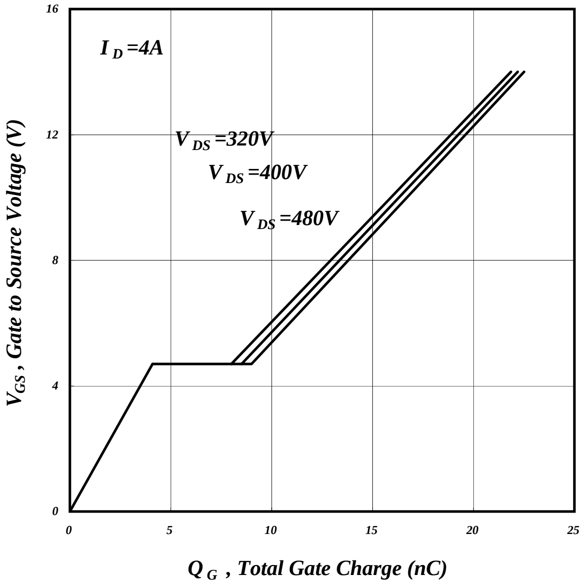


Fig 9. Gate Charge Characteristics

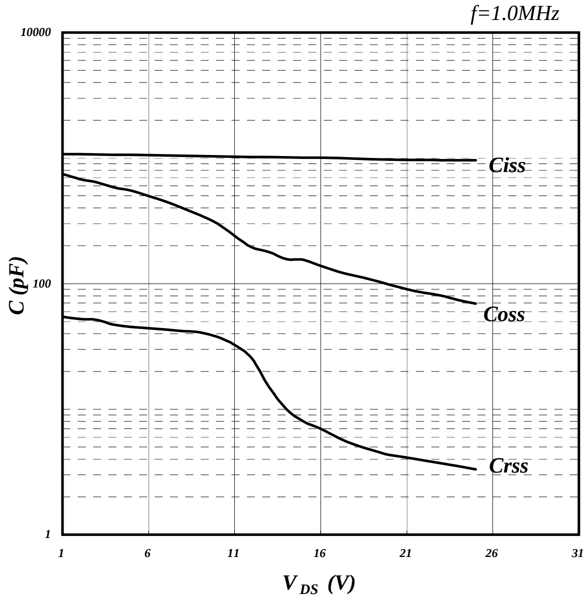


Fig 10. Typical Capacitance Characteristics

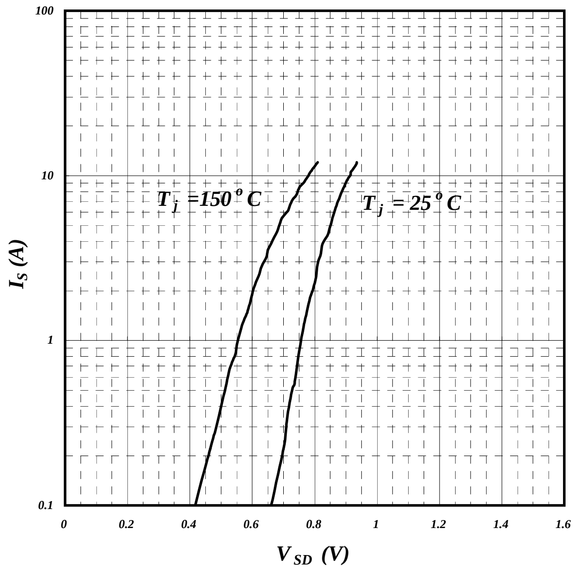


Fig 11. Forward Characteristic of Reverse Diode

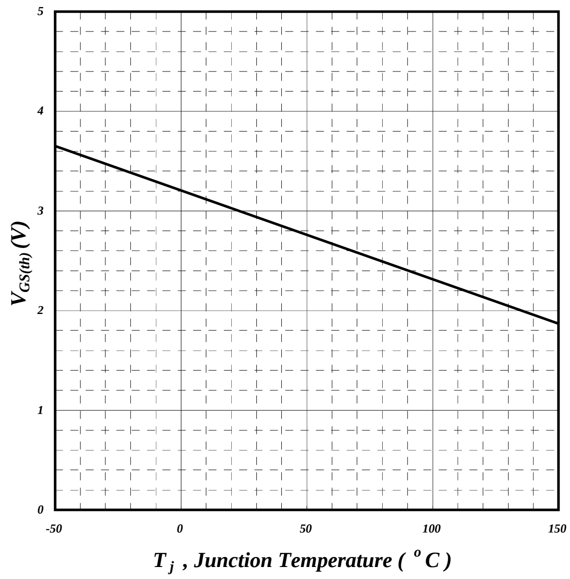


Fig 12. Gate Threshold Voltage v.s. Junction Temperature

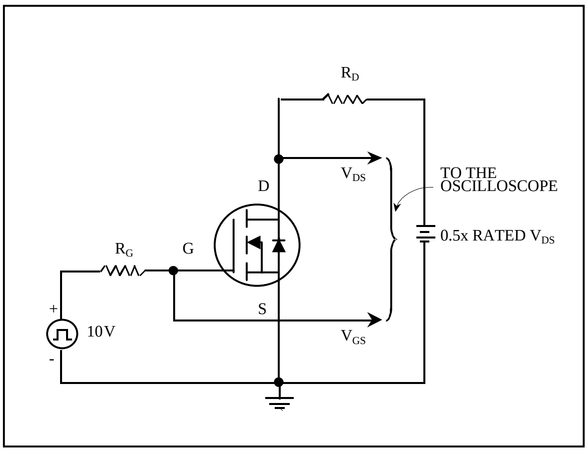


Fig 13. Switching Time Circuit

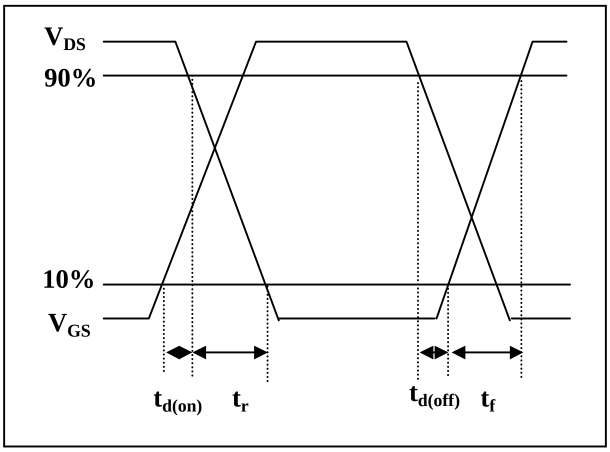


Fig 14. Switching Time Waveform

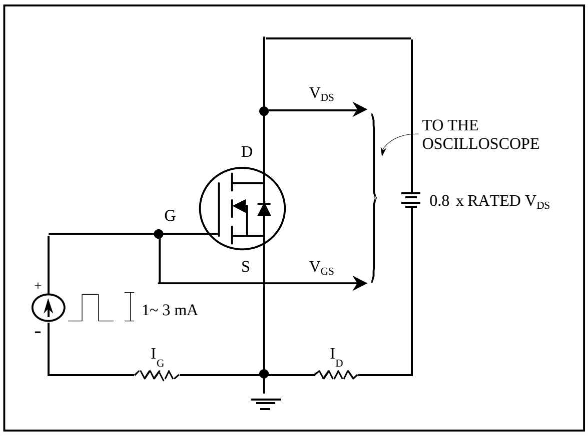


Fig 15. Gate Charge Circuit

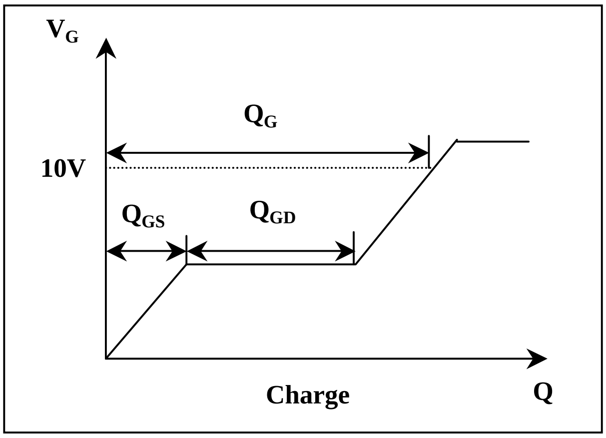


Fig 16. Gate Charge Waveform

MARKING INFORMATION