CMOS HEX VOLTAGE-LEVEL SHIFTER FOR TTL-TO-CMOS or CMOS-TO-CMOS OPERATION

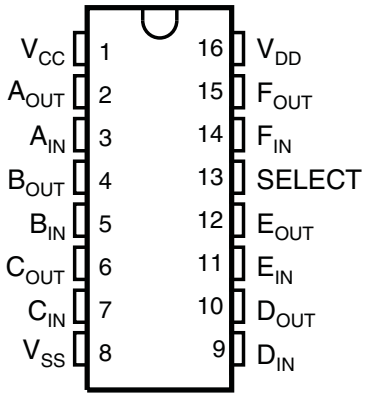
FEATURES

- **Independence of Power-Supply Sequence Considerations – V_{CC} Can Exceed V_{DD}; Input Signals Can Exceed Both V_{CC} and V_{DD}**
- **Up and Down Level-Shifting Capability**
- **Shiftable Input Threshold for Either CMOS or TTL Compatibility**
- **Standardized Symmetrical Output Characteristics**
- **100% Tested for Quiescent Current at 20 V**
- **Maximum Input Current of 1 μA at 18 V Over Full Package-Temperature Range: 100 nA at 18 V and 25°C**
- **5 V, 10 V, and 15 V Parametric Ratings**
- **Meets All Requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(TOP VIEW)



(1) Additional temperature ranges are available – contact factory

DESCRIPTION

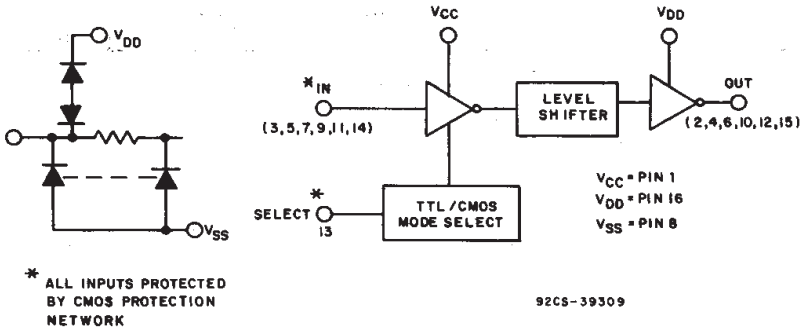
CD4504B hex voltage level-shifter consists of six circuits which shift input signals from the V_{CC} logic level to the V_{DD} logic level. To shift TTL signals to CMOS logic levels, the SELECT input is at the V_{CC} HIGH logic state. When the SELECT input is at a LOW logic state, each circuit translates signals from one CMOS level to another.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	TSSOP – PW	Reel of 2000	CD4504BMPWREP	4504BEP

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	DC supply-voltage range, voltages referenced to V_{SS} terminal		–0.5	+20	V
	Input voltage range, all inputs		–0.5	V_{CC} + 0.5	V
	DC input current, any one input			±10	mA
P_D	Power dissipation per package	T_A = –55°C to +100°C		500	mW
		T_A = +100°C to +125°C	Derate Linearly at 12 mW/°C to 200 nW		
	Device dissipation per output transistor, for TA = full package-temperature range (all package types)			100	mW
T_A	Operating temperature range		–55	+125	°C
θ_{JA}	Package thermal impedance(1)			91.1	°C/W
T_{stg}	Storage temperature range		–85	+150	°C
	Lead temperature (during soldering), at distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max			+265	°C

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

STATIC ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

CHARACTERISTIC		CONDITIONS				LIMITS AT INDICATED TEMPERATURES (°C)							UNIT
		V_O (V)	V_{IN} (V)	V_{CC} (V)	V_{CC} (V)	–55	–40	+85	+125	+25			
										MIN	TYP	MAX	
Quiescent device current, I_{DD} max and I_{CC} in CMOS-CMOS mode			0, 5	5	5	1.5	1.5	1.5	1.5		0.02	1.5	mA
			0, 10	5	10	2	2	2	2		0.02	2	
			0, 15	5	15	4	4	120	120		0.02	4	μA
			0, 20	5	20	20	20	600	600		0.04	20	
Quiescent device current, I_{CC} max TTL-CMOS mode			0, 5	5	5	5	5	6	6		2.5	5	mA
			0, 10	5	10	5	5	6	6		2.5	5	
			0, 15	5	15	5	5	6	6		2.5	5	
Output low (sink) current, I_{OL} min		0.4	0, 5		5	0.64	0.61	0.42	0.36	0.51	1		mA
		0.5	0, 10		10	1.6	1.5	1.1	0.9	1.3	2.6		
		1.5	0, 15		15	4.2	4	2.8	2.4	3.4	6.8		
Output high (source) current, I_{OH} min		4.6	0, 5		5	–0.64	–0.61	–0.42	–0.36	–0.51	–1		
		2.5	0, 5		5	–2	–1.8	–1.3	–1.15	–1.6	–3.2		
		9.5	0, 10		10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6		
		13.5	0, 15		15	–4.2	–4	–2.8	–2.4	–3.4	–6.8		
Output voltage: low-level, V_{OL} max			0, 5		5	0.05					0	0.05	V
			0, 10		10	0.05					0	0.05	
			0, 15		15	0.05					0	0.05	
Output voltage: high-level, V_{OH} min			0, 5		5	4.95				4.95	5		
			0, 10		10	9.95				9.95	10		
			0, 15		15	14.95				14.95	15		
Input low voltage, V_{IL} max[1]	TTL-CMOS	1		5	10	0.8						0.8	
	TTL-CMOS	1		5	15	0.8						0.8	
	CMOS-CMOS	1		5	10	1.5						1.5	
	CMOS-CMOS	1.5		5	15	1.5						1.5	
	CMOS-CMOS	1.5		10	15	3						3	
Input high voltage, V_{IH} min[1]	TTL-CMOS	9		5	10	2				2			
	TTL-CMOS	13.5		5	15	2				2			
	CMOS-CMOS	9		5	10	3.5				3.5			
	CMOS-CMOS	13.5		5	15	3.5				3.5			
	CMOS-CMOS	13.5		10	15	7				7			
Input current, I_{IN} max			0, 18		18	±0.1	±0.1	±1	±1		$±10^{-5}$	±0.1	μA

(1) Applies to the six input signals. For mode control (P13), only the CMOS-CMOS ratings apply.

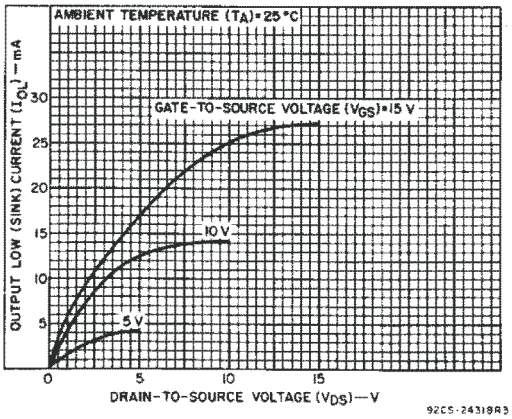


Figure 1. Typical Output Low (sink) Current Characteristics

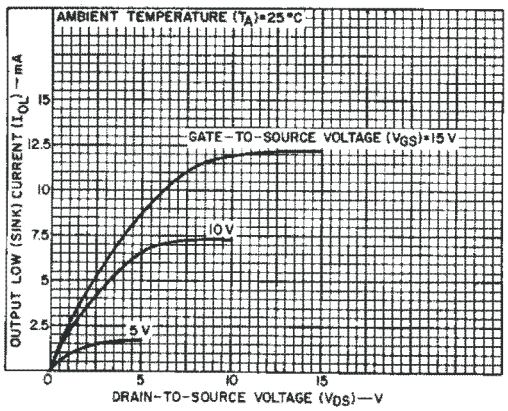


Figure 2. Minimum Output Low (sink) Current Characteristics

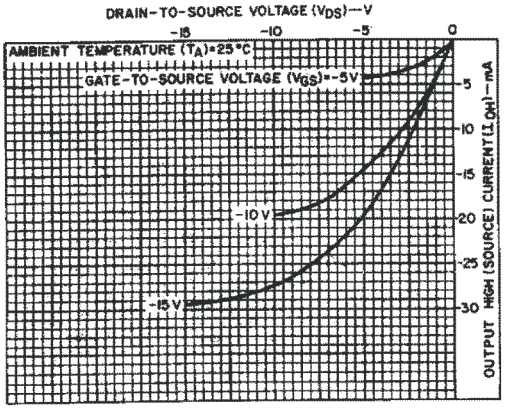


Figure 3. Typical Output High (source) Current Characteristics

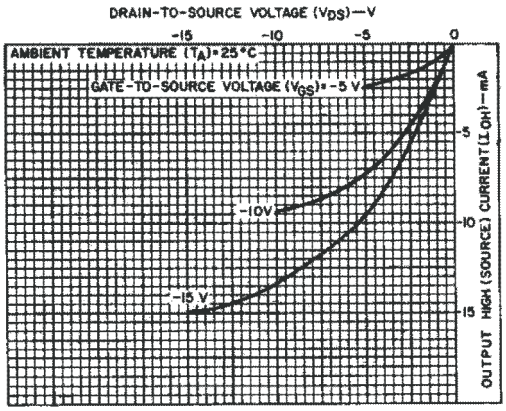


Figure 4. Minimum Output High (source) Current Characteristics

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		MIN	MAX	UNIT
V_{DD}	Supply-voltage range (for T_A = full package temperature range)	5	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS

T_A = 25°C, Input t_r,t_f = 20 ns, C_L = 50 pF, R_L = 200 Ω

CHARACTERISTIC		SHIFTING MODE	V_{CC} (V)	V_{DD} (V)	LIMITS TYP	LIMITS MAX	UNIT
t_{PHL}	Propagation delay: high-to-low,	TTL to CMOS $V_{DD} > V_{CC}$	5	10	140	280	ns
			5	15	140	280	
		CMOS to CMOS $V_{DD} > V_{CC}$	5	10	120	240	
			5	15	120	240	
			10	15	70	140	
		CMOS to CMOS $V_{CC} > V_{DD}$	10	5	275	550	
			15	5	275	550	
			15	10	70	140	
t_{PLH}	Propagation delay: low-to-high	TTL to CMOS $V_{DD} > V_{CC}$	5	10	140	280	ns
			5	15	140	280	
		CMOS to CMOS $V_{DD} > V_{CC}$	5	10	120	240	
			5	15	120	240	
			10	15	70	140	
		CMOS to CMOS $V_{CC} > V_{DD}$	10	5	200	400	
			15	5	200	400	
			15	10	60	120	
t_{THL}, t_{TLH}	Transition time	All modes		5	100	200	ns
				10	50	100	
				15	40	80	
C_{IN}	Input capacitance	Any input			5	7.5	pF

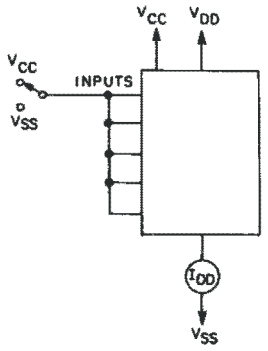


Figure 5. Quiescent Device Current

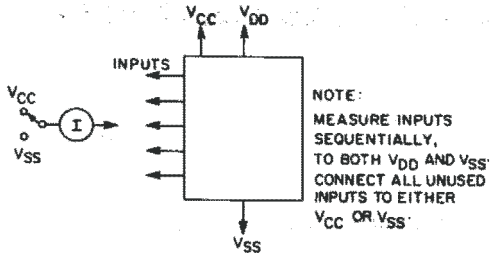


Figure 6. Input Current

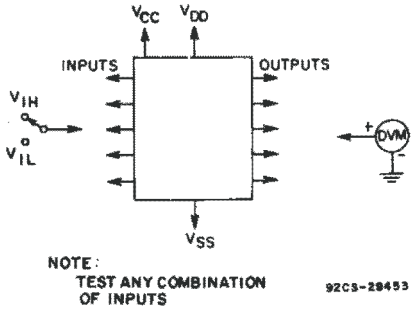


Figure 7. Input Voltage

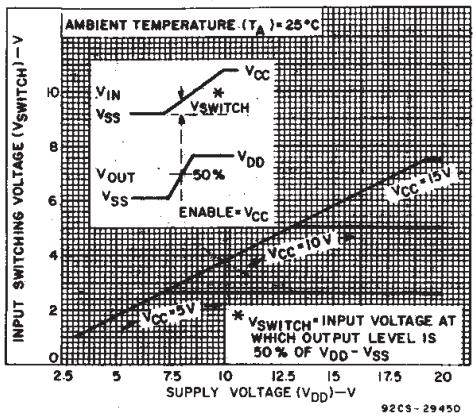


Figure 8. Typical Input Switching as a Function of High-Level Supply Voltage (SELECT at V_{CC} – CMOS Mode

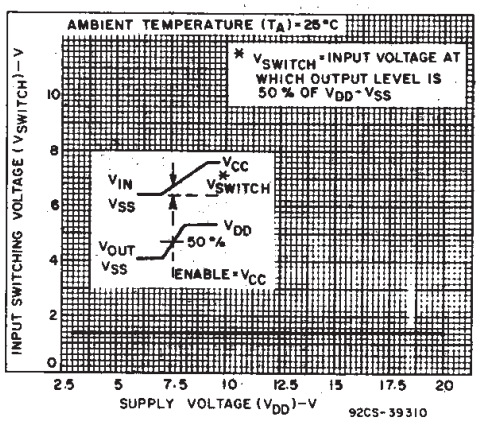


Figure 9. Typical Input Switching as a Function of High-Level Supply Voltage (SELECT at V_{SS} – TTL Mode)

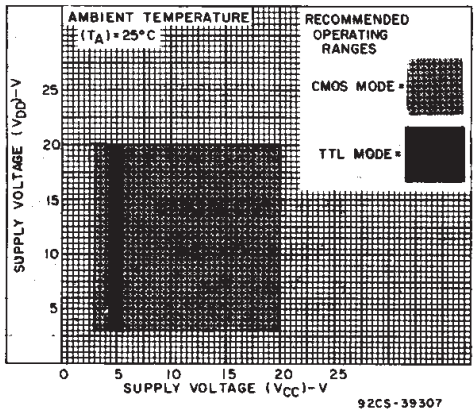
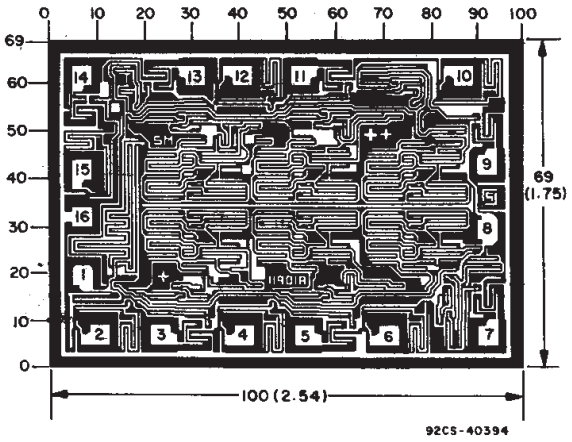


Figure 10. High-Level Supply Voltage vs. Low-Level Supply Voltage



A. Dimensions in parentheses are in millimeters and are derived form the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Figure 11. Dimensions and Pad Layout

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4504BMPWREP	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	4504BEP	Samples
V62/09606-01XE	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	4504BEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4504B-EP :

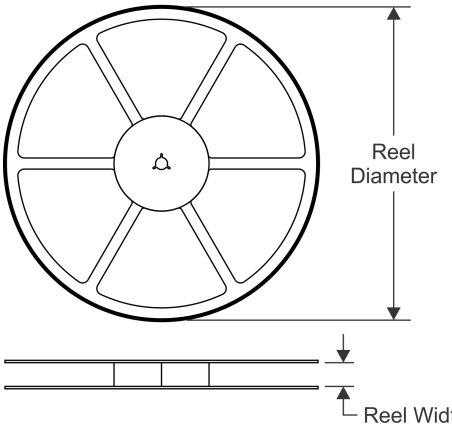
- Catalog: CD4504B
- Military: CD4504B-MIL

NOTE: Qualified Version Definitions:

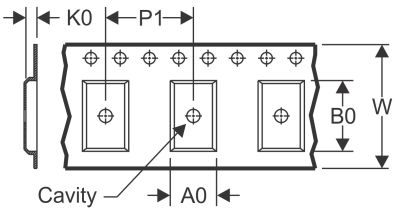
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

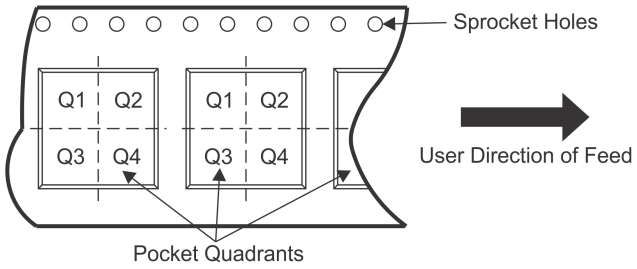


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

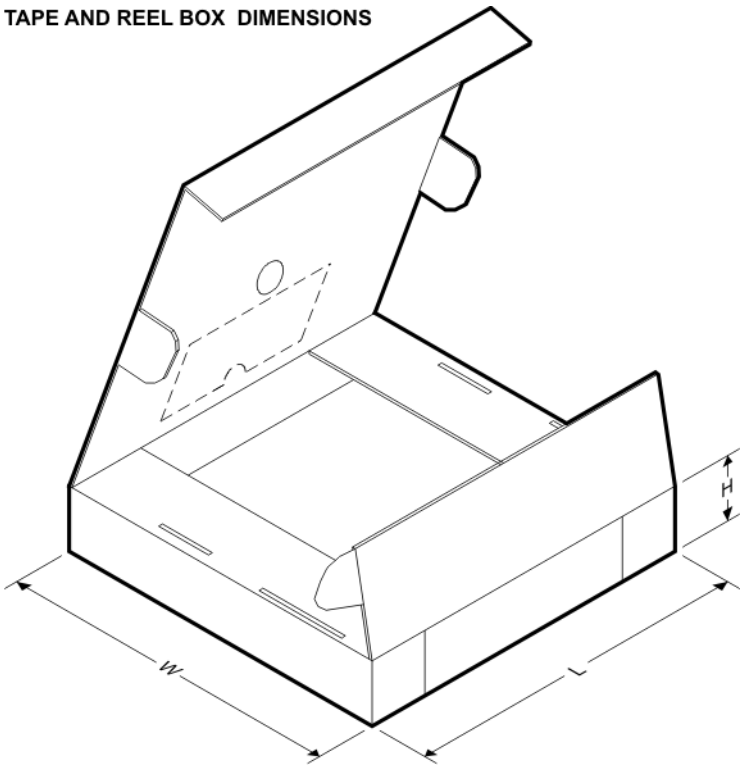
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4504BMPWREP	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

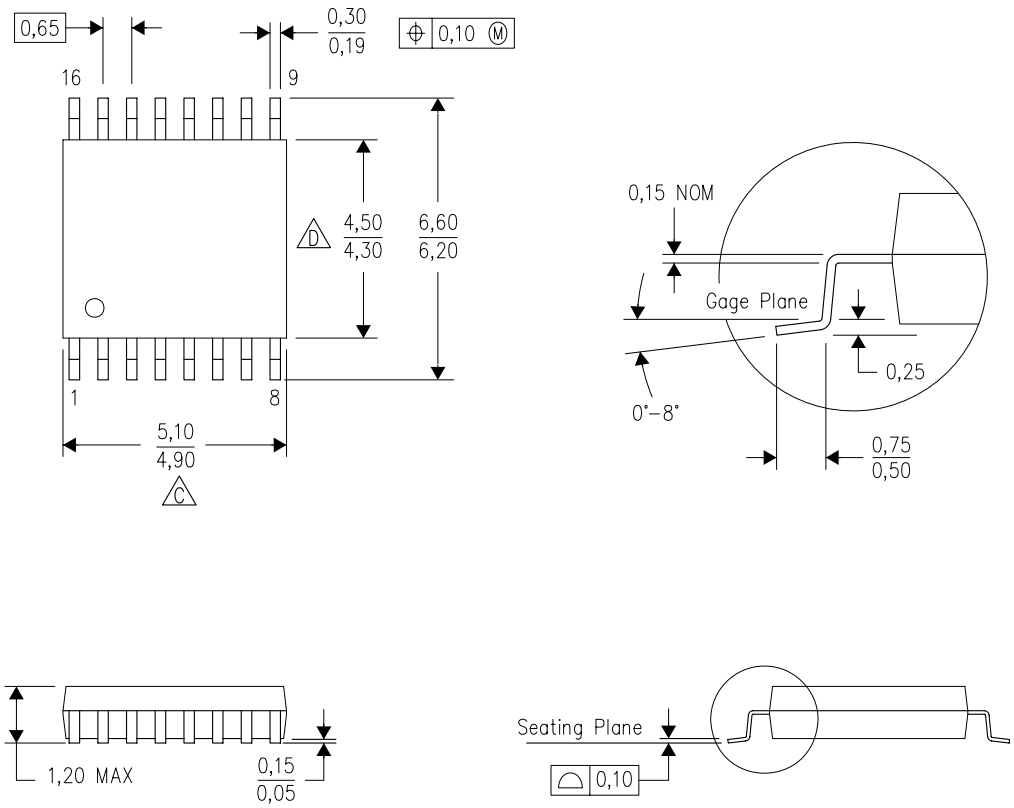
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4504BMPWREP	TSSOP	PW	16	2000	367.0	367.0	35.0

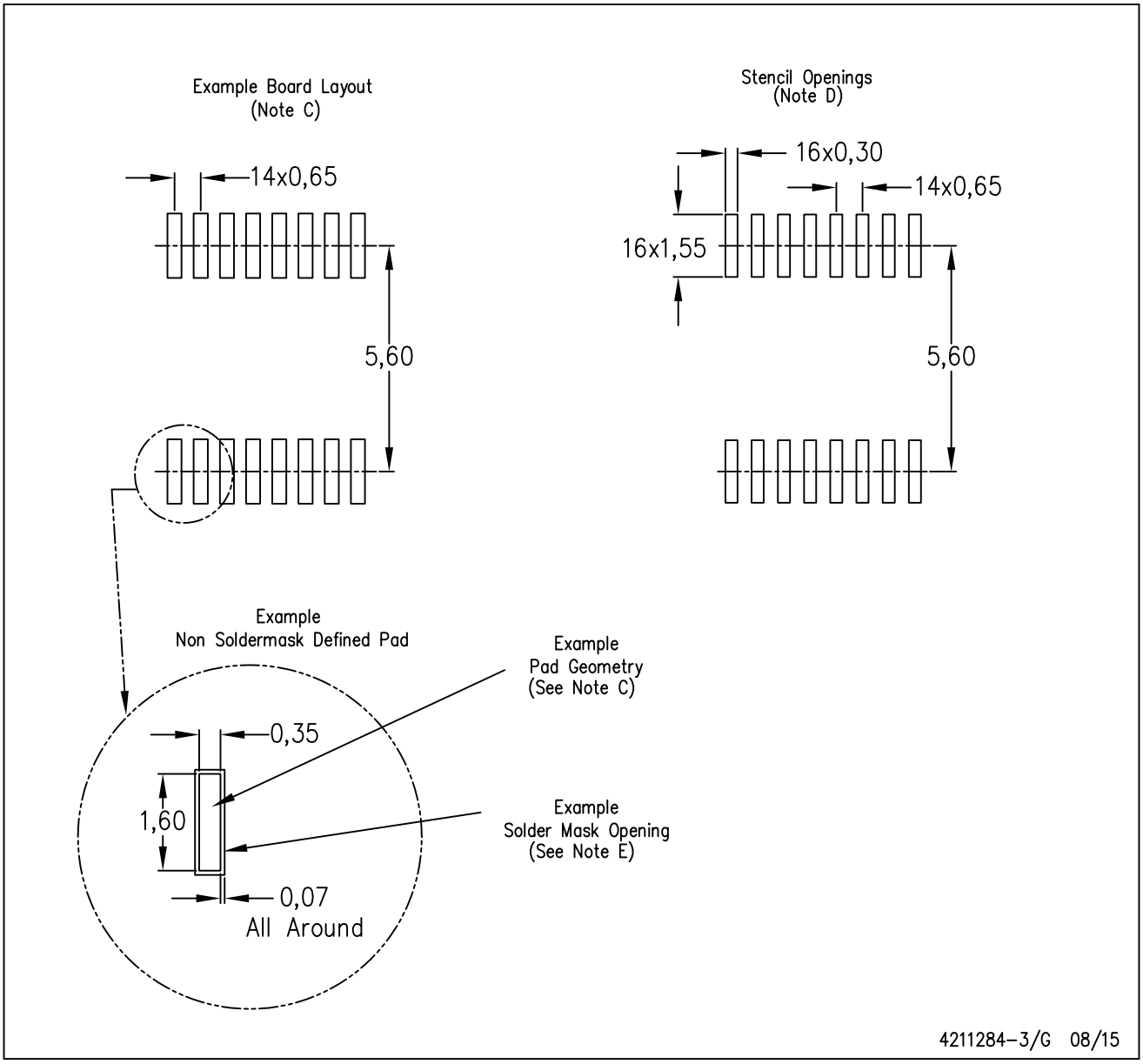
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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