DS100BR111 Ultra Low Power 10.3 Gbps 2-Channel Repeater with Input Equalization and Output De-Emphasis

Check for Samples: DS100BR111

FEATURES

- **Two channel repeaters for up to 10.3 Gbps**
  - **DS100BR210 : 2x unidirectional channels**
  - **DS100BR111 : 1x bidirectional lane**
- **10G-KR bi-directional interface compatibility**
  - **Allows for back-channel communication and training**
- **Low 65mW/channel (typical) power consumption, with option to power down unused channels**
- **Advanced signal conditioning features**
  - **Receive equalization up to +36 dB**
  - **Transmit de-emphasis up to -12 dB**
  - **Transmit VOD control: 700 to 1200 mVp-p**
  - **< 0.3 UI of residual DJ at 10 Gbps**
- **Programmable via pin selection, EEPROM or SMBus interface**
- **Single supply operation selectable: 2.5V or 3.3v**
- **Flow-thru pinout in 4mmx4mm 24-pin leadless WQFN package**
- **>5kV HBM ESD rating**
- **Industrial -40 to 85°C operating temperature range**

APPLICATIONS

- **High-speed active copper cable modules and FR-4 backplane in communication systems**
- **10GE, 10G-KR, FC, SAS, SATA 3/6 Gbps (with OOB detection), InfiniBand, CPRI, RXAUI and many others.**

DESCRIPTION

The DS100BR111 is an extremely low power, high performance dual-channel repeater for serial links with data rates up to 10.3 Gbps. The DS100BR111 pinout is configured as one bidirectional lane (one transmit, one receive channel).

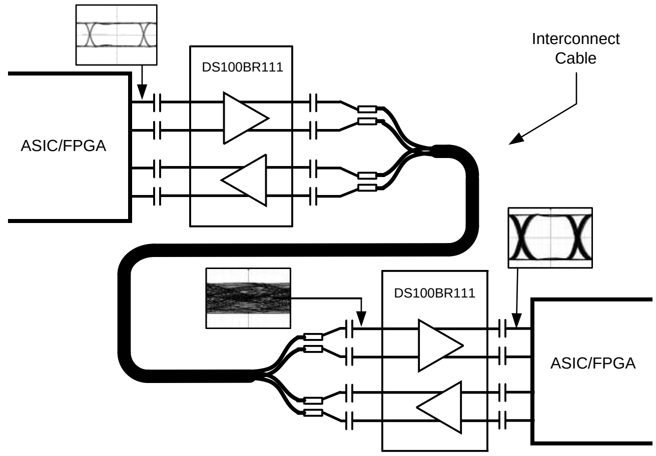
The DS100BR111 inputs feature a powerful 4-stage continuous time linear equalizer (CTLE) to provide a boost of up to +36 dB at 5 GHz and open an input eye that is completely closed due to inter-symbol interference (ISI) induced by the interconnect mediums such as an FR-4 backplane or AWG-30 cables. The transmitter features a programmable output de-emphasis driver with up to -12 dB and allows amplitude voltage levels to be selected from 700 mVp-p to 1200 mVp-p to suit multiple application scenarios.

When configured as a 10G-KR repeater, the DS100BR111 allows the KR host and the end point to optimize the full link by adjusting transmit and receive equalizer coefficients using back-channel communication techniques specified by the 802.3ap standard.

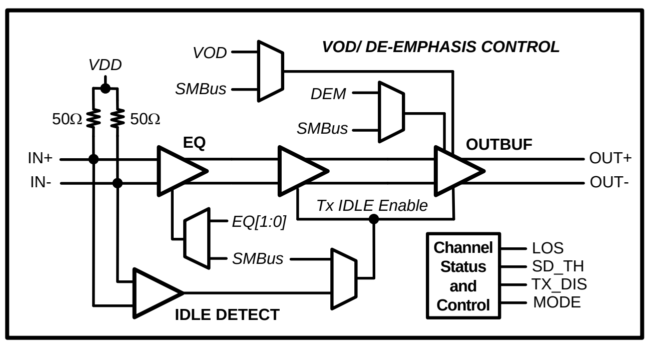
The programmable settings can be applied via pin contol, SMBus (I2C) protocol or an external EEPROM. When operating in the EEPROM mode, the configuration information is automatically loaded on power up – This eliminates the need for an external microprocessor or software driver.

Part of National's PowerWise family of energy efficient devices, the DS100BR111 consumes just 65 mW/channel (typical), and allow the option to turn-off unused channels. This ultra low power consumption eliminates the need for external heat sinks and simplifies thermal management in active cable applications.

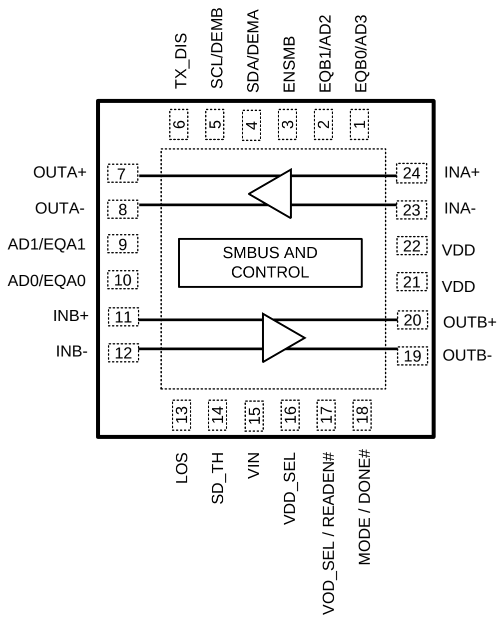
Typical Application



Block Diagram - Detail View Of Channel (1 Of 2)



Pin Diagram



(1) The center DAP on the package bottom is the device GND connection. This pad must be connected to GND through multiple (minimum of 4) vias to ensure optimal electrical and thermal performance.

Figure 1. DS100BR111 Pin Diagram 24 lead

Pin Descriptions[1]

Pin Name	Pin Number	I/O, Type	Pin Description
Differential High Speed I/O's			
INA+, INA- , INB+, INB-,	24, 23 11, 12	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. A on-chip 50Ω termination resistor connects INx+ to VDD and INx- to VDD.
OUTA+, OUTA-, OUTB+, OUTB-,	7, 8 20, 19	O,CML	Inverting and non-inverting 50Ω driver outputs with de-emphasis. Compatible with AC coupled CML inputs.
Control Pins			
ENSMB	3	I, LVCMOS Float	System Management Bus (SMBus) enable pin Tie HIGH = Register Access, SMBus Slave mode FLOAT = SMBus Master read from External EEPROM Tie LOW = External Pin Control Mode
ENSMB = 1 (SMBUS MODE)			
SCL	5	I, LVCMOS O, Open Drain	ENSMB Master or Slave mode SMBUS clock input pin is enabled. A clock input in Slave mode. Can also be a clock output in Master mode.
SDA	4	I, LVCMOS, O, Open Drain	ENSMB Master or Slave mode The SMBus bidirectional SDA pin is enabled. Data input or open drain (pull-down only) output.
AD0-AD3	10, 9, 2, 1	I, LVCMOS, Float (4-Levels)	ENSMB Master or Slave mode SMBus Slave Address Inputs. In SMBus mode, these pins are the user set SMBus slave address inputs. There are 16 addresses supported by these pins. Pins must be tied LOW or HIGH when used to define the device SMBus address. [2]
READEN#	17	I, LVCMOS	When using an External EEPROM, a transition from high to low starts the load from the external EEPROM
DONE#	18	IO, LVCMOS, Float (4-Levels)	EEPROM Download Status HIGH indicates Error / Still Loading LOW indicates download complete. No Error.
ENSMB = 0 (PIN MODE)			
EQA0, EQA1 EQB0, EQB1	10, 9 1, 2	I, LVCMOS, Float (4-Levels)	EQA/B ,0/1 control the level of equalization of each channel. The EQA/B pins are active only when ENSMB is de-asserted (LOW). When ENSMB goes high the SMBus registers provide independent control of each lane, and the EQB0/B1 pins are converted to SMBUS AD2/AD3 inputs. Table 2
DEMA, DEMB	4, 5	IO, LVCMOS, Float (4-Levels)	DEMA/B controls the level of de-emphasis. The DEMA/B pins are only active when ENSMB is de-asserted (LOW). Each of the 4 A/B channels have the same level unless controlled by the SMBus control registers. When ENSMB goes high the SMBus registers provide independent control of each lane and the DEM pins are converted to SMBUS SCL and SDA pins. Table 3
TX_DIS	6	I, LVCMOS	DS100BR111 High = OUTA Enabled /OUTB Disabled Low = OUTA/B Enabled
VOD_SEL	17	I, LVCMOS, Float (4-Levels)	EQ Mode and VOD select. High = 10G-KR Mode (VOD = 1.1V/1.3V) Float = (VOD = 1.0 V) 20K = (VOD = 1.2 V) Low = (VOD = 700m V) See[2][3]. See Table 4 for additional information.
VDD_SEL	16	I, Internal Pull-up	Enables the 3.3V to 2.5V internal regulator Low = 3.3 V Operation Float = 2.5 V Operation

(1) LVCMOS inputs without the “Float” conditions must be driven to a logic low or high at all times or operation is not guaranteed. Unless the "Float" level is desired; 4-Level input pins require a minimum 1K resistor to GND, VDD (in 2.5V mode), or VIN (in 3.3V mode).Input edge rate for LVCMOS/FLOAT inputs must be faster than 50 ns from 10–90%.
(2) Setting VOD_SEL = High in SMBus Mode will force the SMBus Address = B0'h
(3) DS100BR111 OUTA is limited to 700mV in pin mode.

Pin Descriptions[1] (continued)

Pin Name	Pin Number	I/O, Type	Pin Description
MODE	18	I, LVCMOS	Controls Device Mode of Operation High = Continuous Talk Float = 10G-KR Mode, Slow OOB 20KΩ = eSATA Mode, Fast OOB, Auto Low Power on 100 uS of inactivity. SD stays active. Low = SAS Mode, Fast OOB
Status Output			
LOS	13	O, Open Drain	Indicates Loss of Signal (Default is LOS on INA). Can be modified via SMBus registers.
LOS Threshold Input			
SD_TH	14	I, LVCMOS, Float (4-Levels)	The SD_TH pin controls LOS threshold setting; Assert (mV), Deassert (mV) 20K = 160 mV, 100 mV Float = 180 mV, 110 mV (Default) High = 190 mV, 130 mV Low = 210 mV, 150 mV[4]
Power			
VDD	21, 22	Power	Power supply pins 2.5V mode connect to 2.5V 3.3V mode do not connect to any supply voltage. Should be used to attach external decoupling to device, 100 - 200 nF recommended. See Applications Information section for additional information.
VIN	15	Power	VIN = 3.3V +/-10% (input to internal LDO regulator)[5] See Applications Information section for additional information.
GND	DAP	Power	Ground pad (DAP - die attach pad).
For additional information Table 1 Table 5 .			

(4) Using values less than the default level can extend the time required to detect LOS and are not recommended.
(5) Must FLOAT for 2.5V operation.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage (VDD)		-0.5V to +2.75V
Supply Voltage (VIN)		-0.5V to +4.0V
LVCMOS Input/Output Voltage		-0.5V to +4.0V
CML Input Voltage		-0.5V to (VDD+0.5)
CML Input Current		-30 to +30 mA
Junction Temperature		125°C
Storage Temperature		-40°C to +125°C
ESD Rating	HBM, STD - JESD22-A114F	> 5 kV
	MM, STD - JESD22-A115-A	100 V
	CDM, STD - JESD22-C101-D	1250 V
Package Thermal Resistance	θJC	3.2°C/W
	θJA, No Airflow, 4 layer JEDEC	33.0°C/W
For soldering specifications: See product folder at www.national.com www.national.com/ms/MS/MS-SOLDERING.pdf		

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied.

Recommended Operating Conditions (1)

	Min	Typ	Max	Units
Supply Voltage (2.5V mode)	2.375	2.5	2.625	V
Supply Voltage (3.3V mode)	3.0	3.3	3.6	V
Ambient Temperature	-40	25	+85	°C
SMBus (SDA, SCL)			3.6	V

(1) The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are guaranteed for a junction temperature range of -40°C to +125°C. Models are validated to Maximum Operating Voltages only.

Electrical Characteristics

Parameter		Test Conditions	Min	Typ	Max	Units
Power Supply Current						
IDD	Supply Current	TX_DIS = LOW, EQ = ON VOD_SEL = Float (1000 mV)		50	63	mA
		Auto Low Power Mode TX_DIS = LOW, MODE = 20K VID CHA and CHB = 0.0V VOD_SEL = Float (1000 mV)		12	15	
		TX_DIS = HIGH (BR111)		25	35	
LVCMOS DC Specifications						
V_{IH}	High Level Input Voltage		2.0		VDD	V
V_{IL}	Low Level Input Voltage		GND		0.7	V
V_{OH}	High Level Output Voltage	I_{OH} = -4.0 mA (1)	2.0			V
V_{OL}	Low Level Output Voltage	I_{OL} = 4.0 mA			0.4	V

(1) VOH only applies to the DONE# pin; LOS, SCL, and SDA are open-drain outputs that have no internal pull-up capability. DONE# is a full LVCMOS output with pull-up and pull-down capability

Electrical Characteristics (continued)

Parameter		Test Conditions	Min	Typ	Max	Units
I_{IN}	Input Leakage Current	Vinput = 0V or VDD VDD_SEL = Float	-15		+15	µA
		Vinput = 0V or VIN VDD_SEL = Low	-15		+15	
I_{IN-P}	Input Leakage Current 4-Level Input (2)	Vinput = 0V or VDD - 0.05V VDD_SEL = Float Vinput = 0V or VIN - 0.05V VDD_SEL = Low	-160		+80	µA
LOS and ENABLE / DISABLE Timing						
T_{LOS_OFF}	Input IDLE to Active RX_LOS response time	See (3)		0.035		µS
T_{LOS_ON}	Input Active to IDLE RX_LOS response time	See (3)		0.4		µS
T_{OFF}	TX Disable assert Time TX_DIS = HIGH to Output OFF	See (3)		0.005		µS
T_{ON}	TX Disable negateTime TX_DIS = LOW to Output ON	See (3)		0.150		µS
T_{LP_EXIT}	Auto Low Power Exit ALP to Normal Operation	See (3)		150		nS
T_{LP_ENTER}	Auto Low Power Enter Normal Operation to Auto Low Power	See (4)		100		uS
CML Receiver Inputs						
V_{TX}	Source Transmit Launch Signal Level	Default power-up conditions ENSMB = 0 or 1	190	800	1600	mV
RL_{RX-IN}	RX return loss	SDD11 @ 4.1 GHz		-12		dB
		SDD11 @ 11.1 GHz		-8		
		SCD11 @ 11.1 GHz		-10		
High Speed Transmitter Outputs						
V_{OD1}	Output Voltage Differential Swing	OUT+ and OUT- AC coupled and terminated by 50Ω to GND VOD_SEL = LOW (700 mV setting) DE = LOW	500	650	800	mVp-p
V_{OD2}	Output Voltage Differential Swing	OUT+ and OUT- AC coupled and terminated by 50Ω to GND VOD_SEL = FLOAT (1000 mV setting) DE = LOW	800	1000	1100	
V_{OD3}	Output Voltage Differential Swing	OUT+ and OUT- AC coupled and terminated by 50Ω to GND VOD_SEL = 20K (1200 mV setting) DE = LOW	950	1150	1350	
V_{OD_DE1}	De-Emphasis Levels	OUT+ and OUT- AC coupled and terminated by 50Ω to GND VOD_SEL = FLOAT (1000 mV setting) DE = FLOAT		-3		dB

(2) Input is held to a maximum of 50 mV below VDD or VIN to simulate the use of a 1K resistor on the input.
(3) Parameter not tested in production.
(4) Parameter not tested in production.

Electrical Characteristics (continued)

Parameter		Test Conditions	Min	Typ	Max	Units
V_{OD_DE2}	De-Emphasis Levels	OUT+ and OUT- AC coupled and terminated by 50Ω to GND VOD_SEL = FLOAT (1000 mV setting) DE = 20K		-6		dB
V_{OD_DE3}	De-Emphasis Levels	OUT+ and OUT- AC coupled and terminated by 50Ω to GND VOD_SEL = FLOAT (1000 mV setting) DE = HIGH		-9		dB
$V_{CM\text{-}AC}$	Output Common-Mode Voltage	AC Common Mode Voltage DE = 0 dB, VOD <= 1000 mV		4.5		mV (RMS)
$V_{CM\text{-}DC}$	Output DC Common-Mode Voltage	DC Common Mode Voltage	0	1.1	1.9	V
V_{IDLE}	TX IDLE Output Voltage				30	mV
$RL_{TX\text{-}DIFF}$	TX return loss	SDD22 @ 4.1 GHz		-13		dB
		SDD22 @ 11.1 GHz		-9		
		SCC22 @ 2.5 GHz		-22		
		SCC22 @ 11.1 GHz		-10		
delta Z_M	Transmitter Termination Mismatch	DC, I_{FORCE} = +/- 100 µA [(5)]		2.5		%
$T_{R/F}$	Transmitter Rise and Fall Time	Measurement points at 20% - 80% [(6)]		38		ps
T_{PD}	Propagation Delay	Measured at 50% crossing EQ = 00		230		ps
T_{CCSK}	Channel to Channel Skew	T = 25°C, VDD = 2.5V		7		ps
T_{PPSK}	Part to Part Skew	T = 25°C, VDD = 2.5V		20		ps
$T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$	Max time to transition to idle after differential signal	VIN = 1Vpp, 10 Gbps EQ = 00, DE = 0		6.5		ns
$T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$	Max time to transition to valid differential signal after idle	VIN = 1Vpp, 10 Gbps EQ = 00, DE = 0		3.2		ns
$T_{ENV\_DISTORT}$	Active OOB timing distortion, input active time vs. output active time			3.3		ns
Output Jitter Specifications: [(7)]						
R_J	Random Jitter	No Media Source Amplitude = 700 mV, PRBS15 pattern, 10.3125 Gbps VOD = Default, EQ = minimum, DE = 0 dB		0.3		ps (RMS)
D_{J1}	Deterministic Jitter			0.09		UI
Equalization						
D_{JE1}	Residual Deterministic Jitter 10.3125 Gbps	8 meter 30AWG Cable on Input Source = 700 mV, PRBS15 pattern EQ = 0F'h; See Figure 16		0.27		UI

(5) Force +/- 100 uA on output, measure delta V on the Output and calculate impedance. Mismatch is the percentage difference of OUTn+ and OUTn- impedance driving the same logic state.
(6) Default VOD used for testing. DE = -1.5 dB level used to compensate for fixture attenuation.
(7) Typical jitter reported is determined by jitter decomposition software on the DSA8200 Oscilloscope.

Electrical Characteristics (continued)

Parameter		Test Conditions	Min	Typ	Max	Units
D_{JE2}	Residual Deterministic Jitter 10.3125 Gbps	30" 4-mil FR4 on Inputs Source = 700 mV, PRBS15 pattern EQ = 16'h; See Figure 13		0.17		UI
De-emphasis						
D_{JD1}	Residual Deterministic Jitter 10.3125 Gbps	10” 4 mil stripline FR4 on Outputs Source = 700 mV, PRBS15 pattern EQ = Min, VOD = 1200 mV, DE = 010'b See Figure 18		0.13		UI

Electrical Characteristics — Serial Management Bus Interface

Over recommended operating supply and temperature ranges unless other specified.

Parameter		Test Conditions	Min	Typ	Max	Units
Serial Bus Interface DC Specifications: (1)						
V_{IL}	Data, Clock Input Low Voltage				0.8	V
V_{IH}	Data, Clock Input High Voltage		2.1		3.6	V
I_{PULLUP}	Current Through Pull-Up Resistor or Current Source	High Power Specification	4			mA
V_{DD}	Nominal Bus Voltage		2.375		3.6	V
$I_{LEAK\text{-}Bus}$	Input Leakage Per Bus Segment	See (2)	-200		+200	µA
C_I	Capacitance for SDA and SCL	See (2) (3) (4)			10	pF
R_{TERM}	External Termination Resistance pull to V_{DD} = 2.5V ± 5% OR 3.3V ± 10%	Pullup V_{DD} = 3.3V, (2) (3) (5)		2000		Ω
		Pullup V_{DD} = 2.5V, (2) (3) (5)		1000		Ω
Serial Bus Interface Timing Specifications						
FSMB	Bus Operating Frequency	ENSMB = VDD (Slave Mode)			400	kHz
		ENSMB = FLOAT (Master Mode (1)	280	400	520	kHz
TBUF	Bus Free Time Between Stop and Start Condition		1.3			µs
THD:STA	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	At I_{PULLUP}, Max	0.6			µs
TSU:STA	Repeated Start Condition Setup Time		0.6			µs
TSU:STO	Stop Condition Setup Time		0.6			µs
THD:DAT	Data Hold Time		0			ns
TSU:DAT	Data Setup Time		100			ns
T_{LOW}	Clock Low Period		1.3			µs
T_{HIGH}	Clock High Period	See (6)	0.6		50	µs
t_F	Clock/Data Fall Time	See (6)			300	ns
t_R	Clock/Data Rise Time	See (6)			300	ns
t_{POR}	Time in which a device must be operational after power-on reset	See (6) (4)			500	ms

(1) EEPROM interface requires 400 KHz capable EEPROM device.
(2) Recommended value.
(3) Recommended maximum capacitance load per bus segment is 400pF.
(4) Guaranteed by Design and/or characterization. Parameter not tested in production.
(5) Maximum termination voltage should be identical to the device supply voltage.
(6) Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.

TIMING DIAGRAMS

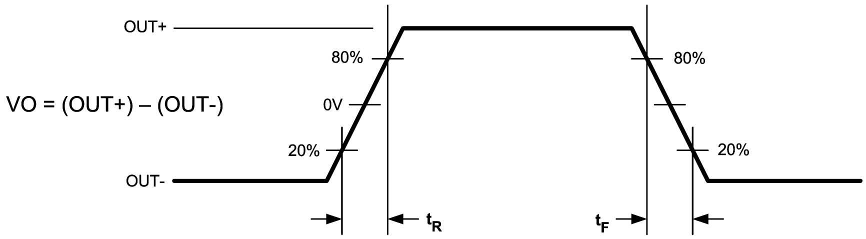


Figure 2. CML Output Transition Times

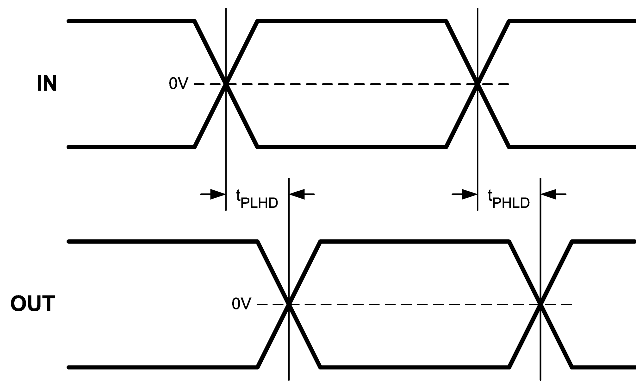


Figure 3. Propagation Delay Timing Diagram

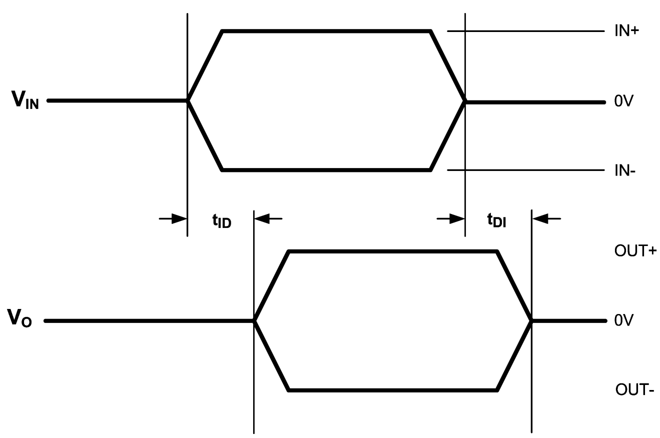


Figure 4. Idle Timing Diagram

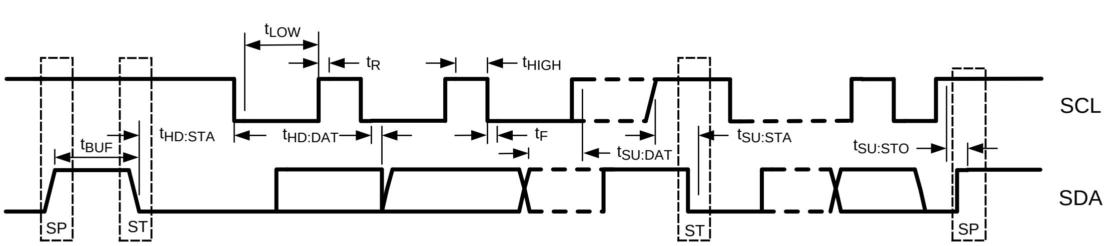


Figure 5. SMBus Timing Parameters

FUNCTIONAL DESCRIPTION

The DS100BR111 is a high performance circuit capable of delivering excellent performance. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the information below and Revision 4 of the LVDS Owner's Manual for more detailed information on high speed design tips to address signal integrity design issues.

The control pins have been enhanced to have 4 different levels and provide a wider range of control settings. Refer to Table 1

Table 1. 4-Level Control Pin Settings

Pin Setting	Description
0	Tie pin to GND through a 1 KΩ resistor
R	Tie pin to ground through 20 KΩ resistor
Float	Float the pin (no connection)
1	Tie pin to VDD through a 1 KΩ resistor

NOTE

4-Level IO pins require a 1K resistance to GND or VDD/VIN. It is possible to tie mulitple 4-level IO pins together with a single resistor to GND or VDD/VIN. When multiple IOs are connected in parallel, the resistance to GND or VDD/VIN should be adjusted to compensate. For 2 pins the optimal resistance is 500 Ohms, 3 pins = 330 Ohms, and 4 pins = 250 Ohms.

NOTE

For 2.5V mode the control pin logic 1 level is VDD (pins 21 and 22), in 3.3V mode the control pin logic 1 level is defined by VIN (pin 15).

Table 2. Equalizer Settings

Level	EQA1/EQB1	EQA0/EQB0	EQ — 8 bits [7:0]	dB Boost at 5 Ghz	Suggested Media
1	0	0	0000 0000 = 0x00	2.5	FR4 < 5 inch trace
2	0	R	0000 0001 = 0x01	6.5	FR4 5 inch trace
3	0	Float	0000 0010 = 0x02	9	FR4 10 inch trace
4	0	1	0000 0011 = 0x03	11.5	FR4 15 inch trace
5	R	0	0000 0111 = 0x07	14	FR4 20 inch trace
6	R	R	0001 0101 = 0x15	15	FR4 25 inch trace
7	R	Float	0000 1011 = 0x0B	17	FR4 25 inch trace
8	R	1	0000 1111 = 0x0F	19	7m 30AWG Cable
9	Float	0	0101 0101 = 0x55	20	FR4 30 inch trace
10	Float	R	0001 1111 = 0x1F	23	8m 30 AWG Cable FR4 35 inch trace
11	Float	Float	0010 1111 = 0x2F	25	10m 30 AWG Cable
12	Float	1	0011 1111 = 0x3F	27	10m - 12m, Cable
13	1	0	1010 1010 = 0xAA	30	
14	1	R	0111 1111 = 0x7F	31	
15	1	Float	1011 1111 = 0xBF	33	
16	1	1	1111 1111 = 0xFF	34	

NOTE

Settings are approximate and will change based on PCB material, trace dimensions, and driver waveform characteristics.

Table 3. De-emphasis and Output Voltage Settings

Level	VOD_SEL	DEMA/B	SMBus Register DEM Level	SMBus Register VOD Level	VOD (mV)	DEM (dB)
1	0	0	000	000	700	0
2	0	Float	010	000	700	- 3.5
3	0	R	011	000	700	- 6
4	0	1	101	000	700	- 9
5	Float	0	000	011	1000	0
6	Float	Float	010	011	1000	- 3.5
7	Float	R	011	011	1000	- 6
8	Float	1	101	011	1000	- 9
9	R	0	000	101	1200	- 0
10	R	Float	010	101	1200	- 3.5
11	R	R	011	101	1200	- 6
12	R	1	101	101	1200	- 9
13	1	0	000	100	1100	0
14	1	Float	001	100	1100	- 1.5
15	1	R	001	110	1300	- 1.5
16	1	1	010	110	1300	- 3.5

NOTE

The DS100BR111 VOD for OUTPUT A is limited to 700 mV in pin mode (ENSMB=0). With ENSMB = 1 or FLOAT, the VOD for OUTPUT A can be adjusted with SMBus register 0x23 [4:2] as shown in Table 9.

NOTE

When VOD_SEL is in the Logic 1 state (1K resistor to VIN/VDD) the DS100BR111 will support 10G-KR back-channel communication using pin control.

NOTE

In SMBus Mode if VOD_SEL is in the Logic 1 state (1K resistor to VIN/VDD) the DS100BR111 AD0-AD3 pins are internally forced to 0'h

Table 4. Signal Detect Threshold Level

SD_TH	SMBus REG bit [3:2] and [1:0]	Assert Level (Typical)	De-assert Level (Typical)
0	10	210 mV	150 mV
20K to GND	01	160 mV	100 mV
Float (Default)	00	180 mV	110 mV
1	11	190 mV	130 mV
Note: VDD = 2.5V, 25°C, and 010101 pattern at 10 Gbps			

APPLICATIONS INFORMATION

4-Level Input Configuration Guidelines

The 4-level input pins utilize a resistor divider to help set the 4 valid levels. There is an internal 30K pull-up and a 60K pull-down connected to the package pin. These resistors, together with the external resistor connection combine to achieve the desired voltage level. Using the 1K pull-up, 1K pull-down, no connect, and 20K pull-down provide the optimal voltage levels for each of the four input states.

Table 5. 4-Level Input Voltage

Level	Setting	3.3V Mode	2.5V Mode
0	01K to GND	0.1 V	0.08 V
R	20K to GND	0.33 * V_{IN}	0.33 * V_{DD}
F	FLOAT	0.67 * V_{IN}	0.67 * V_{DD}
1	1K to V_{DD}/V_{IN}	V_{IN} - 0.05V	V_{IN} - 0.04V

- Typical 4-Level Input Thresholds
  – Level 1 - 2 = 0.2 V_{IN} or V_{DD}
  – Level 2 - 3 = 0.5 V_{IN} or V_{DD}
  – Level 3 - 4 = 0.8 V_{IN} or V_{DD}

In order to minimize the startup current associated with the integrated 2.5V regulator the 1K pull-up / pull-down resistors are recommended. If several 4 level inputs require the same setting, it is possible to combine two or more 1K resistors into a single lower value resistor. As an example; combining two inputs with a single 500Ω resistor is a good way to save board space.

10G-KR Configuration Guidelines

When configured in "KR Mode", using either the VOD_SEL pin setting or SMBus register control, the DS100BR111 is designed to operate transparently within a KR backplance channel environment. Installing a DS100 repeater within the KR backplane channel splits the total channel attenuation into two parts. Ideally the repeater can be placed near the middle of the channel maximizing the signal to noise ratio across the bidirectional interface.

In order to maximize the 10G-KR solution space, the 802.3ap specification calls for an optimization of the transmit signal conditioning coefficients based on feedback for the KR receiver. Setting the DS100BR111 active CTLE to compensate for the channel loss from each of the KR transmitters will reduce the transmit and receive equalization settings required on the KR physical layer devices. This central location keeps a larger S/N raito at all points in the channel, extending the available solution space and increasing the overall margin of almost any channel.

PCB Layout Guidelines

The CML inputs and outputs have been optimized to work with interconnects using a controlled differential impedance of 85 - 100Ω. It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Whenever differential vias are used the layout must also provide for a low inductance path for the return currents as well. Route the differential signals away from other signals and noise sources on the printed circuit board. See SNOA401Q *AN-1187* for additional information on WQFN packages.

Different transmission line topologies can be used in various combinations to achieve the optimal system performance. Impedance discontinuities at vias can be minimized or eliminated by increasing the swell around each hole and providing for a low inductance return current path. When the via structure is associated with thick backplane PCB, further optimization such as back drilling is often used to reduce the detrimental high frequency effects of stubs on the signal path.

Power Supply Configuration Guidelines

The DS100BR111 can be configured for 2.5V operation or 3.3V operation. The lists below outline required connections for each supply selection.

3.3V Mode of Operation

1. Tie VDD_SEL = 0 with 1K resistor to GND.
2. Feed 3.3V supply into VIN pin. Local 1.0 uF decoupling at VIN is recommended.
3. See information on VDD bypass below.
4. SDA and SCL pins should connect pull-up resistor to VIN
5. Any 4-Level input which requires a connection to "Logic 1" should use a 1K resistor to VIN

2.5V Mode of Operation

6. VDD_SEL = Float
7. VIN = Float
8. Feed 2.5V supply into VDD pins.
9. See information on VDD bypass below.
10. SDA and SCL pins connect pull-up resistor to VDD for 2.5V uC SMBus IO
11. SDA and SCL pins connect pull-up resistor to VDD for 3.3V uC SMBus IO
12. Any 4-Level input which requires a connection to "Logic 1" should use a 1K resistor to VIN

NOTE

The DAP (bottom solder pad) is the GND connection.

Power Supply Bypass

Two approaches are recommended to ensure that the DS100BR111 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the V_{DD} and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1 μF bypass capacitor should be connected to each V_{DD} pin such that the capacitor is placed as close as possible to the device. Smaller body size capacitors can help facilitate proper component placement.

System Management Bus (SMBus) and Configuration Registers

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. ENSMB must be pulled high to enable SMBus mode and allow access to the configuration registers.

The DS100BR111 has AD[3:0] inputs in SMBus mode. These pins are the user set SMBus slave address inputs. When pulled low the AD[3:0] = 0000'b, the device default address byte is B0'h. Based on the SMBus 2.0 specification, this configuration results in a 7-bit slave address of 1011000'b. The LSB is set to 0'b (for a WRITE), thus the 8-bit value is 1011 0000'b or B0'h. The device address byte can be set with the use of the AD[3:0] inputs.

Shown in the form of an expression:

Slave Address [7:4] = The DS100BR111 hardware address (1011'b) + Address pin AD[3]

Slave Address [3:1] = Address pins AD[2:0]

Slave Address [0] = 0'b for a WRITE or 1'b for a READ

Slave Address Examples:

- AD[3:0] = 0001'b, the device slave address byte is B2'h
  - Slave Address [7:4] = 1011'b + 0'b = 1011'b or B'h
  - Slave Address [3:1] = 001'b
  - Slave Address [0] = 0'b for a WRITE
- AD[3:0] = 0010'b, the device slave address byte is B4'h

  - Slave Address [7:4] = 1011'b + 0'b = 1011'b or B'h
  - Slave Address [3:1] = 010'b
  - Slave Address [0] = 0'b for a WRITE
- AD[3:0] = 0100'b, the device slave address byte is B8'h
  - Slave Address [7:4] = 1011'b + 0'b = 1011'b or B'h
  - Slave Address [3:1] = 100'b
  - Slave Address [0] = 0'b for a WRITE
- AD[3:0] = 1000'b, the device slave address byte is C0'h
  - Slave Address [7:4] = 1011'b + 1'b = 1100'b or C'h
  - Slave Address [3:1] = 000'b
  - Slave Address [0] = 0'b for a WRITE

TRANSFER OF DATA VIA THE SMBus

During normal operation the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SCL is High indicates a message START condition.

STOP: A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.

IDLE: If SCL and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

SMBus TRANSACTIONS

The device supports WRITE and READ transactions. See Table 9 for register address, type (Read/Write, Read Only), default value and function information.

WRITING A REGISTER

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drive the 8-bit data byte.
6. The Device drives an ACK bit (“0”).
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

READING A REGISTER

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.
7. The Device drives an ACK bit “0”.
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit “1”indicating end of the READ transfer.
10. The Host drives a STOP condition.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

Please see Table 9 for more information.

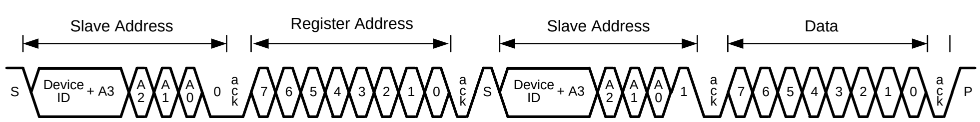


Figure 6. Typical SMBus Write Operation

EEPROM Modes in DS100BR111 Devices

The DS100BR111 supports reading directly from an external EEPROM device by implementing SMBus Master mode. When using the SMBus master mode, the DS100 will read directly from specific location in the external EEPROM. When designing a system for using the external EEPROM, the user needs to follow these specific guidelines.

- Set the DS100BR111 into SMBus Master Mode
  - Float ENSMB (PIN 3)
- The external EEPROM device must support 400 KHz operation
- The external EEPROM device address byte must be 0xA0'h
- Set the AD[3:0] inputs for SMBus address byte. When the AD[3:0] = 0000'b, the device address byte is B0'h.
- Based on the SMBus 2.0 specification, a device can have a 7-bit slave address of 1010 000'b. The LSB is set to 0'b (for a WRITE). The bit mapping for SMBus is listed below:
  - [7:5] = Reserved Bits from the SMBus specification
  - [4:1] = Usable SMBus Address Bits
  - [0] = Write Bit
- The DS100BR111 devices have AD[3:0] inputs in SMBus mode (pins 1, 2, 9, 10). These pins set SMBus slave address. When the AD[3:0] = 0001'b, the device address byte is B2'h.
  - [7:5] = Default to 3b'101
  - [4:1] = Address of 4'b0001
  - [0] = Write Bit, 1'b0
- The device address can be set with the use of the AD[3:0] input up to 16 different addresses. Use the example below to set each of the SMBus addresses.
  - AD[3:0] = 0001'b, the device address byte is B2'h
  - AD[3:0] = 0010'b, the device address byte is B4'h
  - AD[3:0] = 0011'b, the device address byte is B6'h
  - AD[3:0] = 0100'b, the device address byte is B8'h
- The master implementation in the DS100BR111 supports multiple devices reading from 1 EEPROM. When tying multiple devices to the SDA and SCL pins, use these guidelines:
  - Use adjacent SMBus addresses for the 4 devices
  - Use a pull-up resistor on SDA; value = 4.7KΩ
  - Use a pull-up resistor on SCL: value = 4.7KΩ
  - Daisy-chain READEN# (pin 17) and DONE# (pin18) from one device to the next device in the sequence
    1. Tie READEN# of the 1st device in the chain (U1) to GND
    2. Tie DONE# of U1 to READEN# of U2
    3. Tie DONE# of U2 to READEN# of U3
    4. Tie DONE# of U3 to READEN# of U4
    5. Optional: Tie DONE# of U4 to a LED to show each of the devices have been loaded successfully

Master EEPROM Mode in the DS100BR111

Below is an example of a 2 kbits (256 x 8-bit) EEPROM in hex format for the DS100BR111 device. The first 3 bytes of the EEPROM always contain a header common and necessary to control initialization of all devices connected to the I2C bus. CRC enable flag to enable/disable CRC checking. There is a MAP bit to flag the presence of an address map that specifies the configuration data start in the EEPROM. If the MAP bit is not present the configuration data start address is derived from the DS100BR111 address and the configuration data size. A bit to indicate an EEPROM size > 256 bytes is necessary to properly address the EEPROM. There are 37 bytes of data size for each DS100BR111 device.

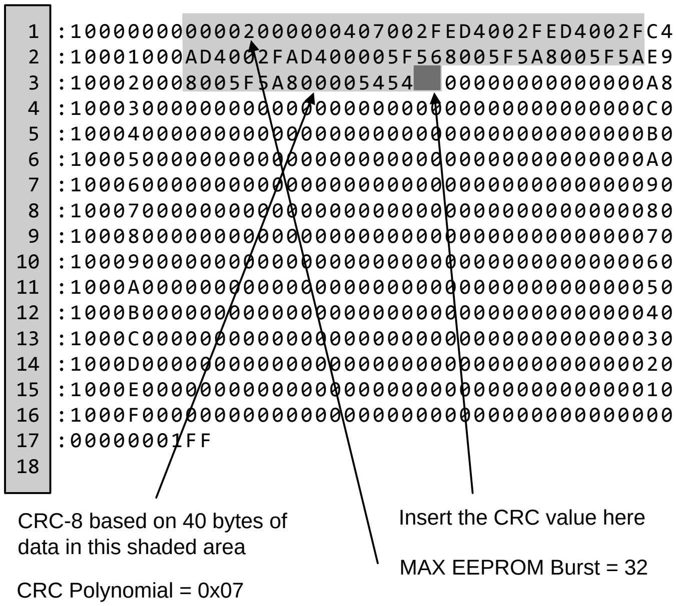


Figure 7. Typical EEPROM Data Set

The CRC-8 calculation is performed on the first 3 bytes of header information plus the 37 bytes of data for the DS100BR111 or 40 bytes in total. The result of this calculation is placed immediately after the DS100BR111 data in the EEPROM which ends with "5454". The CRC-8 in the DS100BR111 uses a polynomial = $x^8 + x^2 + x + 1$

In SMBus master mode the DS100BR111 reads its initial configuration from an external EEPROM upon power-up. Some of the pins of the DS100BR111 perform the same functions in SMBus master and SMBus slave mode. Once the DS100BR111 has finished reading its initial configuration from the external EEPROM in SMBus master mode it reverts to SMBus slave mode and can be further configured by an external controller over the SMBus. The connection to an external SMBus master is optional and can be omitted for applications were additional security is desirable. There are two pins that provide unique functions in SMBus master mode.

- DONE#
- READEN#

When the DS100BR111 is powered up in SMBus master mode, it reads its configuration from the external EEPROM when the READEN# pin goes low. When the DS100BR111 is finished reading its configuration from the external EEPROM, it drives the DONE# pin low. In applications where there is more than one DS100BR111 on the same SMBus, bus contention can result if more than one DS100BR111 tries to take control of the SMBus at the same time. The READEN# and DONE# pins prevent this bus contention. The system should be designed so that the READEN# pin from one DS100BR111 in the system is driven low on power-up. This DS100BR111 will take command of the SMBus on power-up and will read its initial configuration from the external EEPROM. When it is finished reading its configuration, it will drive the DONE# pin low. This pin should be connected to the READEN# pin of another DS100BR111. When this DS100BR111 senses its READEN# pin driven low, it will take command of the SMBus and read its initial configuration from the external EEPROM, after which it will set its DONE# pin low. By connecting the DONE# pin of each DS100BR111 to the READEN# pin of the next DS100BR111, each DS100BR111 can read its initial configuration from the EEPROM without causing bus contention.

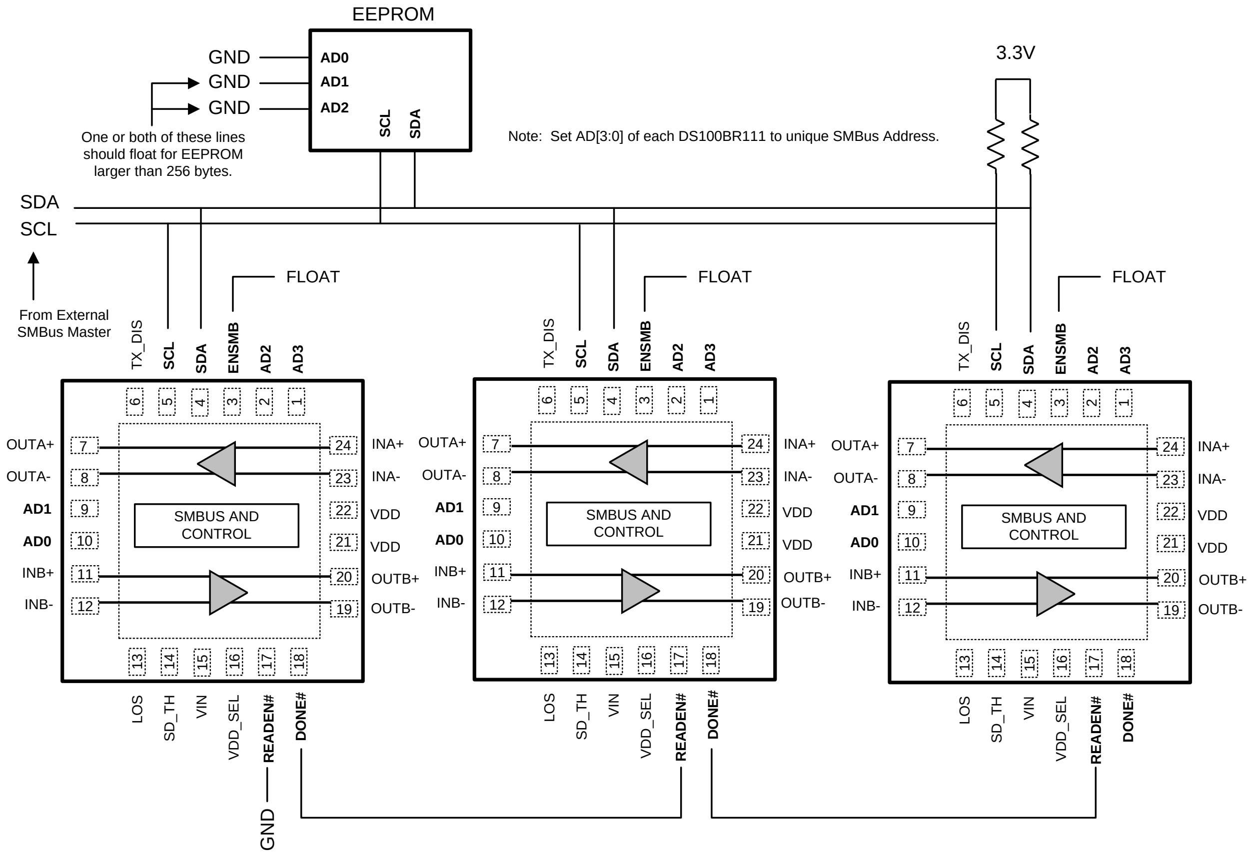


Figure 8. Typical multi-device EEPROM connection diagram

Table 6. Multi-Device EEPROM Register Map Overview

	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	BIt 0
Header	0	CRC EN	Address Map	EEPROM > 256 Bytes	Reserved	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]
	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	2	EE Burst[7]	EE Burst[6]	EE Burst[5]	EE Burst[4]	EE Burst[3]	EE Burst[2]	EE Burst[1]	EE Burst[0]
Device 0 Info	3	CRC[7]	CRC[6]	CRC[5]	CRC[4]	CRC[3]	CRC[2]	CRC[1]	CRC[0]
	4	EE AD0 [7]	EE AD0 [6]	EE AD0 [5]	EE AD0 [4]	EE AD0 [3]	EE AD0 [2]	EE AD0 [1]	EE AD0 [0]
Device 1 Info	5	CRC[7]	CRC[6]	CRC[5]	CRC[4]	CRC[3]	CRC[2]	CRC[1]	CRC[0]
	6	EE AD1 [7]	EE AD1 [6]	EE AD1 [5]	EE AD1 [4]	EE AD1 [3]	EE AD1 [2]	EE AD1 [1]	EE AD1 [0]
Device 2 Info	7	CRC[7]	CRC[6]	CRC[5]	CRC[4]	CRC[3]	CRC[2]	CRC[1]	CRC[0]
	8	EE AD2 [7]	EE AD2 [6]	EE AD2 [5]	EE AD2 [4]	EE AD2 [3]	EE AD2 [2]	EE AD2 [1]	EE AD2 [0]
Device 3 Info	9	CRC[7]	CRC[6]	CRC[5]	CRC[4]	CRC[3]	CRC[2]	CRC[1]	CRC[0]
	10	EE AD3 [7]	EE AD3 [6]	EE AD3 [5]	EE AD3 [4]	EE AD3 [3]	EE AD3 [2]	EE AD3 [1]	EE AD3 [0]
Device 0 Addr 3	11	RES	RES	RES	RES	RES	RES	RES	RES
Device 0 Addr 4	12	RES	RES	PDWN Inp	PDWN OSC	RES	eSATA CHA	eSATA CHB	Ovrd TX_DIS
Device 0 Addr 38	46	RES	RES	RES	RES	RES	RES	RES	RES
Device 0 Addr 39	47	DRES	RES	RES	RES	RES	RES	RES	RES
Device 1 Addr 3	48	RES	RES	RES	RES	RES	RES	RES	RES
Device 1 Addr 4	49	RES	RES	PDWN Inp	PDWN OSC	RES	eSATA CHA	eSATA CHB	Ovrd TX_DIS
Device 1 Addr 38	83	RES	RES	RES	RES	RES	RES	RES	RES
Device 1 Addr 39	84	RES	RES	RES	RES	RES	RES	RES	RES
Device 2 Addr 3	85	RES	RES	RES	RES	RES	RES	RES	RES
Device 2 Addr 4	86	RES	RES	PDWN Inp	PDWN OSC	RES	eSATA CHA	eSATA CHB	Ovrd TX_DIS
Device 2 Addr 38	120	RES	RES	RES	RES	RES	RES	RES	RES
Device 2 Addr 39	121	RES	RES	RES	RES	RES	RES	RES	RES
Device 3 Addr 3	122	RES	RES	RES	RES	RES	RES	RES	RES
Device 3 Addr 4	123	RES	RES	PDWN Inp	PDWN OSC	RES	eSATA CHA	eSATA CHB	Ovrd TX_DIS
Device 3 Addr 38	157	RES	RES	RES	RES	RES	RES	RES	RES
Device 3 Addr 39	158	RES	RES	RES	RES	RES	RES	RES	RES

- CRC EN = 1; Address Map = 1
- EEPROM > 256 Bytes = 0
- COUNT[3:0] = 0011'b
- Note: Multiple DS100BR111 devices may point at the same address space if they have identical programming values.

Table 7. Single EEPROM Header + Register Map with Default Value

EEPROM Address Byte		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	BIt 0
Description	0	CRC EN	Address Map Present	EEPROM > 256 Bytes	RES	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]
Value		0	0	0	0	0	0	0	0
Description	1	RES	RES	RES	RES	RES	RES	RES	RES
Value		0	0	0	0	0	0	0	0
Description	2	Max EEPROM Burst size[7]	Max EEPROM Burst size[6]	Max EEPROM Burst size[5]	Max EEPROM Burst size[4]	Max EEPROM Burst size[3]	Max EEPROM Burst size[2]	Max EEPROM Burst size[1]	Max EEPROM Burst size[0]
Value		0	0	0	0	0	0	0	0
Description	3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register		0x01 [7]	0x01 [6]	0x01 [5]	0x01 [4]	0x01 [3]	0x01 [2]	0x01 [1]	0x01 [0]
Value		0	0	0	0	0	0	0	0
Description	4	Ovrd_LOS	LOS_Value	PDWN Inp	PWDN Osc	Reserved	eSATA Enable A	eSATA Enable B	Ovrd TX_DIS
Register		0x02 [5]	0x02 [4]	0x02 [3]	0x02 [2]	0x02 [0]	0x04 [7]	0x04 [6]	0x04 [5]
Value		0	0	0	0	0	0	0	0
Description	5	TX_DIS CHA	TX_DIS CHB	Reserved	EQ Stage 4 CHB	EQ Stage 4 CHA	Reserved	Overide IDLE_th	Reserved
Register		0x04 [4]	0x04 [3]	0x04 [2]	0x04 [1]	0x04 [0]	0x06 [4]	0x08 [6]	0x08 [5]
Value		0	0	0	0	0	1	0	0
Description	6	Ovrd_IDLE	Reserved	Ovrd_Out Mode	Reserved	Reserved	Reserved	Reserved	Reserved
Register		0x08 [4]	0x08 [3]	0x08 [2]	0x08 [1]	0x08 [0]	0x0B [6]	0x0B [5]	0x0B [4]
Value		0	0	0	0	0	1	1	1
Description	7	Reserved	Reserved	Reserved	Reserved	Idle auto A	Idle sel A	Reserved	Reserved
Register		0x0B [3]	0x0B [2]	0x0B [1]	0x0B [0]	0x0E [5]	0x0E [4]	0x0E [3]	0x0E [2]
Value		0	0	0	0	0	0	0	0
Description	8	CHA EQ[7]	CHA EQ[6]	CHA EQ[5]	CHA EQ[4]	CHA EQ[3]	CHA EQ[2]	CHA EQ[1]	CHA EQ[0]
Register		0x0F [7]	0x0F [6]	0x0F [5]	0x0F [4]	0x0F [3]	0x0F [2]	0x0F [1]	0x0F [0]
Value		0	0	1	0	1	1	1	1
Description	9	A Sel scp	A Out Mode	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register		0x10 [7]	0x10 [6]	0x10 [5]	0x10 [4]	0x10 [3]	0x10 [2]	0x10 [1]	0x10 [0]
Value		1	1	1	0	1	1	0	1
Description	10	DEMA[2]	DEMA[1]	DEMA[0]	CHA Slow	IDLE thA[1]	IDLE thA[0]	IDLE thD[1]	IDLE thD[0]
Register		0x11 [2]	0x11 [1]	0x11 [0]	0x12 [7]	0x12 [3]	0x12 [2]	0x12 [1]	0x12 [0]
Value		0	1	0	0	0	0	0	0
Description	11	Idle auto B	Idle sel B	Reserved	Reserved	CHB EQ[7]	CHB EQ[6]	CHB EQ[5]	CHB EQ[4]
Register		0x15 [5]	0x15 [4]	0x15 [3]	0x15 [2]	0x16 [7]	0x16 [6]	0x16 [5]	0x16 [4]
Value		0	0	0	0	0	0	1	0
Description	12	CHB EQ[3]	CHB EQ[2]	CHB EQ[1]	CHB EQ[0]	B Sel scp	B Out Mode	Reserved	Reserved
Register		0x16 [3]	0x16 [2]	0x16 [1]	0x16 [0]	0x17 [7]	0x17 [6]	0x17 [5]	0x17 [4]
Value		1	1	1	1	1	1	1	0
Description	13	Reserved	Reserved	Reserved	Reserved	CHB DEM[2]	CHB DEM[1]	CHB DEM[0]	CHB Slow
Register		0x17 [3]	0x17 [2]	0x17 [1]	0x17 [1]	0x18 [2]	0x18 [1]	0x18 [0]	0x19 [7]
Value		1	1	0	1	0	1	0	0
Description	14	IDLE thA[1]	IDLE thA[0]	IDLE thD[1]	IDLE thD[0]	Reserved	Reserved	Reserved	Reserved
Register		0x19 [3]	0x19 [2]	0x19 [1]	0x19 [0]				
Value		0	0	0	0	0	0	0	0

Table 7. Single EEPROM Header + Register Map with Default Value (continued)

EEPROM Address Byte		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	BIt 0
Description	15	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	0	1	0	1	1	1	1
Description	16	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		1	0	1	0	1	1	0	1
Description	17	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	1	0	0	0	0	0	0
Description	18	Reserved	CHA VOD[2]	CHA VOD[1]	CHA VOD[0]	Reserved	Reserved	Reserved	Reserved
Register			0x23 [4]	0x23 [3]	0x23 [2]				
Value		0	0	0	0	0	0	1	0
Description	19	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									0x25 [4]
Value		1	1	1	1	1	0	1	0
Description	20	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register		0x25 [3]	0x25 [2]						
Value		1	1	0	1	0	1	0	0
Description	21	Reserved	Reserved	Reserved	Reserved	ovrd fst idle	en hi idle th A	en hi idle th B	en fst idle A
Register						0x28 [6]	0x28 [5]	0x28 [4]	0x28 [3]
Value		0	0	0	0	0	0	0	0
Description	22	en fst idle B	sd mgain A	sd mgain B	Reserved	Reserved	Reserved	Reserved	Reserved
Register		0x28 [2]	0x28 [1]	0x28 [0]					
Value		0	0	0	0	0	0	0	0
Description	23	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	1	0	1	1	1	1	1
Description	24	Reserved	Reserved	Reserved	Reserved	CHB VOD[2]	CHB VOD[1]	CHB VOD[0]	Reserved
Register						0x2D [4]	0x2D 3]	0x2D [2]	
Value		0	1	0	1	0	1	1	0
Description	25	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		1	0	0	0	0	0	0	0
Description	26	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	0	0	0	0	1	0	1
Description	27	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		1	1	1	1	0	1	0	1
Description	28	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		1	0	1	0	1	0	0	0
Description	29	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	0	0	0	0	0	0	0

Table 7. Single EEPROM Header + Register Map with Default Value (continued)

EEPROM Address Byte		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	BIt 0
Description	30	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	1	0	1	1	1	1	1
Description	31	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	1	0	1	1	0	1	0
Description	32	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		1	0	0	0	0	0	0	0
Description	33	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	0	0	0	0	1	0	1
Description	34	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		1	1	1	1	0	1	0	1
Description	35	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		1	0	1	0	1	0	0	0
Description	36	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	0	0	0	0	0	0	0
Description	37	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	0	0	0	0	0	0	0
Description	38	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	1	0	1	0	1	0	0
Description	39	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	1	0	1	0	1	0	0

Below is an example of a 2 kbits (256 x 8-bit) EEPROM Register Dump in hex format for a multi-device DS100BR111 application.

Table 8. Multi DS100BR111 EEPROM Data

EEPROM Address	Address (Hex)	EEPROM Data	Comments
0	00	0x43	CRC_EN = 0, Address Map = 1, Device Count = 3 (Devices 0, 1, 2, and 3)
1	01	0x00	
2	02	0x08	EEPROM Burst Size
3	03	0x00	CRC not used
4	04	0x0B	Device 0 Address Location
5	05	0x00	CRC not used
6	06	0x30	Device 1 Address Location
7	07	0x00	CRC not used
8	08	0x30	Device 2 Address Location
9	09	0x00	CRC not used
10	0A	0x0B	Device 3 Address Location
11	0B	0x00	Begin Device 0 and Device 3 - Address Offset 3
12	0C	0x00	
13	0D	0x04	
14	0E	0x07	
15	0F	0x00	
16	10	0x2F	Default EQ CHA
17	11	0xED	
18	12	0x40	
19	13	0x02	Default EQ CHB
20	14	0xFE	Default EQ CHB
21	15	0xD4	
22	16	0x00	
23	17	0x2F	
24	18	0xAD	
25	19	0x40	
26	1A	0x02	BR111 CHA VOD = 700 mV
27	1B	0xFA	
28	1C	0xD4	
29	1D	0x01	
30	1E	0x80	
31	1F	0x5F	
32	20	0x56	BR111 CHB VOD = 1000 mV
33	21	0x80	
34	22	0x05	
35	23	0xF5	
36	24	0xA8	
37	25	0x00	
38	26	0x5F	
39	27	0x5A	
40	28	0x80	
41	29	0x05	
42	2A	0xF5	
43	2B	0xA8	
44	2C	0x00	
45	2D	0x00	
46	2E	0x54	

Table 8. Multi DS100BR111 EEPROM Data (continued)

EEPROM Address	Address (Hex)	EEPROM Data	Comments
47	2F	0x54	End Device 0 and Device 3 - Address Offset 39
48	30	0x00	Begin Device 1 and Device 2 - Address Offset 3
49	31	0x00	
50	32	0x04	
51	33	0x07	
52	34	0x00	
53	35	0x2F	Default EQ CHA
54	36	0xED	
55	37	0x40	
56	38	0x02	Default EQ CHB
57	39	0xFE	Default EQ CHB
58	3A	0xD4	
59	3B	0x00	
60	3C	0x2F	
61	3D	0xAD	
62	3E	0x40	
63	3F	0x02	BR111 CHA VOD = 700 mV
64	40	0xFA	
65	41	0xD4	
66	42	0x01	
67	43	0x80	
68	44	0x5F	
69	45	0x56	BR111 CHB VOD = 1000 mV
70	46	0x80	
71	47	0x05	
72	48	0xF5	
73	49	0xA8	
74	4A	0x00	
75	4B	0x5F	
76	4C	0x5A	
77	4D	0x80	
78	4E	0x05	
79	4F	0xF5	
80	50	0xA8	
81	51	0x00	
82	52	0x00	
83	53	0x54	
84	54	0x54	End Device 1 and Device 2 - Address Offset 39

Table 9. SMBus Register Map

Address	Register Name	Bits	Field	Type	Default	EEPROM Reg Bit	Description
0x00	Device ID	7	Reserved	R/W	0x00		set bit to 0
		6:3	I2C Address [3:0]	R			[6:3] SMBus strap observation
		2	EEPROM reading done	R			1: EEPROM Loading 0: EEPROM Done Loading
		1	Reserved	RWSC			set bit to 0
		0	Reserved	RWSC			set bit to 0
0x01	Control 1	7:6	Idle Control	R/W	0x00	Yes	Control [7]: Continuous talk ENABLE (Channel A) [6]: Continuous talk ENABLE (Channel B)
		5:3	Reserved	R/W			Set bits to 0
		2	LOS Select	R/W			LOS Monitor Selection 1: Use LOS from CH B 0: Use LOS from CH A
		1:0	Reserved	R/W			Set bits to 00'b
0x02	Control 2	7	Reserved	R/W	0x00		Set bit to 0
		6	Reserved				Set bit to 0
		5	LOS override			Yes	LOS pin override enable (1); Use Normal Signal Detection (0)
		4	LOS override value			Yes	1: Normal Operation 0: Output LOS
		3	PWDN Inputs			Yes	1: PWDN 0: Normal Operation
		2	PWDN Oscillator			Yes	
		1	Reserved				
		0	Reserved			Yes	Set bit to 0
0x04	Control 3	7:6	eSATA Mode Enable	R/W	0x00	Yes	[7] Channel A (1) [6] Channel B (1)
		5	TX_DIS Override Enable				1: Override Use Reg 0x04[4:3] 0: Normal Operation - uses pin
		4	TX_DIS Value Channel A				1: TX Disabled 0: TX Enabled
		3	TX_DIS Value Channel B				
		2	Reserved				Set bit to 0
		1:0	EQ CONTROL				[1]: Channel B - EQ Stage 4 ON/OFF [0]: Channel A - EQ Stage 4 ON/OFF
0x05	CRC 1	7:0	CRC[7:0]	R/W	0x00		Slave Mode CRC Bits
0x06	CRC 2	7	Disable EEPROM CFG	R/W	0x10		Disable Master Mode EEPROM Configuration
		6:5	Reserved				Set bits to 0
		4	Reserved			Yes	Set bit to 1
		3	CRC Slave Mode Disable				[1]: CRC Disable (No CRC Check) [0]: CRC Check ENABLE Note: With CRC check DISABLED register updates take immediate effect on high speed data path. With CRC check ENABLED register updates will NOT take effect until correct CRC value is loaded
		2:1	Reserved				Set bits to 0
		0	CRC Enable				Slave CRC Trigger

Table 9. SMBus Register Map (continued)

Address	Register Name	Bits	Field	Type	Default	EEPROM Reg Bit	Description
0x07	Digital Reset and Control	7	Reserved	R/W	0x01		Set bit to 0
		6	Reset Regs				Self clearing reset for registers. Writing a [1] will return register settings to default values.
		5	Reset SMBus Master				Self clearing reset for SMBus master state machine
		4:0	Reserved				Set bits to '0001b
0x08	Pin Override	7	Reserved	R/W	0x00		Set bit to 0
		6	Override Idle Threshold			Yes	[1]: Override by Channel - see Reg 0x13 and 0x19 [0]: SD_TH pin control
		5	Reserved			Yes	Set bit to 0
		4	Override IDLE			Yes	[1]: Force IDLE by Channel - see Reg 0x0E and 0x15 [0]: Normal Operation
		3	Reserved			Yes	Set bit to 0
		2	Override Out Mode				[1]: Enable Output Mode control for individual outputs. See register locations 0x10[6] and 0x17[6]. [0]: Disable - Outputs are kept in the normal mode of operation allowing VOD and DE adjustments.
		1	Override DEM			Yes	
		0	Reserved			Yes	Set bit to 0
0x0C	CH A Analog Override 1	7	Reserved	R/W	0x00		Set bit to 0
		6	Reserved				Set bit to 0
		5	Reserved				Set bit to 0
		4	Reserved				Set bit to 0
		3:0	Reserved				Set bits to 0000'b.
0x0D	CH A Reserved	7:0	Reserved	R/W	0x00		Set bits to 00'h.
0x0E	CH A Idle Control	7:6	Reserved	R/W	0x00		Set bits to 00'b.
		5	Idle Auto			Yes	Auto IDLE value when override bit is set (reg 0x08 [4] = 1)
		4	Idle Select			Yes	Force IDLE value when override bit is set (reg 0x08 [4] = 1)
		3	Reserved			Yes	Set bit to 0.
		2:0	Reserved				Set bits to 0.
0x0F	CH A EQ Setting	7:0	BOOST [7:0]	R/W	0x2F	Yes	EQ Boost Default to 24 dB See Table 2 for Information
0x10	CH A Control 1	7	Sel_scp	R/W	0xED	Yes	[1]: Short Circuit Protection ON [0]: Short Circuit Protection OFF
		6	Output Mode			Yes	[1]: Normal operation [0]: 10G-KR operation
		5:3	Reserved			Yes	Set bits to = 101'b
		2:0	Reserved			Yes	Set bits to = 101'b

Table 9. SMBus Register Map (continued)

Address	Register Name	Bits	Field	Type	Default	EEPROM Reg Bit	Description
0x11	CH A Control 2	7:5	Reserved	R	0x82		Set bits to = 100'b
		4	Reserved	R/W			Set bit to 0
		3	Reserved				Set bit to 0
		2:0	DEM [2:0]			Yes	De-Emphasis (Default = -3.5 dB) 000'b = -0.0 dB 001'b = -1.5 dB 010'b = -3.5 dB 011'b = -6.0 dB 100'b = -8.0 dB 101'b = -9.0 dB 110'b = -10.5 dB 111'b = -12.0 dB
0x12	CH A Idle Threshold	7	Slow OOB	R/W	0x00	Yes	Slow OOB Enable (1); Disable (0)
		6:4	Reserved				Set bits to 000'b.
		3:2	IDLE thA[1:0]			Yes	Assert Thresholds Use only if register 0x08 [6] = 1 00 = 180 mV (Default) 01 = 160 mV 10 = 210 mV 11= 190 mV
		1:0	IDLE thD[1:0]			Yes	De-assert Thresholds Use only if register 0x08 [6] = 1 00 = 110 mV (Default) 01 = 100 mV 10 = 150 mV 11= 130 mV
0x13	CH B Analog Override 1	7	Reserved	R/W	0x00		Set bit to 0
		6	Reserved				Set bit to 0
		5	Reserved				Set bit to 0
		4	Reserved				Set bit to 0
		3:0	Reserved				Set bits to 0000'b.
0x14	CH B Reserved	7:0	Reserved	R/W	0x00		Set bits to 00'h.
0x15	CH B Idle Control	7:6	Reserved	R/W	0x00		Set bits to 00'b
		5	Idle Auto			Yes	Auto IDLE value when override bit is set (reg 0x08 [4] = 1)
		4	Idle Select			Yes	Force IDLE value when override bit is set (reg 0x08 [4] = 1)
		3:2	Reserved			Yes	Set bits to 00'b.
		1:0	Reserved				Set bits to 00'b.
0x16	CH B EQ Setting	7:0	BOOST [7:0]	R/W	0x2F	Yes	EQ Boost Default to 24 dB See Table 2 for Information
0x17	CH B Control 1	7	Sel_scp	R/W	0xED	Yes	1 = Short Circuit Protection ON 0 = Short Circuit Protection OFF
		6	Output Mode			Yes	[1]: Normal operation [0]: 10G-KR operation
		5:3	Reserved			Yes	Set bits to = 101'b
		2:0	Reserved				Set bits to = 101'b

Table 9. SMBus Register Map (continued)

Address	Register Name	Bits	Field	Type	Default	EEPROM Reg Bit	Description
0x18	CH B Control 2	7:5	Reserved	R	0x82		Set bits to = 100'b
		4	Reserved	R/W			Set bit to 0
		3	Reserved				Set bit to 0
		2:0	DEM [2:0]			Yes	De-Emphasis (Default = -3.5 dB) 000'b = -0.0 dB 001'b = -1.5 dB 010'b = -3.5 dB 011'b = -6.0 dB 100'b = -8.0 dB 101'b = -9.0 dB 110'b = -10.5 dB 111'b = -12.0 dB
0x19	CH B Idle Threshold	7	Slow OOB	R/W	0x00	Yes	Slow OOB Enable (1); Disable (0)
		6:4	Reserved				Set bits to 000'b.
		3:2	IDLE thA[1:0]			Yes	Assert Thresholds Use only if register 0x08 [6] = 1 00 = 180 mV (Default) 01 = 160 mV 10 = 210 mV 11= 190 mV
		1:0	IDLE thD[1:0]			Yes	De-assert Thresholds Use only if register 0x08 [6] = 1 00 = 110 mV (Default) 01 = 100 mV 10 = 150 mV 11= 130 mV
0x23	CH A VOD Control	7:6	Reserved	R/W	0x00		Set bits to 00'b.
		4:2	VOD_CH0[2:0]			Yes	DS100BR111 VOD Controls for CH A (Default = 000'b) 000'b = 700 mV 001'b = 800 mV 010'b = 900 mV 011'b = 1000 mV 100'b = 1100 mV 101'b = 1200 mV 110'b = 1300 mV
		1:0	Reserved				Set bits to 00'b.
0x25	Reserved	7:5	Reserved	R/W	0xAD		Set bits to 101'b.
		4:2	Reserved			Yes	Set bits to 011'b.
		1:0	Reserved				Set bits to 01'b.
0x28	Idle Control	7	Reserved	R/W	0x00		
		6	Override Fast Idle			Yes	
		5:4	en_high_idle_th[1:0]			Yes	Enable high SD thresholds [5]: CH A [4]: CH B
		3:2	en_fast_idle[1:0]			Yes	Enable Fast IDLE [3]: CH A [2]: CH B
		1:0	Reserved			Yes	Set bits to 00'b.

Table 9. SMBus Register Map (continued)

Address	Register Name	Bits	Field	Type	Default	EEPROM Reg Bit	Description
0x2D	CH B VOD Control	7:5	Reserved	R/W	0xAD		Set bits to 101'b.
		4:2	VOD_CH0[2:0]			Yes	VOD Controls for CH B (Default = 011'b) 000'b = 700 mV 001'b = 800 mV 010'b = 900 mV 011'b = 1000 mV 100'b = 1100 mV 101'b = 1200 mV 110'b = 1300 mV
		1:0	Reserved				Set bits to = 01'b
0x51	Device Information	7:5	Version[2:0]	R	0x67		Read bits = 011'b
		4:0	Device ID[4:0]				BR111 = 0 0111'b

Typical DC Performance Characteristics

The following data was collected at 25°C

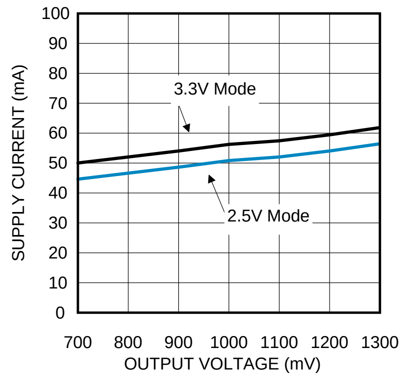


Figure 9. Supply Current vs. Output Voltage Setting

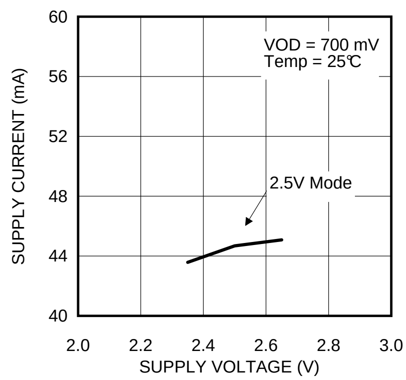


Figure 10. Supply Current vs. Supply Voltage

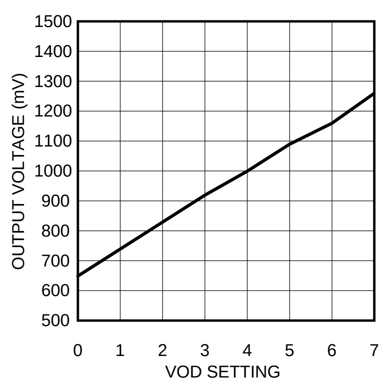


Figure 11. Output Voltage vs. Output Voltage Setting

Typical AC Performance Characteristics

NO MEDIA:

Device	Random Jitter (Rj)	Deterministic Jitter (Dj)	Dj Component Breakdown	Total Jitter (Tj @ 1E-12)
DS100BR111 @ 10.3125 Gbps	280 fs	9.8 ps	DDJ = 7.6 ps	13.7 ps
			DCD = 2.1 ps	
			DDPWS = 5.4 ps	
			PJ = 0.25 ps	

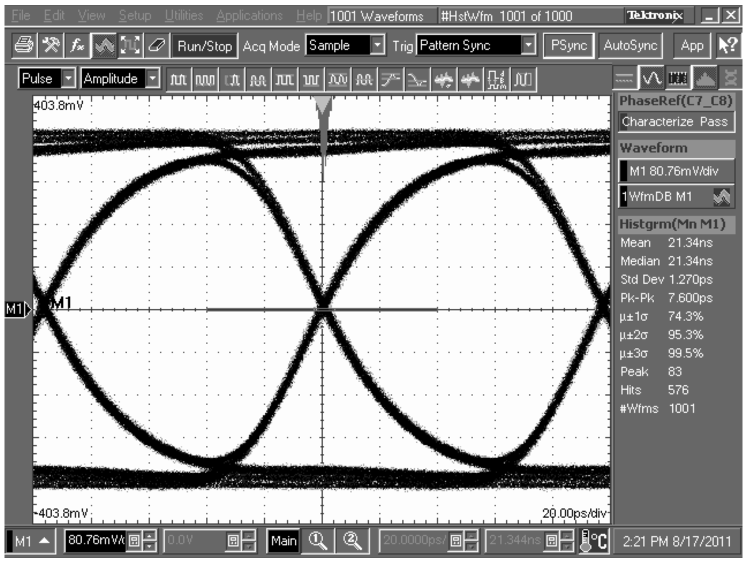


Figure 12. No Media; D3186 driving device directly

EQUALIZATION RESULTS:

The following lab setups were used to collect typical performance data on FR4 and Cable media

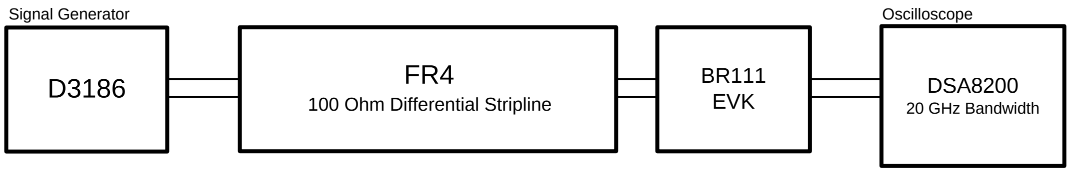


Figure 13. Equalization Test Setup for FR4

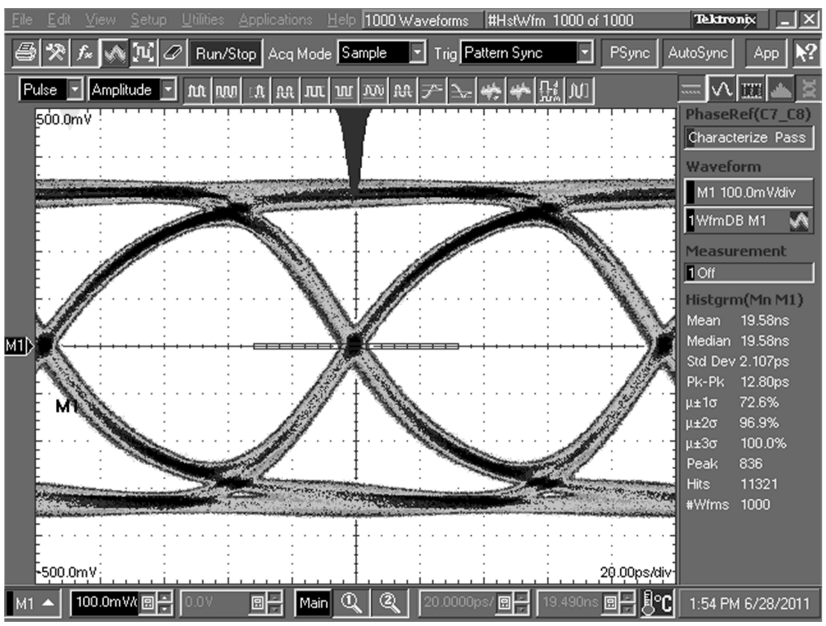


Figure 14. Equalization Performance with 10" of 4 mil FR4 using EQ settting 0x01

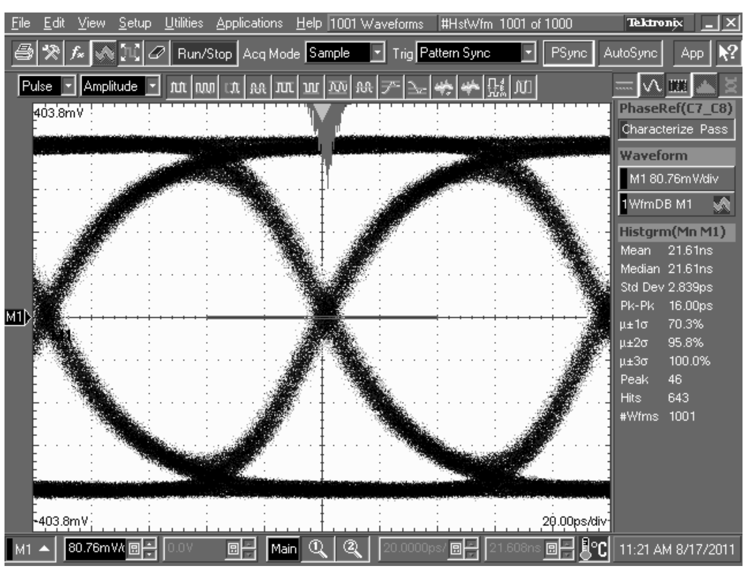


Figure 15. Equalization Performance with 30" of 4 mil FR4 using EQ settting 0x16

CABLE TRANSMIT and RECEIVE RESULTS:

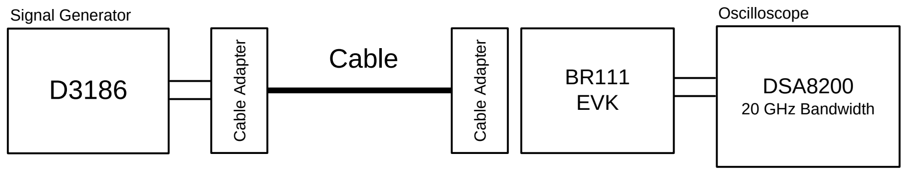


Figure 16. Equalization Test Setup for Cables

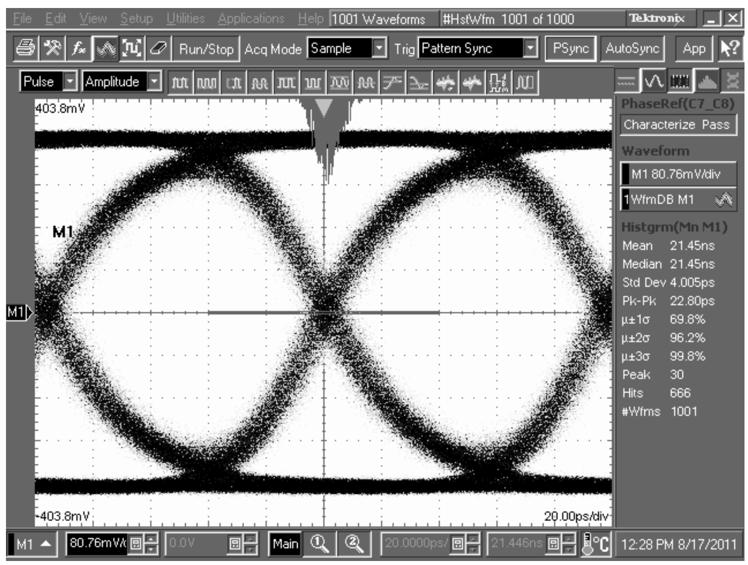


Figure 17. 8M 30AWG Cable Performance with 700mV Launch VOD and Rx EQ setting 0x0F

DE-EMPHASIS RESULTS:

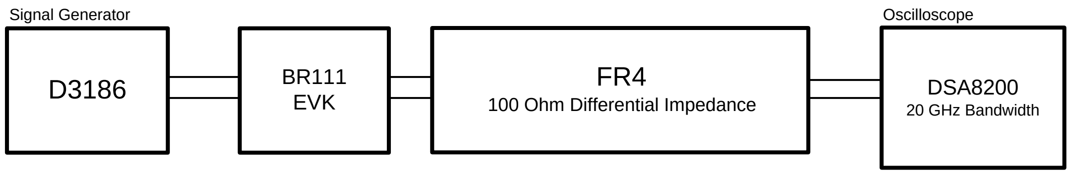


Figure 18. De-Emphasis Test Setup

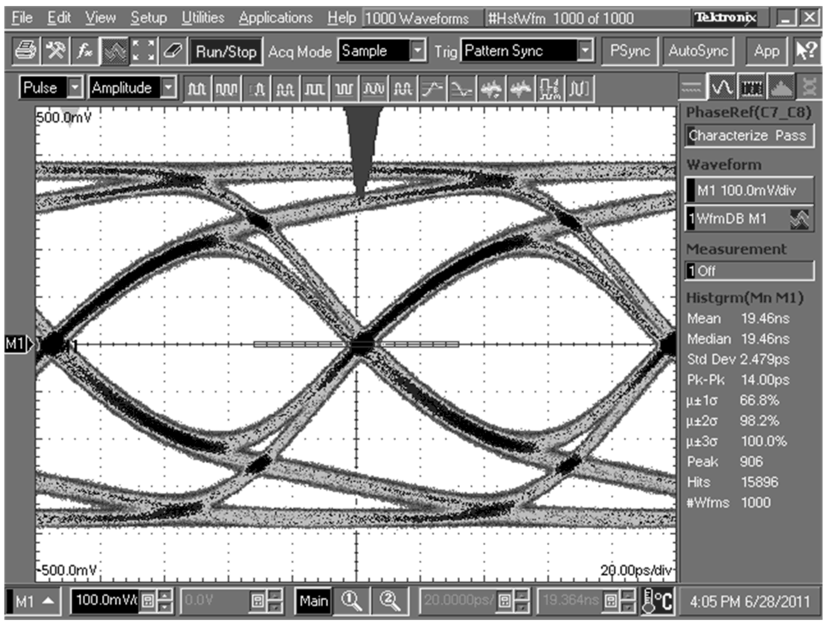


Figure 19. De-Emphasis Performance with 5" of 4 mil FR4 using DE settting 0x01

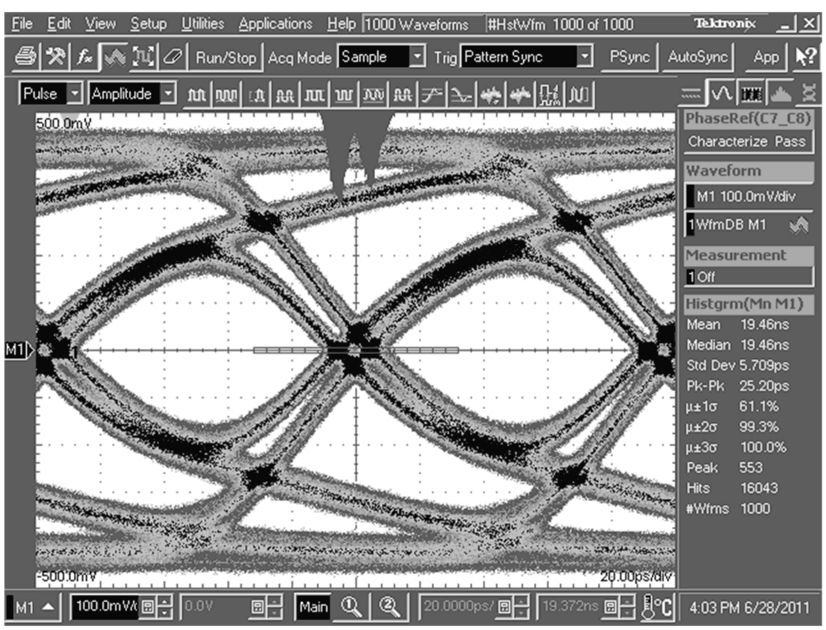


Figure 20. 5" of 4 mil FR4 Without De-Emphasis

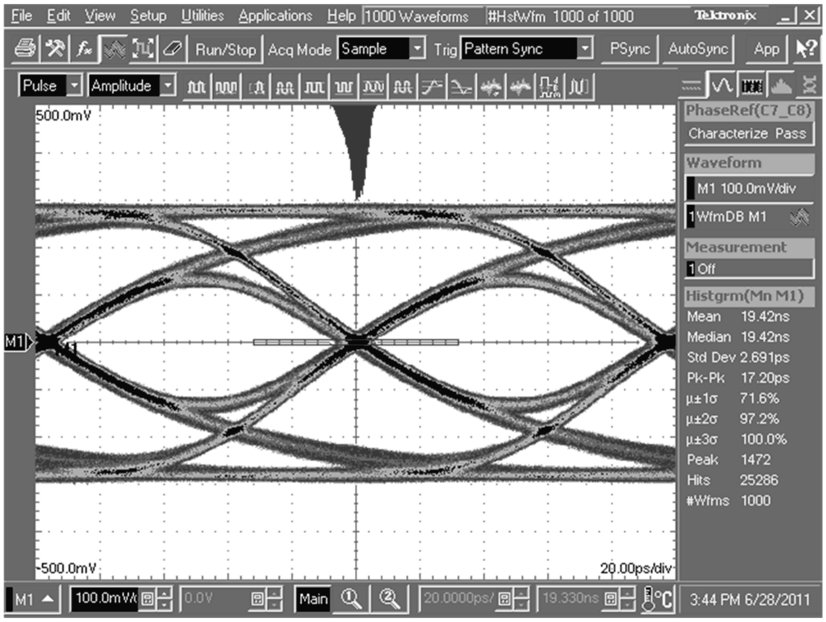


Figure 21. De-Emphasis Performance with 10" of 4 mil FR4 using DE settting 0x02

Figure 22. 10" of 4 mil FR4 Without De-Emphasis

REVISION HISTORY

Changes from Revision D (February 2013) to Revision E **Page**

- Changed layout of National Data Sheet to TI format 37

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS100BR111SQ/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	BR111	Samples
DS100BR111SQE/NOPB	ACTIVE	WQFN	RTW	24	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	BR111	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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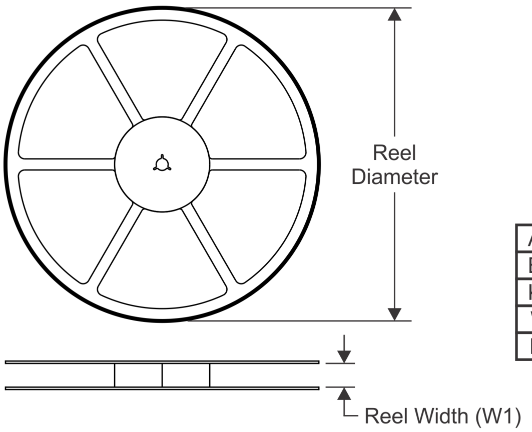
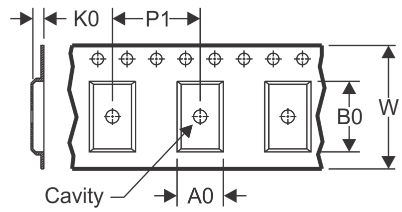
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

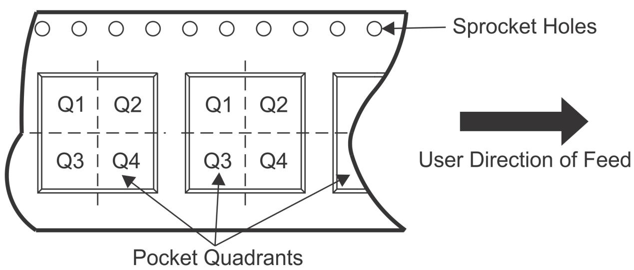


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

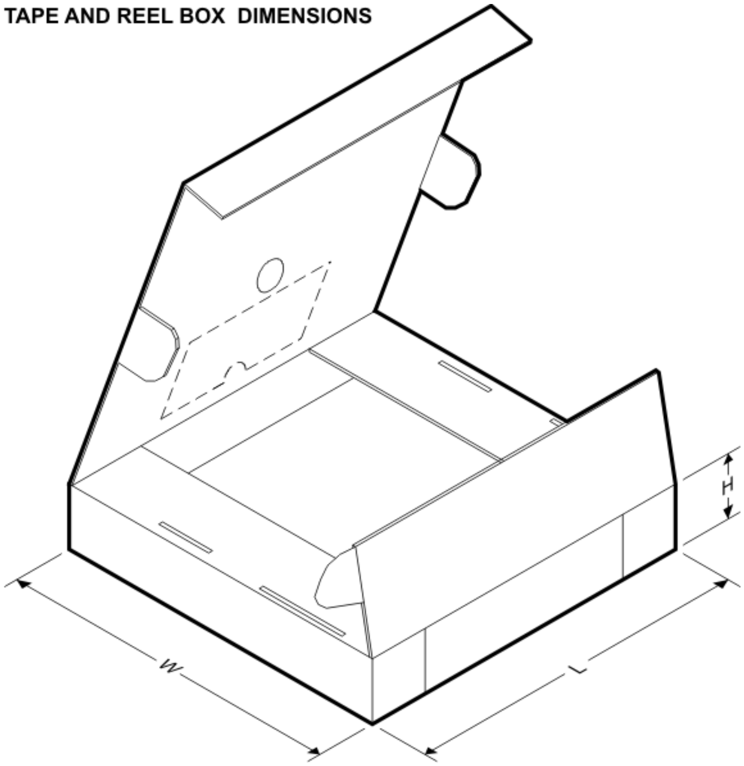
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS100BR111SQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
DS100BR111SQE/NOPB	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

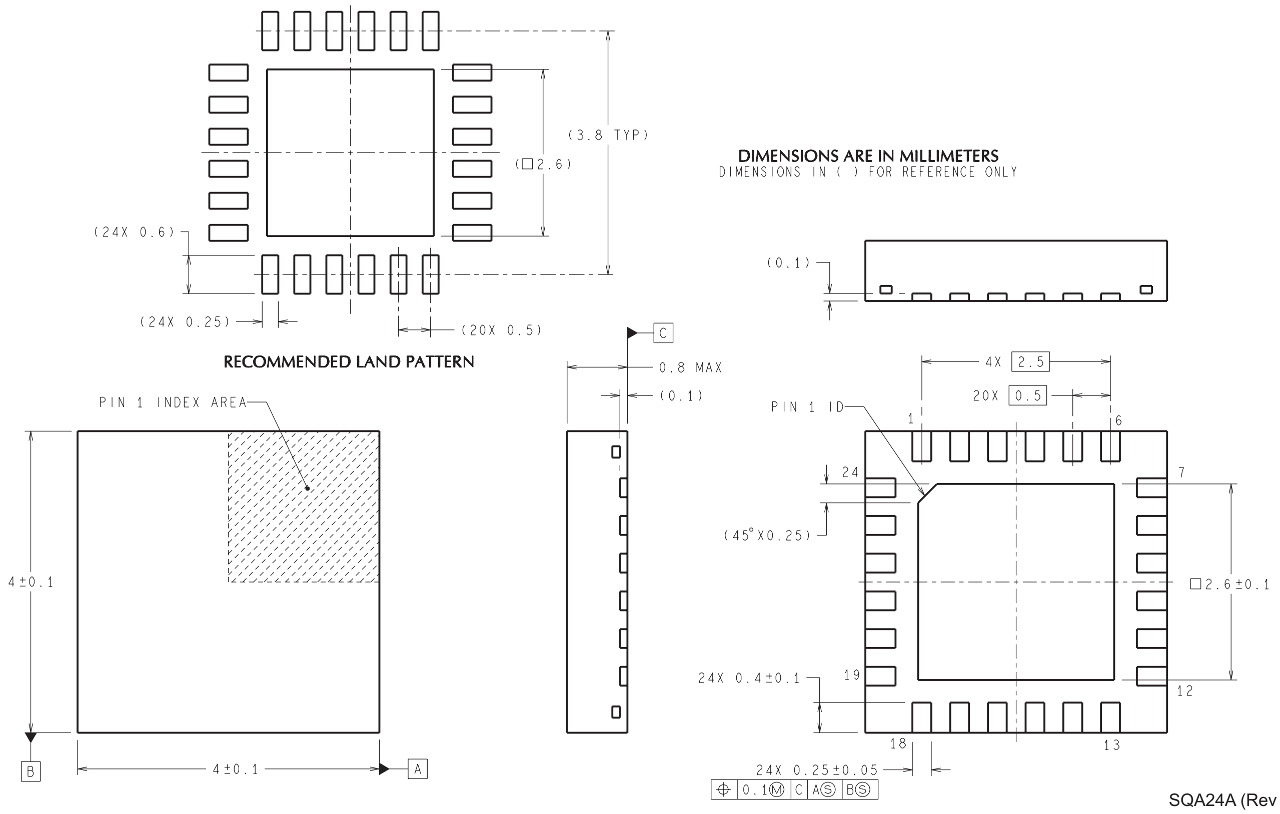
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS100BR111SQ/NOPB	WQFN	RTW	24	1000	213.0	191.0	55.0
DS100BR111SQE/NOPB	WQFN	RTW	24	250	213.0	191.0	55.0

RTW0024A



SQA24A (Rev B)

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