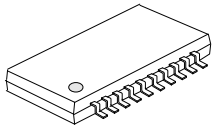
FET BIAS CONTROLLER



SSOP-20(150mil)

■ DESCRIPTION

The UTC **L8001** is specially designed integrated circuit for satellite receiver front-end block. It provides stable drain and gate bias conditions for GaAs or HEMT FETs.

The UTC **L8001**, provide six FETs bias control respectively. By adjusting two external resistors, it can change the FET's bias current to optimize the satellite receiver front end block performances.

It generates the required negative voltage to bias the gate of GaAs FET, and internally provides protection circuit that can protect the FET devices during supply voltage transient. So it is very popular in satellite receiver front end block.

■ FEATURES

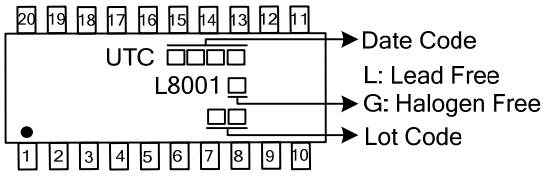
* Built in FET device protection circuit
* Adjustable FET device operating current
* Stable bias control for GaAs and HEMT FETs
* Drive up to six FETs
* Wide supply voltage range

■ ORDERING INFORMATION

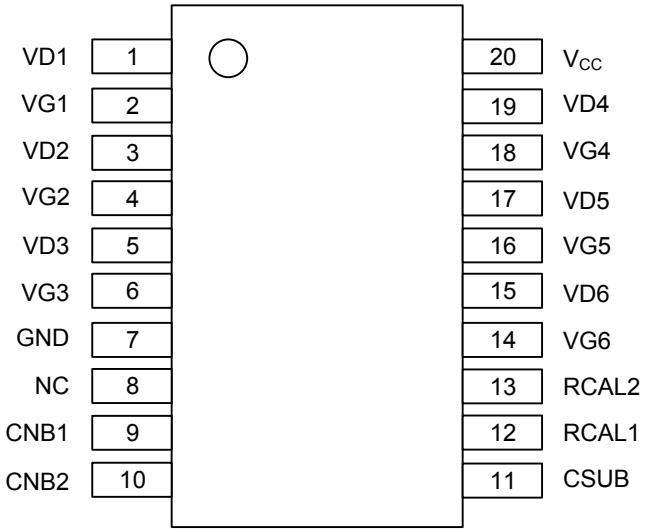
Ordering Number		Package	Packing
Lead Free	Halogen Free		
L8001L-R20-R	L8001G-R20-R	SSOP-20	Tape Reel

L8001G-R20-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) SSOP-20 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



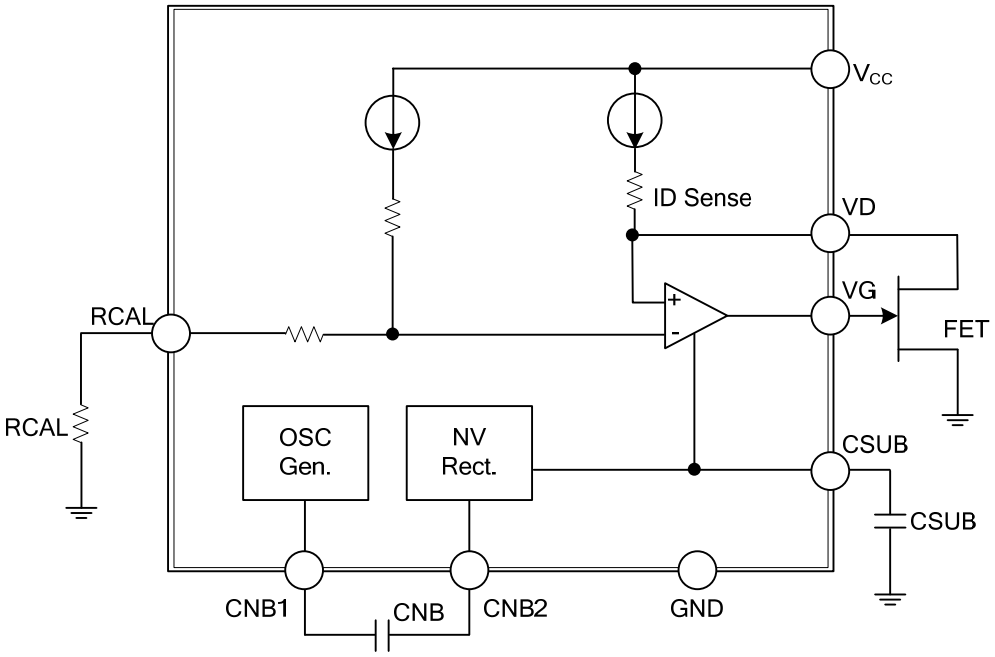
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	VD1	1st Drain output voltage
2	VG1	1st Gate output voltage
3	VD2	2nd Drain output voltage
4	VG2	2nd Gate output voltage
5	VG3	3rd Gate output voltage
6	VD3	3rd Drain output voltage
7	GND	Ground
8	NC	No connect
9	CNB1	OSC output
10	CNB2	Rectifier Input
11	CSUB	Negative voltage output
12	RCAL1	VD1/VD2/VD3 current set resistor connect
13	RCAL2	VD4/VD5/VD6 current set resistor connect
14	VG6	6th Gate output voltage
15	VD6	6th Drain output voltage
16	VG5	5th Gate output voltage
17	VD5	5th Drain output voltage
18	VG4	4th Gate output voltage
19	VD4	4th Drain output voltage
20	V_{CC}	Supply voltage

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.6 ~ 8	V
Supply Current	I_{CC}	100	mA
Maximum Drain Current	I_D	15	mA
Maximum CSUB Sink Current	I_{CSUB}	-500	uA
Operating Temperature	T_{OPR}	-40 ~ 80	°C
Storage Temperature	T_{STG}	-50 ~ 150	°C

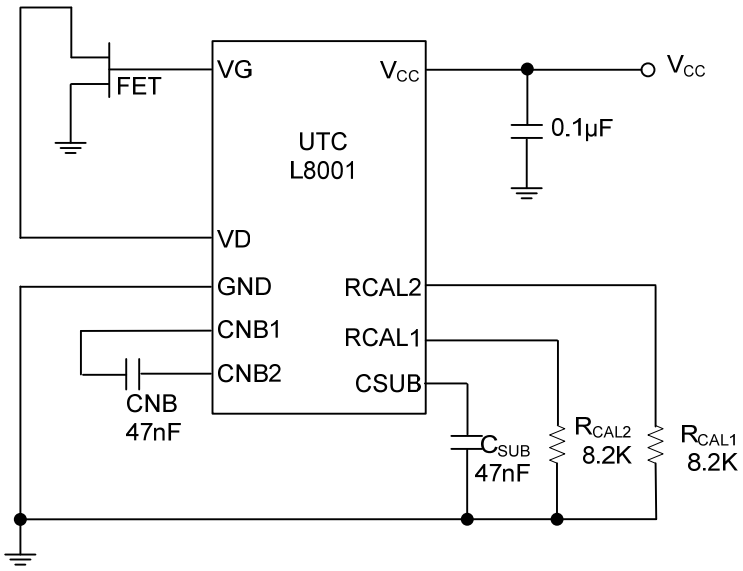
Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS

(V_{CC}=3.3V, I_D=10mA, R_{CAL1}=8.2KΩ, R_{CAL2}=8.2KΩ, T_A=25°C, unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		3.3		6	V
Supply Current	I_{CC}	No FET			10	mA
Negative Voltage	V_{SUB}	I_{SUB}=0uA, V_{CC}=6V	-3.0	-2.5	-1	V
		I_{SUB}=-200uA			-1	V
Oscillator Freq.	f_O		200	350	800	KHz
Drain Current	I_D		8	10	12	mA
Drain Current Change with V_{CC}	ΔI_{DV}	V_{CC}=3.3~6V		0.2		%/V
VD1/VD2/VD3/VD4/VD5/VD6 Drain Offset Current	ΔI_{DC}			0.2		mA
Drain Current Change with Temp.	ΔI_{DT}	T=-40~80°C		0.1		%/°C
Drain Voltage	V_D	I_D=10mA	1.8	2	2.2	V
Drain Voltage Change with V_{CC}	ΔV_{DV}	V_{CC}=3.3~6V		0.5		%/V
Drain Voltage Change	ΔV_{DT}	T=-40~80°C		50		ppm
Dynamic Gate Voltage Range	V_G	Csub without loading	-2.5		0.7	V
Drain Output Noise Voltage	V_{dn}	With drain bypass capacitor=10nF			0.05	V_{PP}
Gate Output Noise Voltage	V_{GN}	With gate bypass capacitor=10nF			0.03	V_{PP}

■ TYPICAL APPLICATION CIRCUIT



There are three major functions provided by L8001G: support negative voltage, bias control circuit, and FET protesting circuit.

The negative voltage is generated using internal oscillator. It only needs an ac coupled capacitor C_{NB} 47nF and a negative voltage bypass capacitor C_{SUB} 47nF.

The bias control circuit is used to establish a stable bias current for FETs. It's bias current can be adjusted by external resistor Rcal.Rcal1 resistor is used to set I_{D1}, I_{D2}, I_{D3} in L8001G. Rcal2 resistor is used to set I_{D4}, I_{D5}, I_{D6} in L8001G. if the same drain current is required for all FETs then pins Ical1 and Ical2 can be wired together and shunted to ground by a single resistor of half normal value.

The L8001G devices have been designed to protect the external FETs from adverse operating conditions. With a JFET connected to any bias circuit, the gate output voltage of the bias circuit can not exceed the range -2.5V to 0.7V, under any conditions including powerup and powerdown transients. Should the negative bias generator be shorted or overloaded so that the drain current of the external FETs can no longer be controlled, the drain supply to FETs is shut down to avoid damage to the FETs by excessive drain current. The following diagrams show the L8001G in typical LNB applications. Within each FET gain stage the numbering system indicates how the bias stages relate to the application circuits. This is important when RCAL values are used to set differing drain currents.

■ TYPICAL APPLICATION CIRCUIT