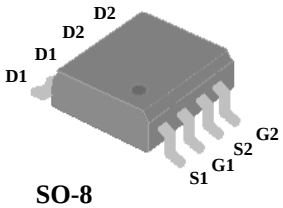
AP3700M

Halogen-Free Product

Advanced Power Electronics Corp.

N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

- ▼ **Simple Drive Requirement**
- ▼ **Low Gate Charge**
- ▼ **Fast Switching Performance**
- ▼ **RoHS Compliant & Halogen-Free**



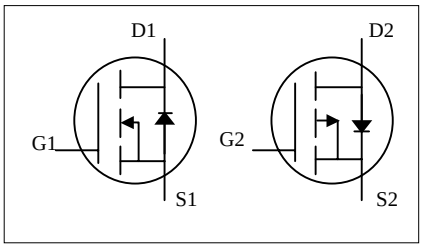
SO-8

N-CH	BV_{DSS}	30V
	$R_{DS(ON)}$	20mΩ
	I_D	7.8A
P-CH	BV_{DSS}	-30V
	$R_{DS(ON)}$	45mΩ
	I_D	-5.5A

Description

AP3700 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The SO-8 package is widely preferred for all commercial-industrial surface mount applications using infrared reflow technique and suited for voltage conversion or switch applications.



Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D@T_A=25℃	Drain Current, V_{GS} @ 10V[3]	7.8	-5.5	A
I_D@T_A=70℃	Drain Current, V_{GS} @ 10V[3]	6.2	-4.4	A
I_{DM}	Pulsed Drain Current[1]	20	-20	A
P_D@T_A=25℃	Total Power Dissipation	2		W
T_{STG}	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	62.5	℃/W

N-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=7A	-	-	20	mΩ
		V_{GS}=4.5V, I_D=6A	-	-	35	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1.4	-	2.2	V
g_{fs}	Forward Transconductance	V_{DS}=5V, I_D=7A	-	23	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V, V_{GS}=0V	-	-	10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge	I_D=6A	-	5	8	nC
Q_{gs}	Gate-Source Charge	V_{DS}=15V	-	1.7	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=4.5V	-	1.9	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=15V	-	7	-	ns
t_r	Rise Time	I_D=1A	-	7	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=6Ω	-	16	-	ns
t_f	Fall Time	V_{GS}=10V	-	4	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	550	880	pF
C_{oss}	Output Capacitance	V_{DS}=15V	-	90	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	60	-	pF
R_g	Gate Resistance	f=1.0MHz	-	2.5	5	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=1.5A, V_{GS}=0V	-	-	1.2	V
t_{rr}	Reverse Recovery Time	I_S=7A, V_{GS}=0V	-	10	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	3	-	nC

P-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V, I_D=-5A	-	-	45	mΩ
		V_{GS}=-4.5V, I_D=-4A	-	-	85	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1	-	-2	V
g_{fs}	Forward Transconductance	V_{DS}=-5V, I_D=-5A	-	8.5	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-24V, V_{GS}=0V	-	-	-10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge	I_D=-4A	-	5.8	9.3	nC
Q_{gs}	Gate-Source Charge	V_{DS}=-15V	-	1.9	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=-4.5V	-	2	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=-15V	-	9	-	ns
t_r	Rise Time	I_D=-1A	-	8	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=6Ω	-	28	-	ns
t_f	Fall Time	V_{GS}=-10V	-	14	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	610	980	pF
C_{oss}	Output Capacitance	V_{DS}=-15V	-	100	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	70	-	pF
R_g	Gate Resistance	f=1.0MHz	-	11	22	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=-1.5A, V_{GS}=0V	-	-	-1.2	V
t_{rr}	Reverse Recovery Time	I_S=-5A, V_{GS}=0V	-	11	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=-100A/μs	-	4	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board, t ≤10sec ; 135 ℃/W when mounted on Min. copper pad.

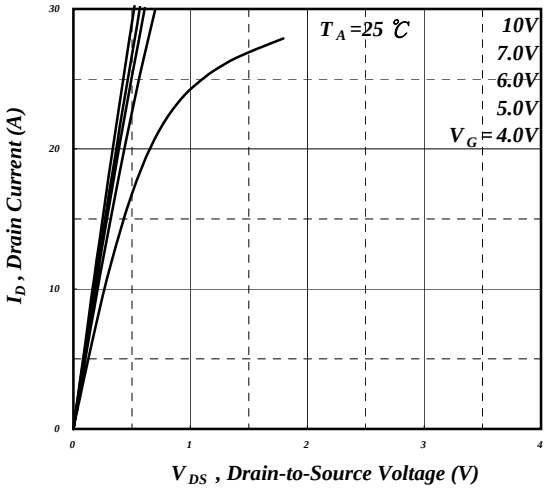


Fig 1. Typical Output Characteristics

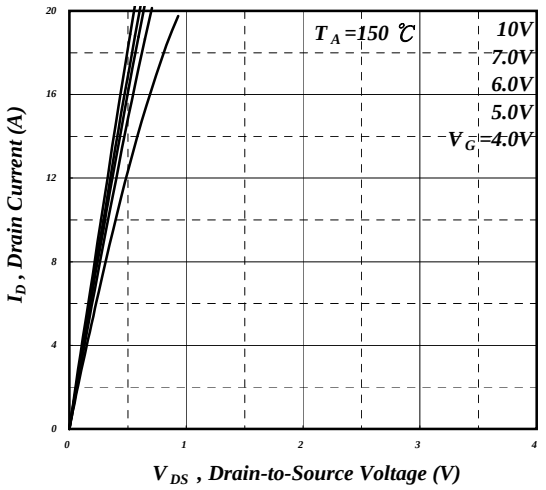


Fig 2. Typical Output Characteristics

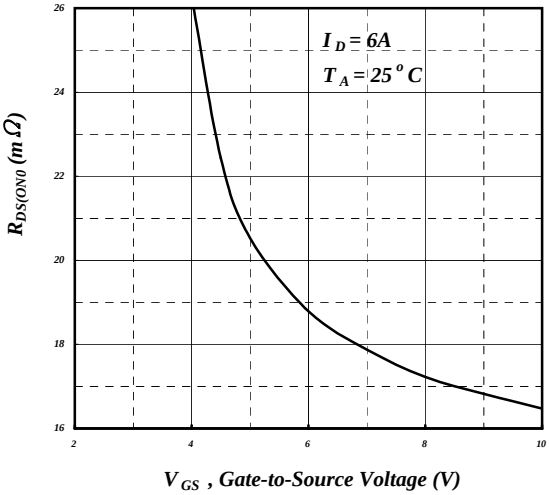


Fig 3. On-Resistance v.s. Gate Voltage

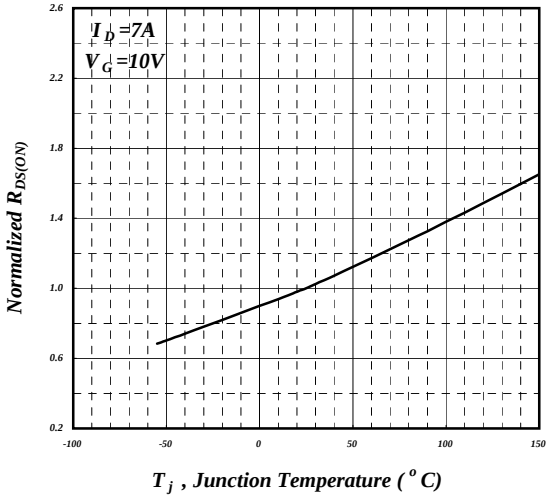


Fig 4. Normalized On-Resistance v.s. Junction Temperature

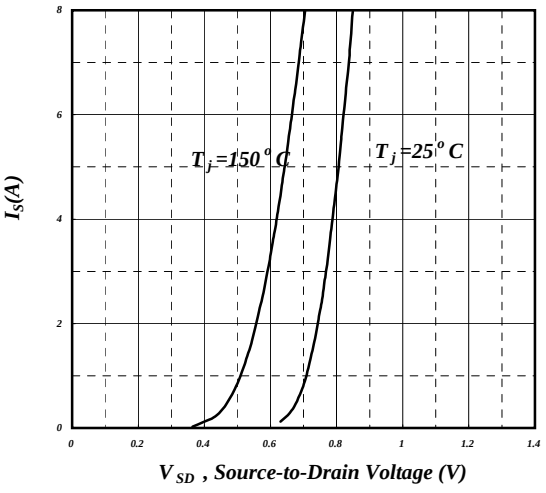


Fig 5. Forward Characteristic of Reverse Diode

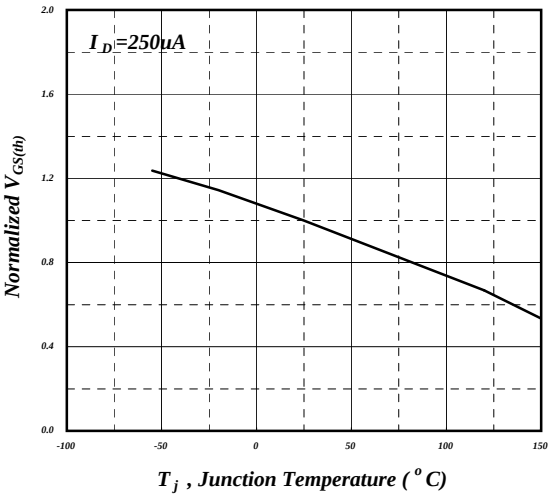


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

N-Channel

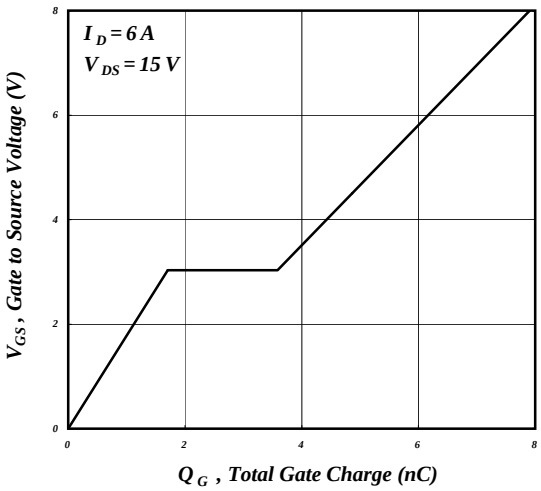


Fig 7. Gate Charge Characteristics

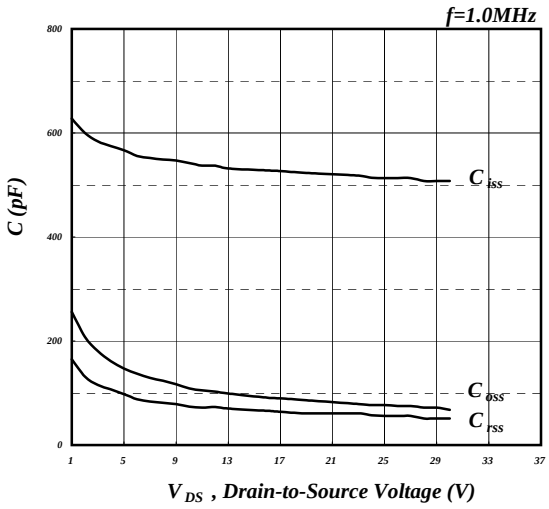


Fig 8. Typical Capacitance Characteristics

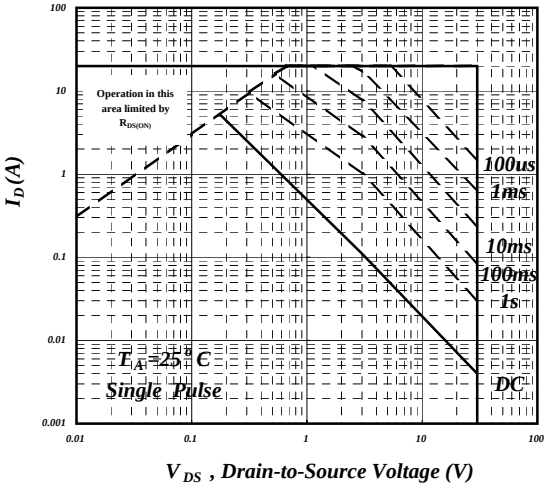


Fig 9. Maximum Safe Operating Area

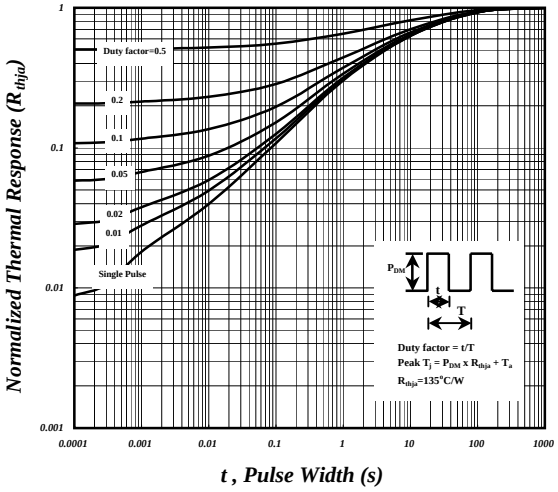


Fig 10. Effective Transient Thermal Impedance

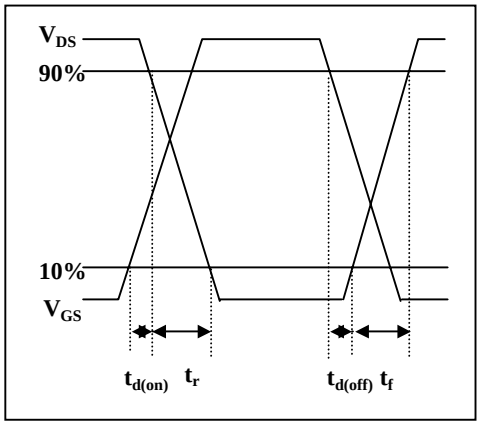


Fig 11. Switching Time Waveform

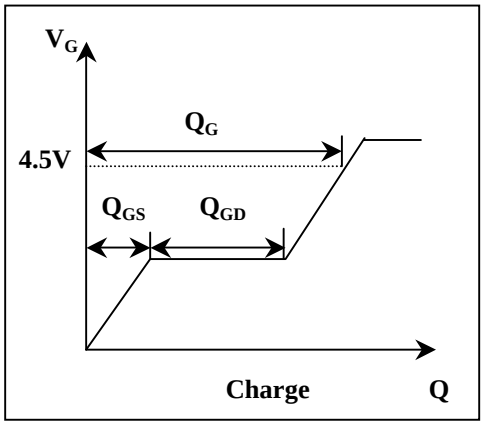


Fig 12. Gate Charge Waveform

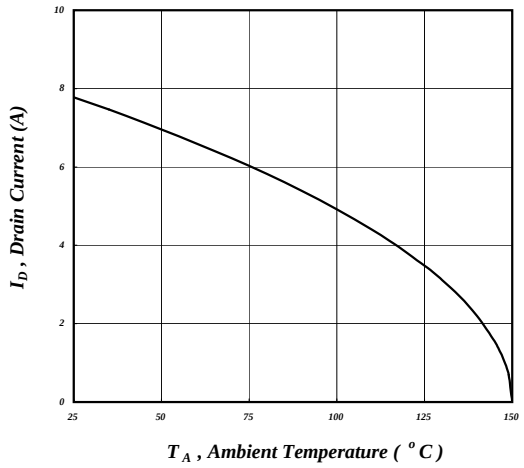


Fig 13. Drain Current v.s. Ambient Temperature

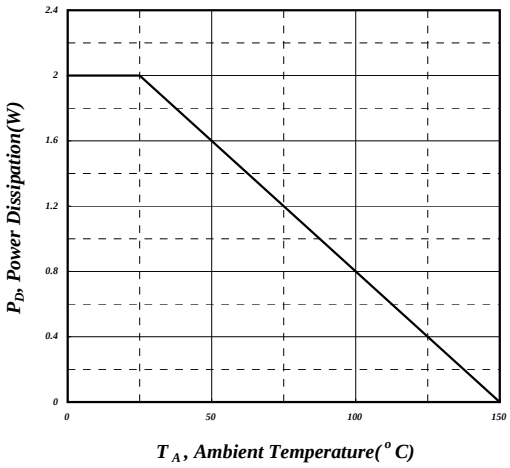


Fig 14. Total Power Dissipation

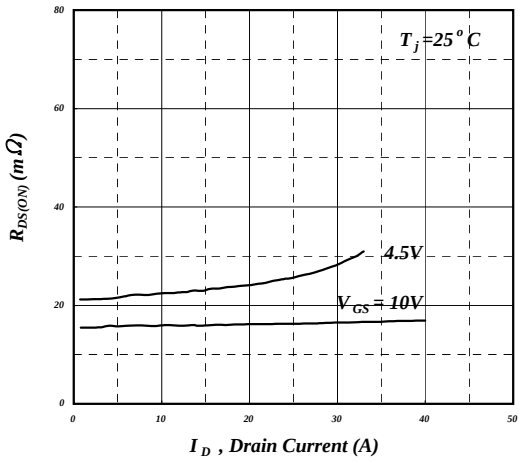


Fig 15. Typ. Drain-Source on State Resistance

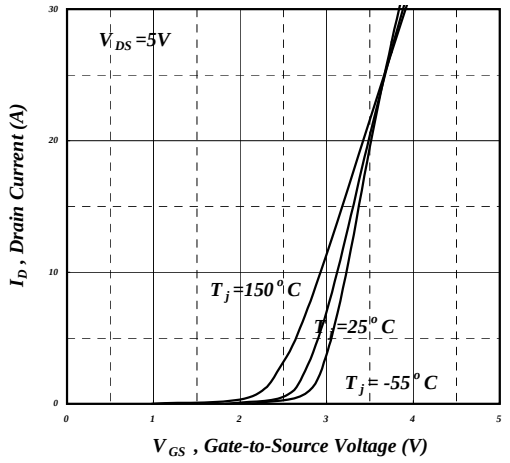


Fig 16. Transfer Characteristics

P-Channel

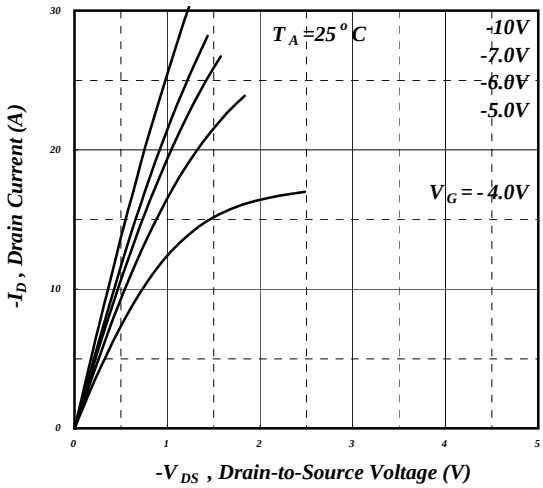


Fig 1. Typical Output Characteristics

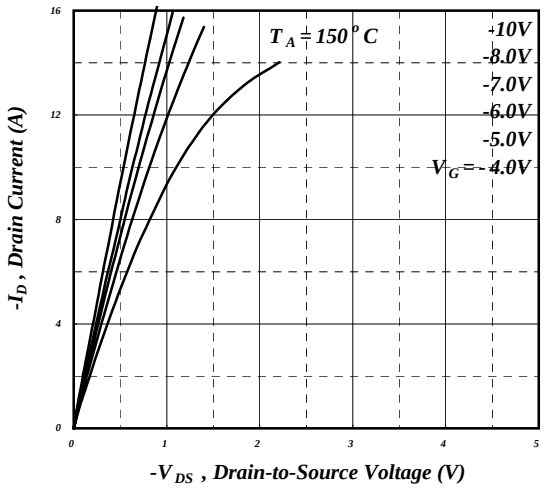


Fig 2. Typical Output Characteristics

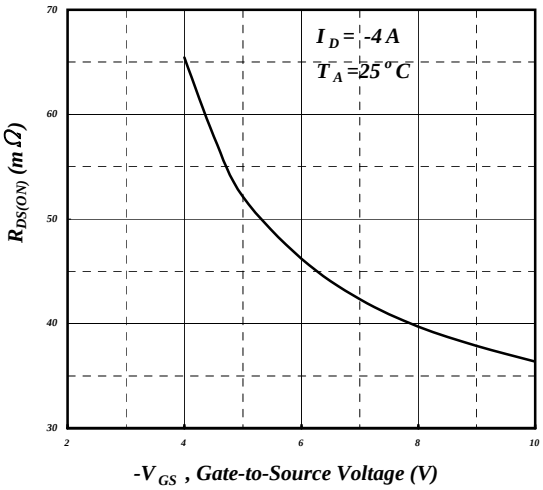


Fig 3. On-Resistance v.s. Gate Voltage

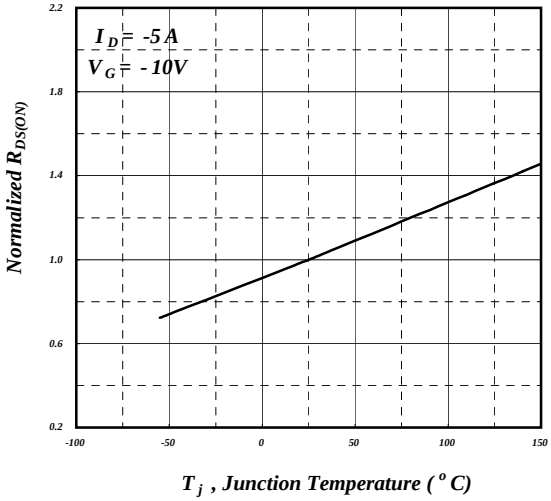


Fig 4. Normalized On-Resistance v.s. Junction Temperature

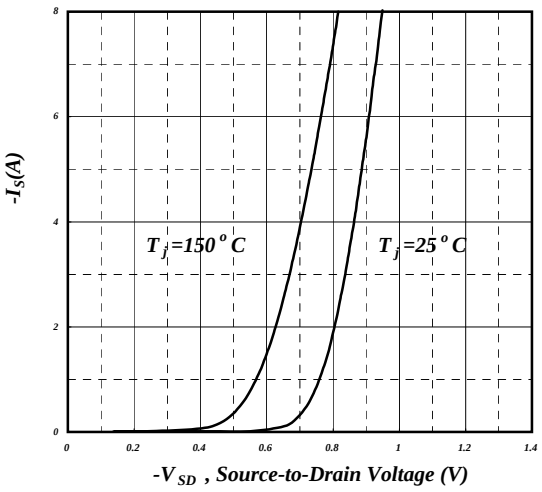


Fig 5. Forward Characteristic of Reverse Diode

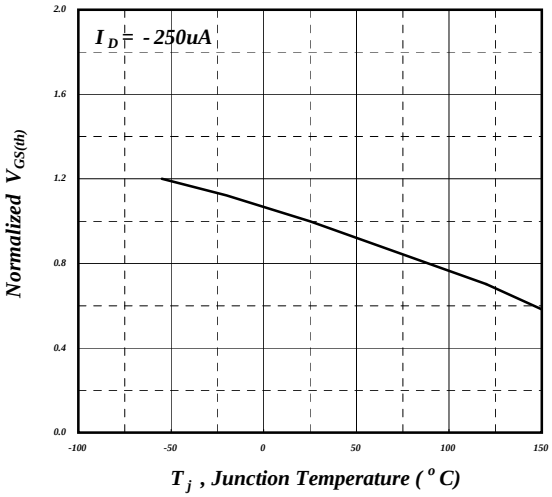


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

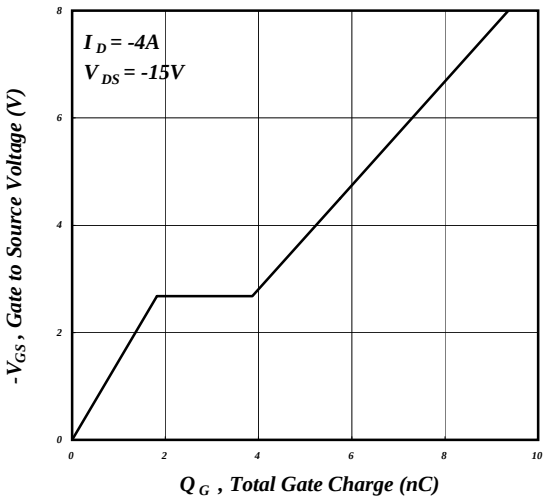


Fig 7. Gate Charge Characteristics

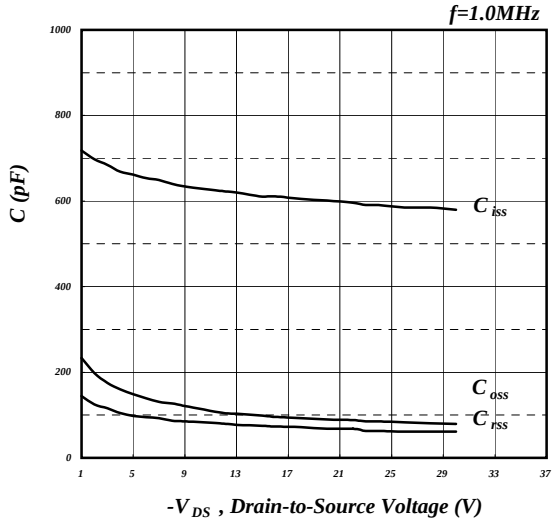


Fig 8. Typical Capacitance Characteristics

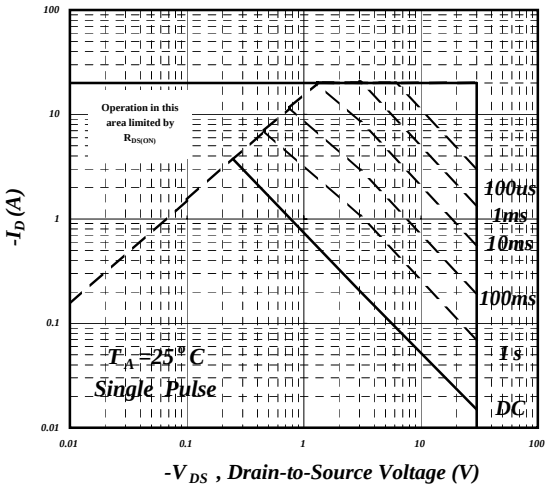


Fig 9. Maximum Safe Operating Area

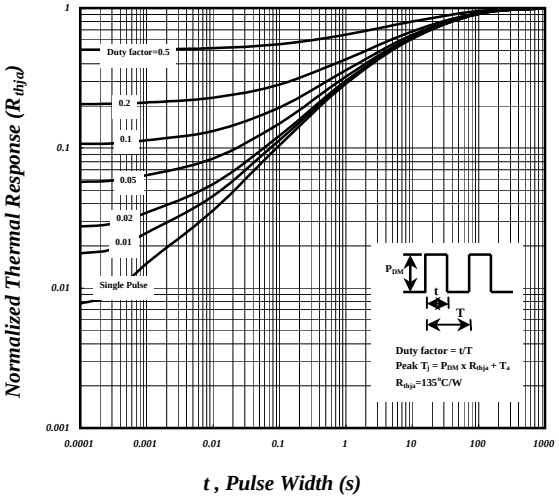


Fig 10. Effective Transient Thermal Impedance

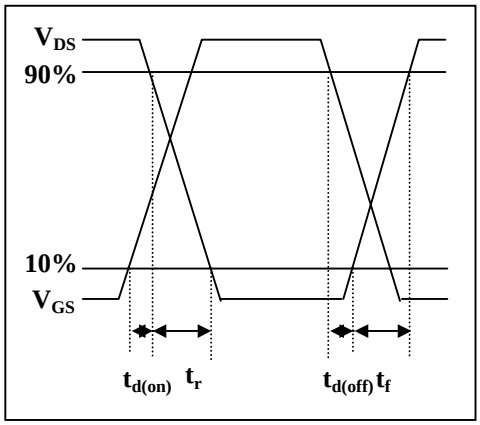


Fig 11. Switching Time Waveform

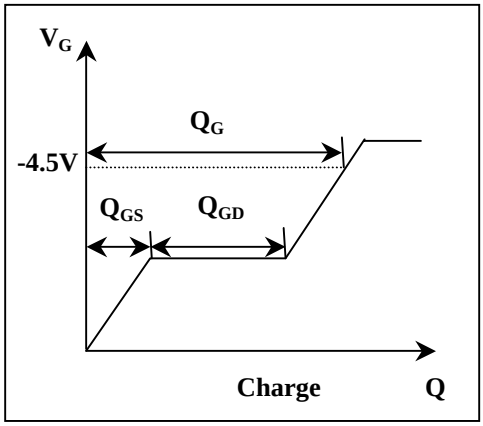


Fig 12. Gate Charge Waveform

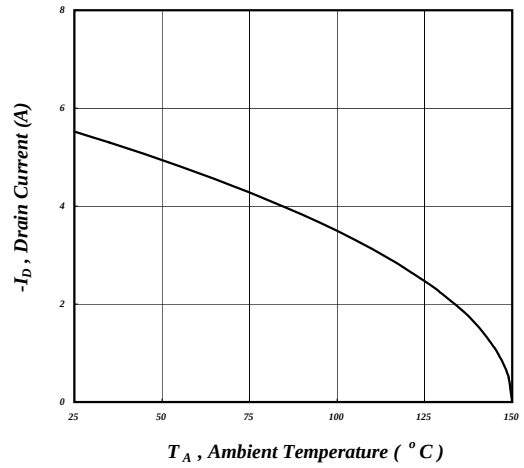


Fig 13. Drain Current v.s. Ambient Temperature

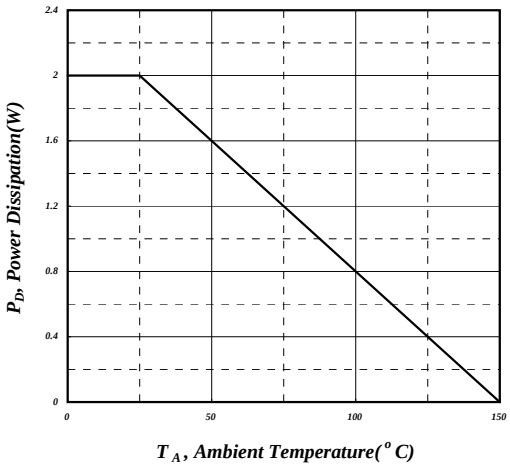


Fig 14. Total Power Dissipation

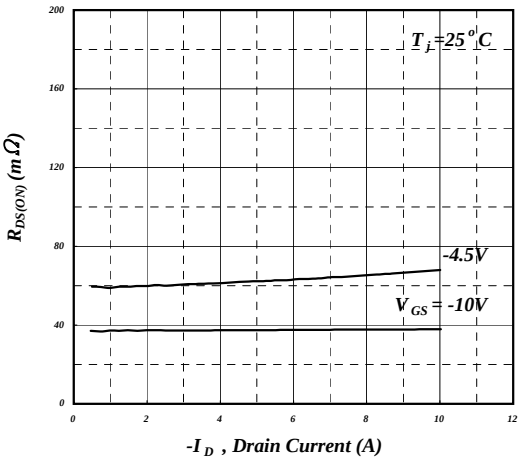


Fig 15. Typ. Drain-Source on State Resistance

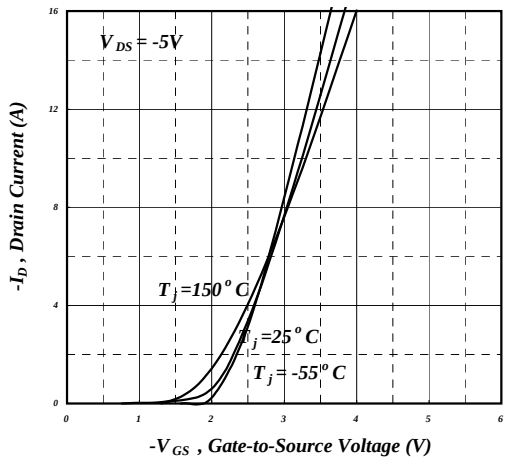


Fig 16. Transfer Characteristics

MARKING INFORMATION