

# Spread-Spectrum Crystal Multiplier

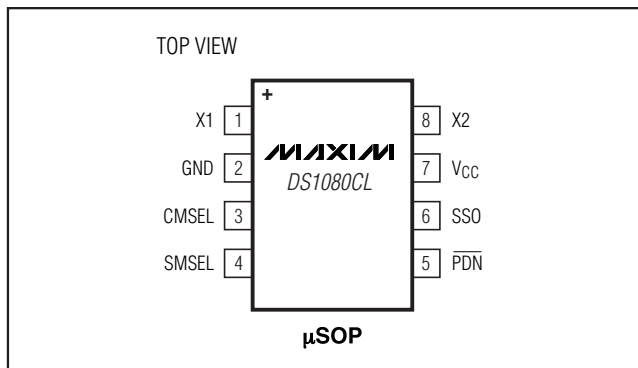
## General Description

The DS1080CL is a low-jitter, crystal-based clock generator with an integrated phase-locked loop (PLL) to generate spread-spectrum clock outputs from 8MHz to 64MHz. The device is pin programmable to select the clock multiplier rate as well as the dither magnitude. The DS1080CL has a spread-spectrum disable mode and a power-down mode to conserve power.

## Applications

Automotive	Copiers
Cable Modems	Infotainment
Cell Phones	PCs
Computer Peripherals	Printers

## Pin Configuration



## Features

- ◆ Generates Spread-Spectrum Clocks from 8MHz to 64MHz
- ◆ Selectable Clock Multiplier Rates of 1x, 2x, and 4x
- ◆ Center Spread-Spectrum Dithering
- ◆ Selectable Spread-Spectrum Modulation Magnitudes of  $\pm 0.5\%$ ,  $\pm 1.0\%$ , and  $\pm 1.5\%$
- ◆ Spread-Spectrum Disable Mode
- ◆ Low Cycle-to-Cycle Jitter
- ◆ Power-Down Mode with High-Impedance Output
- ◆ Low-Power Consumption
- ◆ 3.0V to 3.6V Single-Supply Operation
- ◆  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Temperature Operation
- ◆ Small 8-Pin  $\mu\text{SOP}$  Package

## Ordering Information

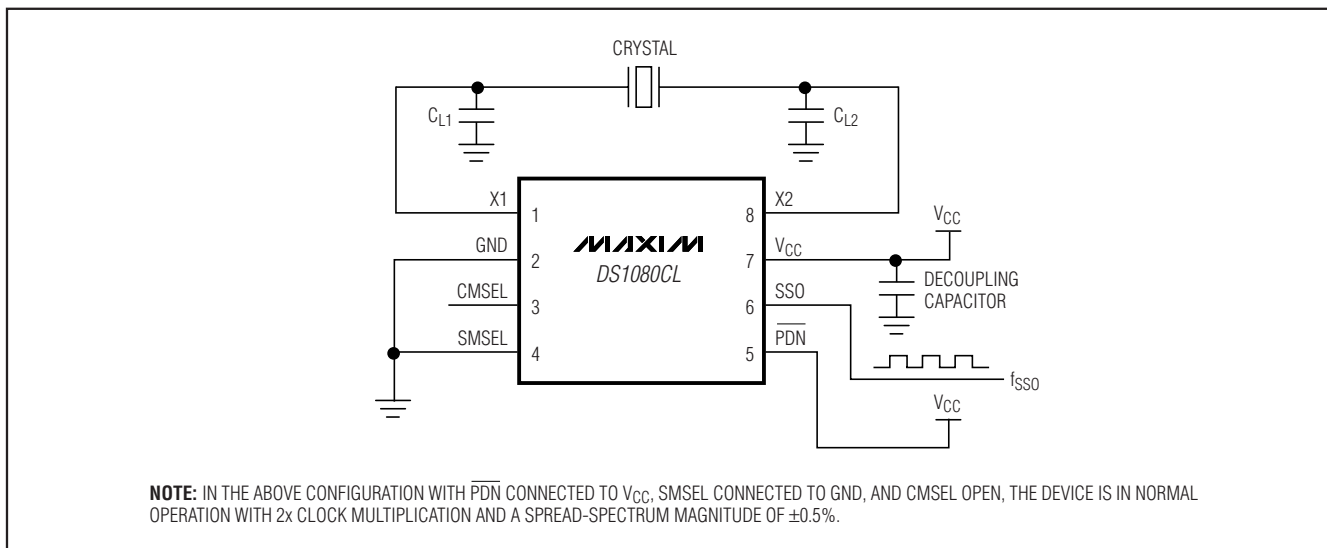
PART	TEMP RANGE	PIN-PACKAGE
DS1080CLU+	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	8 $\mu\text{SOP}$
DS1080CLU+T	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	8 $\mu\text{SOP}$
DS1080CLU/V+	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	8 $\mu\text{SOP}$
DS1080CLU/V+T	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	8 $\mu\text{SOP}$

+Denotes a lead-free package.

/V denotes an automotive qualified part.

T = Tape and reel.

## Typical Operating Circuit



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## ABSOLUTE MAXIMUM RATINGS

Voltage Range on  $V_{CC}$  Relative to GND .....-0.5V to +3.63V  
 Voltage Range on Any Pin Relative  
 to GND .....-0.5V to ( $V_{CC} + 0.5V$ ), not to exceed +3.63V  
 Continuous Power Dissipation ( $T_A = +75^\circ\text{C}$ )  
 $\mu\text{SOP}$  (derate 4.5mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ).....362mW

Operating Temperature Range .....-40 $^\circ\text{C}$  to +125 $^\circ\text{C}$   
 Storage Temperature Range .....-55 $^\circ\text{C}$  to +125 $^\circ\text{C}$   
 Lead Temperature (soldering, 10s) .....+300 $^\circ\text{C}$   
 Soldering Temperature (reflow) .....+260 $^\circ\text{C}$

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## RECOMMENDED OPERATING CONDITIONS

( $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	$V_{CC}$	(Note 1)	3.0		3.6	V
Input Logic 1	$V_{IH}$		0.8 x $V_{CC}$		$V_{CC} +$ 0.3	V
Input Logic 0	$V_{IL}$		$V_{GND} -$ 0.3		0.2 x $V_{CC}$	V
Input Logic Open	$I_{IF}$	$0V < V_{IN} < V_{CC}$ (Note 2)			$\pm 1$	$\mu\text{A}$
Input Leakage	$I_{IL}$	$0V < V_{IN} < V_{CC}$ (Note 3)			$\pm 80$	$\mu\text{A}$
SSO Load	$C_{SSO}$				15	pF
Crystal or Clock Input Frequency	$f_{IN}$		8		16	MHz
Crystal ESR	$X_{ESR}$				90	$\Omega$
Clock Input Duty Cycle	$F_{INDC}$		40		60	%
Crystal Parallel Load Capacitance	$C_L$	(Note 4)			18	pF

## DC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +3.0V$  to  $+3.6V$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	$I_{CC1}$	$C_{SSO} = 15\text{pF}$ , $f_{SSO} = 8\text{MHz}$		7	12	mA
Power-Down Current	$I_{CCQ}$	$\overline{\text{PDN}} = \text{GND}$ , all input pins open			200	$\mu\text{A}$
Output Leakage (SSO)	$I_{OZ}$	$\overline{\text{PDN}} = \text{GND}$	-1		+1	$\mu\text{A}$
Low-Level Output Voltage (SSO)	$V_{OL}$	$I_{OL} = 4\text{mA}$			0.4	V
High-Level Output Voltage (SSO)	$V_{OH}$	$I_{OH} = -4\text{mA}$	2.4			V
Input Capacitance (X1/X2)	$C_{IN}$	(Note 5)		5		pF

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DS1080CL

## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +3.0$  to  $+3.6V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SSO Duty Cycle	SSODC	Measured at $V_{CC}/2$	45		55	%
Rise Time	$t_R$	(Note 6)		1.6		ns
Fall Time	$t_F$	(Note 6)		1.6		ns
Peak Cycle-to-Cycle Jitter	$t_J$	$f_{SSO} = 8MHz$ , $T_A = -40^{\circ}C$ to $+85^{\circ}C$ , 10,000 cycles (Note 5)		75		ps
Power-Up Time	$t_{POR}$	$\overline{PDN}$ pin (Note 7)	8MHz		20	ms
			16MHz		10	
Power-Down Time	$t_{PDN}$	$\overline{PDN}$ pin (Notes 8, 9)			100	ns
Dither Rate	$f_{DITHER}$			$f_{IN}/512$		

**Note 1:** All voltages referenced to ground.

**Note 2:** Maximum source/sink current applied to input to be considered an open.

**Note 3:** Applicable to pins CMSEL, SMSEL, and  $\overline{PDN}$ .

**Note 4:** See information about  $C_{L1}$  and  $C_{L2}$  in the *Applications Information* section.

**Note 5:** Not production tested.

**Note 6:** For 15pF load.

**Note 7:** Time between  $\overline{PDN}$  deasserted to output active.

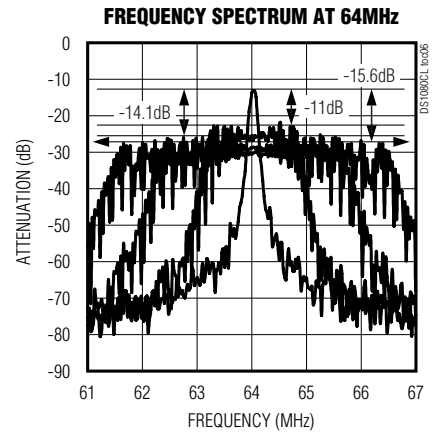
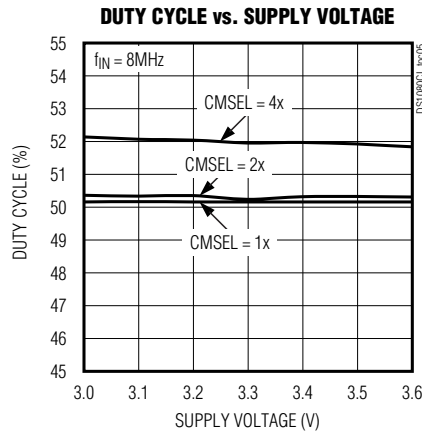
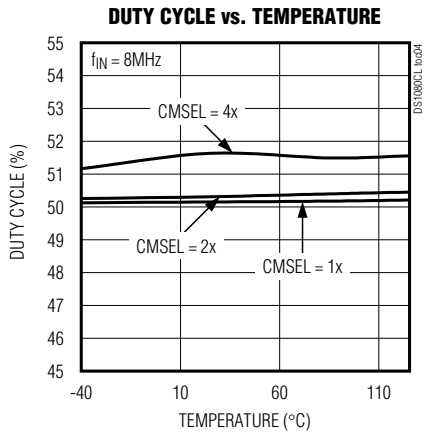
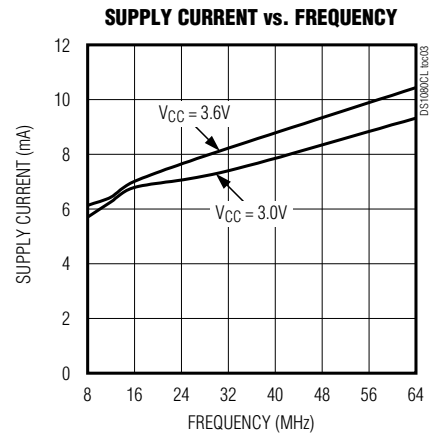
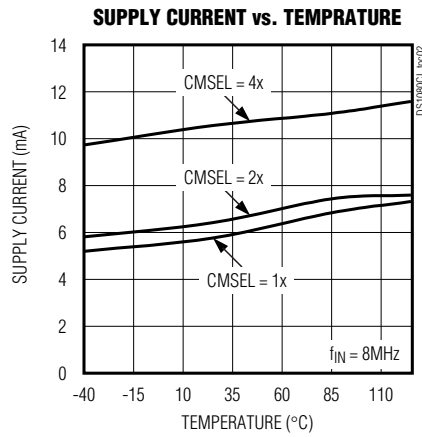
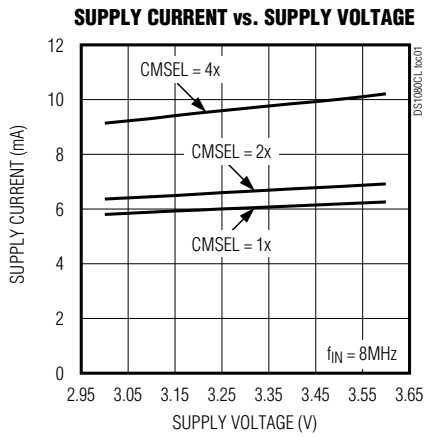
**Note 8:** Time between  $\overline{PDN}$  asserted to output high impedance.

**Note 9:** Guaranteed by design.

# Spread-Spectrum Crystal Multiplier

## Typical Operating Characteristics

( $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



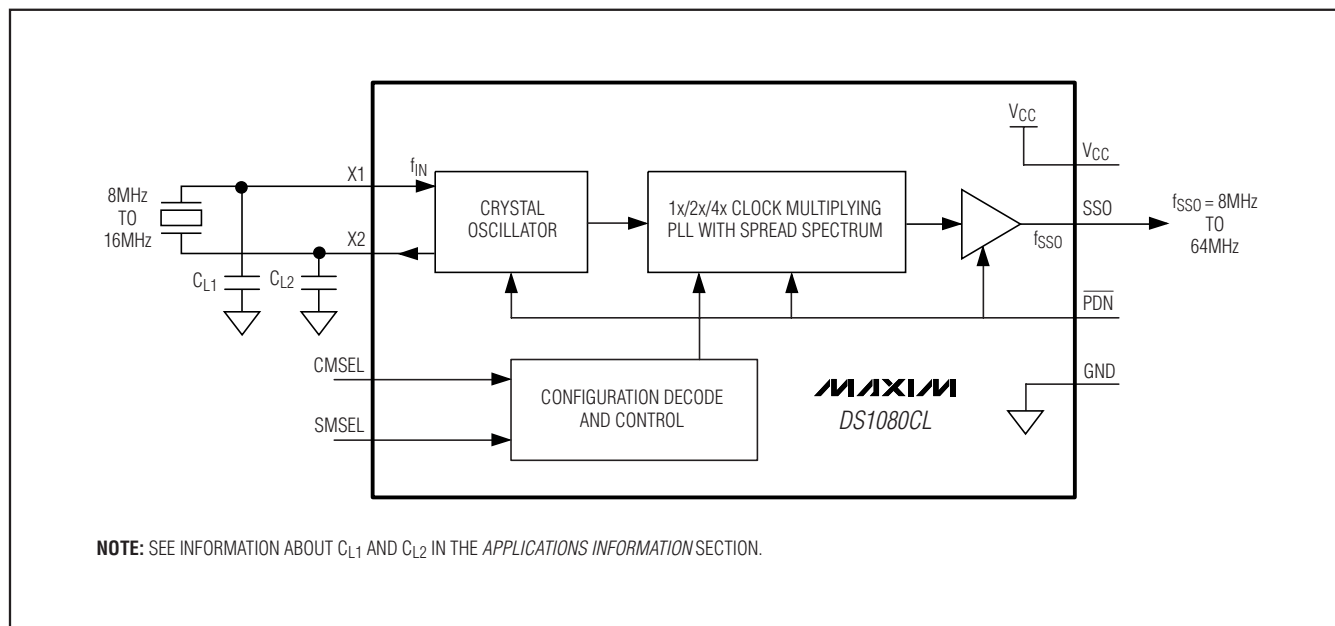
# Spread-Spectrum Crystal Multiplier

**DS1080CL**

## Pin Description

PIN	NAME	FUNCTION
1	X1	Crystal Drive/Clock Input. A crystal with the proper loading capacitors is connected across X1 and X2. Instead of a crystal, a clock can be applied at the X1 input.
2	GND	Signal Ground
3	CMSEL	Clock Multiplier Select. Trilevel digital input. 0 = 1x Open = 2x 1 = 4x
4	SMSEL	Spread-Spectrum Magnitude Select. Trilevel digital input. 0 = ±0.5% Open = ±1.0% 1 = ±1.5%
5	$\overline{\text{PDN}}$	Power-Down/Spread-Spectrum Disable. Trilevel digital input. 0 = Power-Down/SSO High Impedance Open = Power-Up/Spread Spectrum Disabled 1 = Power-Up/Spread Spectrum Enabled
6	SSO	Spread-Spectrum Clock Multiplier Output. Outputs a 1x, 2x, or 4x spread-spectrum version of the crystal or clock applied at the X1/X2 pins.
7	VCC	Supply Voltage
8	X2	Crystal Drive Output. A crystal with the proper loading capacitors is connected across X1 and X2. If a clock is connected to X1, then X2 should be left open circuit.

## Block Diagram



# Spread-Spectrum Crystal Multiplier

## Detailed Description

The DS1080CL is a crystal multiplier with center spread-spectrum capability. An 8MHz to 16MHz crystal is connected to the X1 and X2 pins. Alternately, an 8MHz to 16MHz clock can be applied to X1 in place of the crystal. In such applications, X2 would be left open circuit. Using the CMSEL input, the user selects whether the attached crystal or input clock is multiplied by 1, 2, or 4. The DS1080CL can generate spread-spectrum clocks from 8MHz to 64MHz.

The PLL can dither the output clock about its center frequency at a user-selectable magnitude. Using the

SMSEL input, the user selects the dither magnitude. The  $\overline{\text{PDN}}$  input can be used to place the device into a low-power standby mode where the SSO output is high impedance. If the  $\overline{\text{PDN}}$  pin is open, the SSO output is active but the spread-spectrum dithering is disabled. The spread-spectrum dither rate is fixed at  $f_{\text{IN}}/512$  to keep the dither rate above the audio frequency range. On power-up, the output clock (SSO) remains high impedance until the PLL reaches a stable frequency ( $f_{\text{SSO}}$ ) and dither ( $f_{\text{DITHER}}$ ). A power cycle is needed for the PLL whenever there is a change in input frequency, CMSEL, or SMSEL.

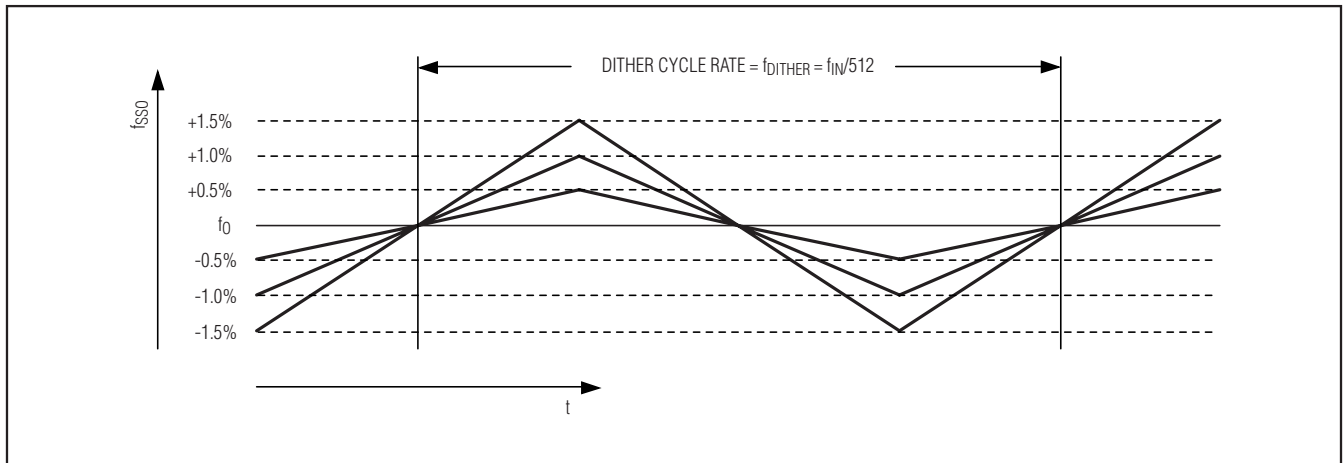


Figure 1. Spread-Spectrum Frequency Modulation

# Spread-Spectrum Crystal Multiplier

## Applications Information

### Crystal Selection

The DS1080CL requires a parallel resonating crystal operating in the fundamental mode, with an ESR of less than  $90\Omega$ . The crystal should be placed very close to the device to minimize excessive loading due to parasitic capacitances.

### Oscillator Input

When driving the DS1080CL using an external oscillator clock, consider the input (X1) to be high impedance.

### Crystal Capacitor Selection

The load capacitors  $C_{L1}$  and  $C_{L2}$  are selected based on the crystal specifications (from the data sheet of the crystal used). The crystal parallel load capacitance is calculated as follows:

$$C_L = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} + C_{IN} \quad (1)$$

For the DS1080CL use  $C_{L1} = C_{L2} = C_{LX}$ .

In this case, the equation then reduces to:

$$C_L = \frac{C_{LX}}{2} + C_{IN} \quad (2)$$

where  $C_{L1} = C_{L2} = C_{LX}$ .

Equation 2 is used to calculate the values of  $C_{L1}$  and  $C_{L2}$  based on values of  $C_L$  and  $C_{IN}$  noted in the electrical specifications.

### Power-Supply Decoupling

To achieve best results, it is highly recommended that a decoupling capacitor is used on the IC power-supply pins. Typical values of decoupling capacitors are  $0.001\mu\text{F}$  and  $0.1\mu\text{F}$ . Use a high-quality, ceramic, surface-mount capacitor, and mount it as close as possible to the  $V_{CC}$  and  $GND$  pins of the IC to minimize lead inductance.

### Layout Considerations

As noted earlier, the crystal should be placed very close to the device to minimize excessive loading due to parasitic capacitances. Care should also be taken to minimize loading on pins that could be open as a programming option (SMSEL and CMSEL). Coupling on inputs due to clocks should be minimized.

## Package Information

For the latest package outline information and land patterns (footprints), go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 $\mu$ SOP	U8+1	<a href="#">21-0036</a>	<a href="#">90-0092</a>

# Spread-Spectrum Crystal Multiplier

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/08	Initial release	—
1	10/11	Updated the <i>Ordering Information</i> table and the <i>Absolute Maximum Ratings</i> section; added the land pattern no. to the <i>Package Information</i> table	1, 2, 7

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