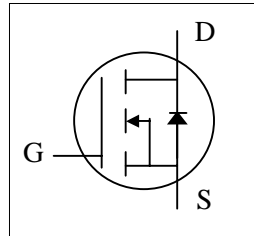




- ▼ 100% R_g & UIS Test
- ▼ Simple Drive Requirement
- ▼ Ultra Low On-resistance
- ▼ RoHS Compliant & Halogen-Free

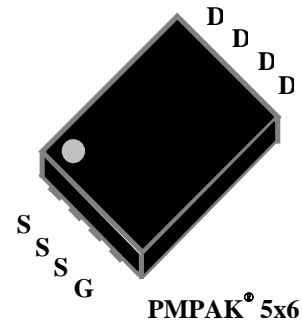


| | |
|--------------|---------------|
| BV_{DSS} | 45V |
| $R_{DS(ON)}$ | 1.8m Ω |
| I_D^4 | 180A |

Description

AP4N1R8C series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK[®] 5x6 package is special for DC-DC converters application and the foot print is compatible with SO-8 with backside heat sink and lower profile.



PMPAK[®] 5x6

Absolute Maximum Ratings @T_j=25°C (unless otherwise specified)

| Symbol | Parameter | Rating | Units |
|--------------------------------------|--|------------|-------|
| V _{DS} | Drain-Source Voltage | 45 | V |
| V _{GS} | Gate-Source Voltage | +20 / -12 | V |
| I _D @T _C =25°C | Drain Current (Chip), V _{GS} @ 10V ⁴ | 180 | A |
| I _D @T _A =25°C | Drain Current, V _{GS} @ 10V ³ | 40 | A |
| I _D @T _A =70°C | Drain Current, V _{GS} @ 10V ³ | 32 | A |
| I _{DM} | Pulsed Drain Current ¹ | 400 | A |
| P _D @T _C =25°C | Total Power Dissipation | 104 | W |
| P _D @T _A =25°C | Total Power Dissipation ³ | 5 | W |
| E _{AS} | Single Pulse Avalanche Energy ⁵ | 295 | mJ |
| T _{STG} | Storage Temperature Range | -55 to 150 | °C |
| T _J | Operating Junction Temperature Range | -55 to 150 | °C |

Thermal Data

| Symbol | Parameter | Value | Unit |
|--------------------|---|-------|------|
| R _{thj-c} | Maximum Thermal Resistance, Junction-case | 1.2 | °C/W |
| R _{thj-a} | Maximum Thermal Resistance, Junction-ambient ³ | 25 | °C/W |



AP4N1R8CMT-A

Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|--------------|--|-------------------------------|------|------|-------|-----------|
| BV_{DSS} | Drain-Source Breakdown Voltage | $V_{GS}=0V, I_D=1mA$ | 45 | - | - | V |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance ² | $V_{GS}=10V, I_D=20A$ | - | - | 1.8 | $m\Omega$ |
| | | $V_{GS}=4.5V, I_D=20A$ | - | - | 2.5 | $m\Omega$ |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}=V_{GS}, I_D=250\mu A$ | 1 | - | 3 | V |
| g_{fs} | Forward Transconductance | $V_{DS}=5V, I_D=20A$ | - | 110 | - | S |
| I_{DSS} | Drain-Source Leakage Current | $V_{DS}=32V, V_{GS}=0V$ | - | - | 10 | μA |
| I_{GSS} | Gate-Source Leakage | $V_{GS}=20V, V_{DS}=0V$ | - | - | 100 | nA |
| Q_g | Total Gate Charge | $I_D=20A$ | - | 50 | 80 | nC |
| Q_{gs} | Gate-Source Charge | $V_{DS}=20V$ | - | 19 | - | nC |
| Q_{gd} | Gate-Drain ("Miller") Charge | $V_{GS}=4.5V$ | - | 10 | - | nC |
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DS}=20V$ | - | 12 | - | ns |
| t_r | Rise Time | $I_D=20A$ | - | 55 | - | ns |
| $t_{d(off)}$ | Turn-off Delay Time | $R_G=1.6\Omega$ | - | 90 | - | ns |
| t_f | Fall Time | $V_{GS}=10V$ | - | 15 | - | ns |
| C_{iss} | Input Capacitance | $V_{GS}=0V$ | - | 7500 | 12000 | pF |
| C_{oss} | Output Capacitance | $V_{DS}=20V$ | - | 960 | - | pF |
| C_{rss} | Reverse Transfer Capacitance | $f=1.0MHz$ | - | 20 | - | pF |
| R_g | Gate Resistance | $f=1.0MHz$ | - | 2.2 | 4.4 | Ω |

Source-Drain Diode

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|----------|---------------------------------|-----------------------|------|------|------|-------|
| V_{SD} | Forward On Voltage ² | $I_S=20A, V_{GS}=0V$ | - | - | 1.3 | V |
| t_{rr} | Reverse Recovery Time | $I_S=20A, V_{GS}=0V,$ | - | 45 | - | ns |
| Q_{rr} | Reverse Recovery Charge | $di/dt=100A/\mu s$ | - | 65 | - | nC |

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Surface mounted on 1 in² copper pad of FR4 board, $t \leq 10\text{sec}$; 60°C/W at steady state.
4. Package limitation current is 100A .
5. Starting $T_j=25^{\circ}\text{C}$, $V_{DD}=30V$, $L=0.3mH$, $R_G=25\Omega$

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

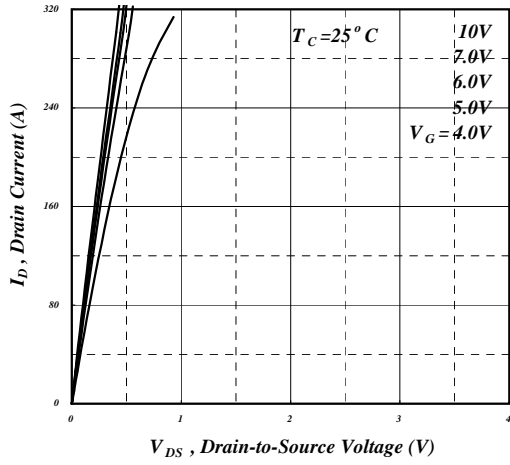


Fig 1. Typical Output Characteristics

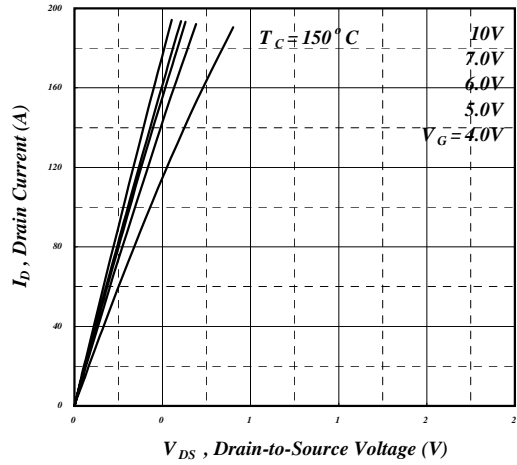


Fig 2. Typical Output Characteristics

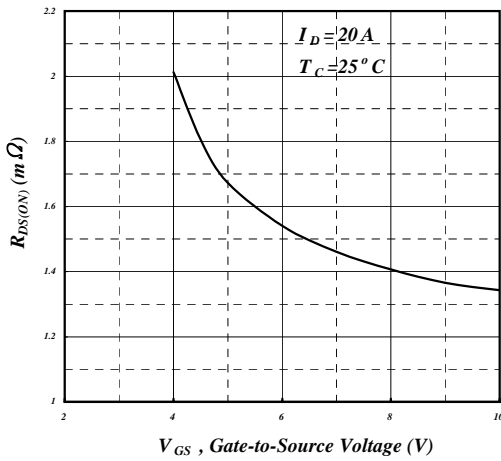


Fig 3. On-Resistance v.s. Gate Voltage

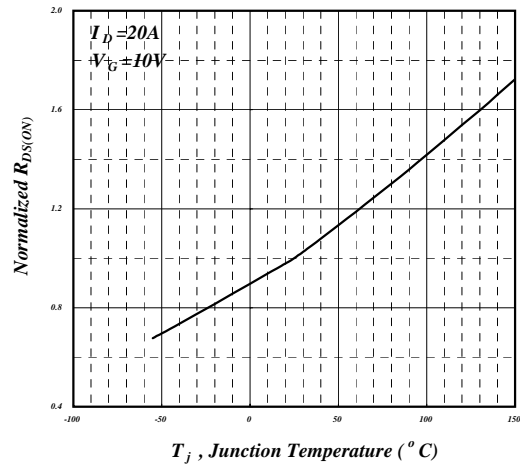


Fig 4. Normalized On-Resistance v.s. Junction Temperature

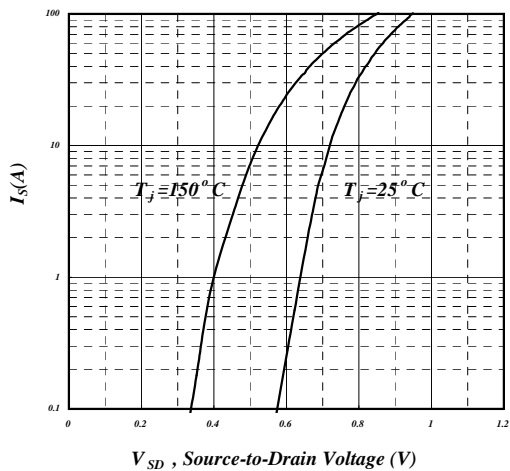


Fig 5. Forward Characteristic of Reverse Diode

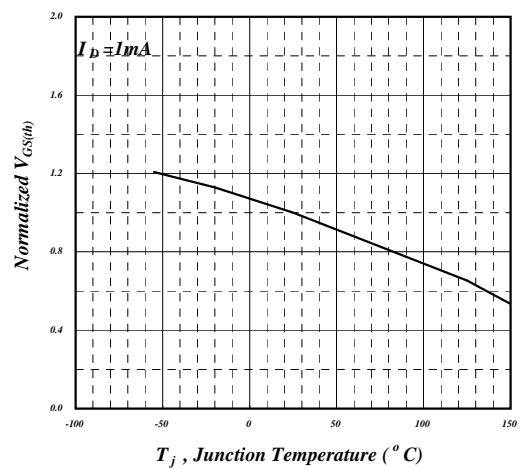


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

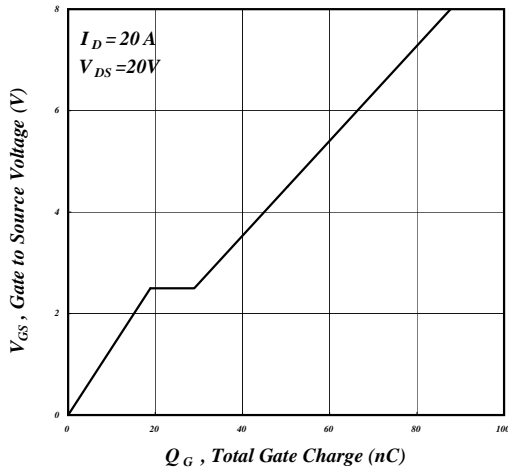


Fig 7. Gate Charge Characteristics

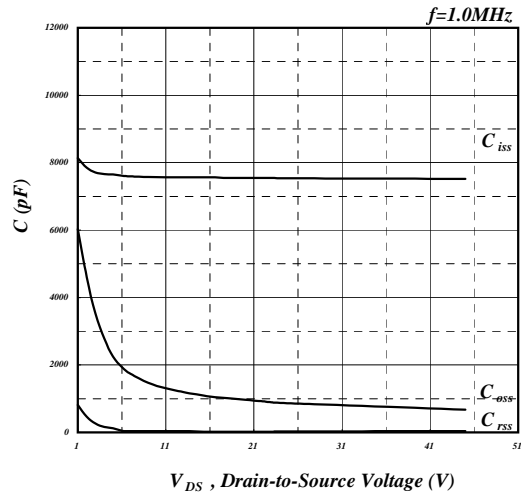


Fig 8. Typical Capacitance Characteristics

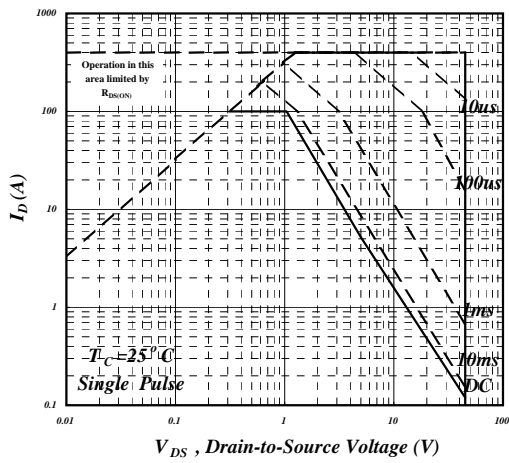


Fig 9. Maximum Safe Operating Area

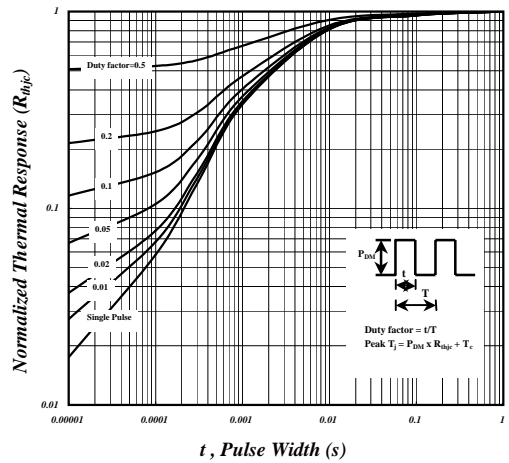


Fig 10. Effective Transient Thermal Impedance

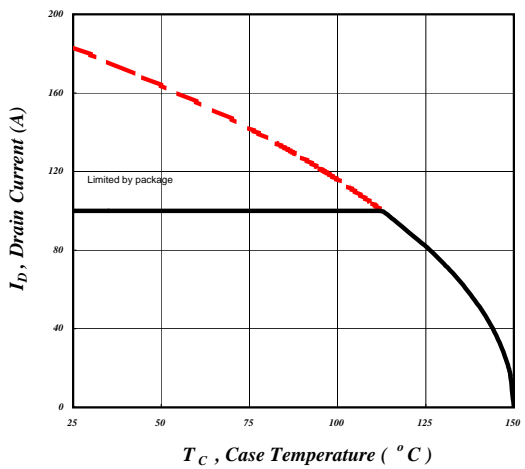


Fig 11. Drain Current v.s. Case Temperature

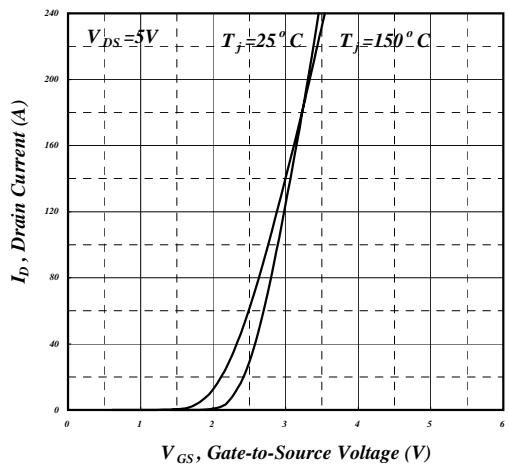


Fig 12. Transfer Characteristics

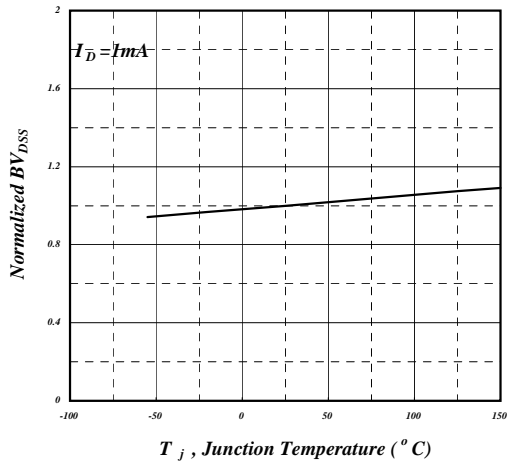


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

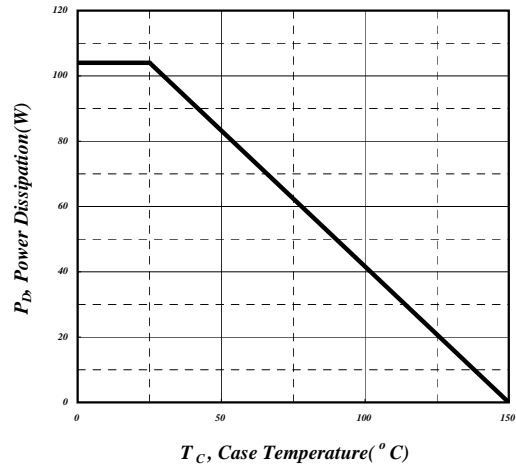


Fig 14. Total Power Dissipation

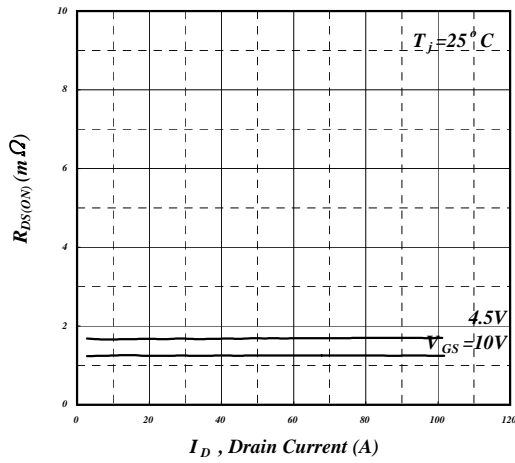
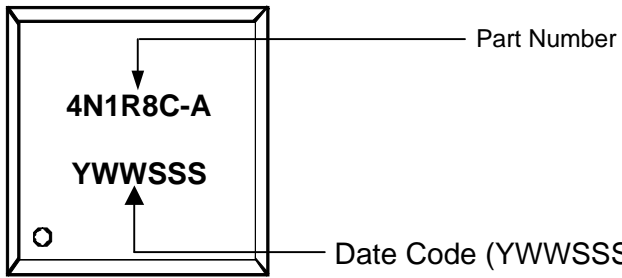


Fig 15. Typ. Drain-Source on State Resistance



AP4N1R8CMT-A

MARKING INFORMATION



Y : Last Digit Of The Year

WW : Week

SSS : Sequence