

## M2702/M2703 Series SPECIFICATION FOR 5.0x7.0mm LVPECL/LVDS SMT OSCILLATOR

### FEATURES

LVPECL/LVDS Differential Output  
Low RMS Jitter Performance 12 kHz to 20 MHz  
(1 ps max, 156.25 MHz)  
RoHS 6/6 Compliant

### APPLICATIONS

10G Reference  
NIC Card  
Ethernet  
Test and Measurement

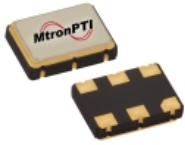
### Ordering Information:

Product Family (Supply Voltage Option)	Temperature Range		Stability		Enable/Disable		Logic Type		Package/Lead Configuration		Frequency MHz
	Code	Value	Code	Value	Code	Value	Code	Value	Code	Value	
<b>M2702</b> (3.3V) <b>M2703</b> (2.5V)	<b>6</b>	-20 °C to +70 °C	<b>3</b>	±100 ppm	<b>B</b>	Enable High (pad 1)	<b>P</b>	LVPECL	<b>N</b>	Leadless	XXX.XXXXXX
	<b>2</b>	-40 °C to +85 °C	<b>4</b>	±50 ppm			<b>L</b>	LVDS			
			<b>6</b>	±25 ppm							
			<b>8</b>	±20 ppm							
Example: M270224BPN 100.000000 MHz											
<b>M2702</b>	<b>2</b>		<b>4</b>		<b>B</b>		<b>P</b>		<b>N</b>		<b>100.000000</b>

### LVPECL Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	
Frequency of Operation	F <sub>O</sub>	10		1500	MHz		
<b>Frequency Stability</b>							
Frequency Stability	ΔF/F	See ordering information					
Aging			±2		ppm	1 <sup>st</sup> year	
<b>RF Output</b>							
Output Type		LVPECL Compatible					
Output Load		50 Ω to (V <sub>CC</sub> -2.0) V <sub>DC</sub>			V		
Symmetry (duty cycle)		45		55	%	Ref. to 50% of waveform	
Logic Level "0"	V <sub>OL</sub>	V <sub>CC</sub> -1.85		V <sub>CC</sub> -1.63	V		
Logic Level "1"	V <sub>OH</sub>	V <sub>CC</sub> -1.03		V <sub>CC</sub> -0.60	V		
Rise/Fall Time	T <sub>R</sub> /T <sub>F</sub>		0.3	0.4	ns	20% to 80% of waveform	
Start-up Time	T <sub>SU</sub>			10	ms	T <sub>ambient</sub> = +25°C	
Enable Logic (Pad 1)		70% V <sub>CC</sub> or N/C			V	Output Enabled	
Disable Logic (Pad 1)				30% V <sub>CC</sub>	V	Output Disabled to high-Z	
<b>Supply Voltage &amp; Power Consumption</b>							
Operating Voltage	V <sub>CC</sub>	3.135	3.300	3.465	V	(M2702)	
		2.375	2.500	2.625	V	(M2703)	
Supply Current	I <sub>CC</sub>			80	mA		

Revision B  
10/09/17



## M2702/M2703 Series SPECIFICATION FOR 5.0x7.0mm LVPECL/LVDS SMT OSCILLATOR

### LVDS Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	
Frequency of Operation	$F_O$	10		1500	MHz		
<b>Frequency Stability</b>							
Frequency Stability	$\Delta F/F$	See ordering information					
Aging			$\pm 2$		ppm	1 <sup>st</sup> year	
<b>RF Output</b>							
Output Type		LVDS Compatible					
Output Load		100 $\Omega$ Differential			V		
Symmetry (duty cycle)	$V_{OH}$	45		55	%	Ref. to 50% of waveform	
Differential Output Voltage	$V_{DIFF}$	175	350		mV	peak-to-peak differential output voltage	
Output Offset Voltage	$V_{OS}$		1.250		V		
Rise/Fall Time	$T_R/T_F$			0.6	ns	20% to 80% of waveform	
Start-up Time	$T_{SU}$			10	ms	$T_{ambient} = +25^\circ C$	
Enable Logic (Pad 1)		70% $V_{CC}$ or N/C			V	Output Enabled	
Disable Logic (Pad 1)				30% $V_{CC}$	V	Output Disabled to high-Z	
<b>Supply Voltage &amp; Power Consumption</b>							
Operating Voltage	$V_{CC}$	3.135	3.300	3.465	V	(M2702)	
		2.375	2.500	2.625	V	(M2703)	
Supply Current	$I_{CC}$			60	mA		

### Environmental & Packaging Requirements:

Storage Temperature	-55°C to 125°C
Mechanical Shock	Per MIL-STD-202, Method 213, Condition C (100 g's, 6 ms)
Vibration	Per MIL-STD-202, Method 204D, Condition C (10 g's, 55 – 2000 Hz)
Aging	+85°C $\pm 3^\circ C$ , 720H (No BIAS)
Humidity	+40°C $\pm 2^\circ C$ X90~95%, 96H (NO BIAS)
Thermal Cycle	Per MIL-STD-883, Method 1010, Condition B (-55 °C to +125 °C, 10 cycles)
Hermeticity	Per MIL-STD-202, Method 112 (1 x 10 <sup>-8</sup> atm cc/s of Helium)
Moisture Sensitivity Level	MSL1
Solderability	Per EIAJ-STD-002, Method 208
Max. Soldering Conditions	See solder profile, Figure 1
Pad Termination	Gold, 1 $\mu m$ maximum thickness
Package Type	6-pad 5.0 X 7.0 mm leadless ceramic. RoHS compliant.



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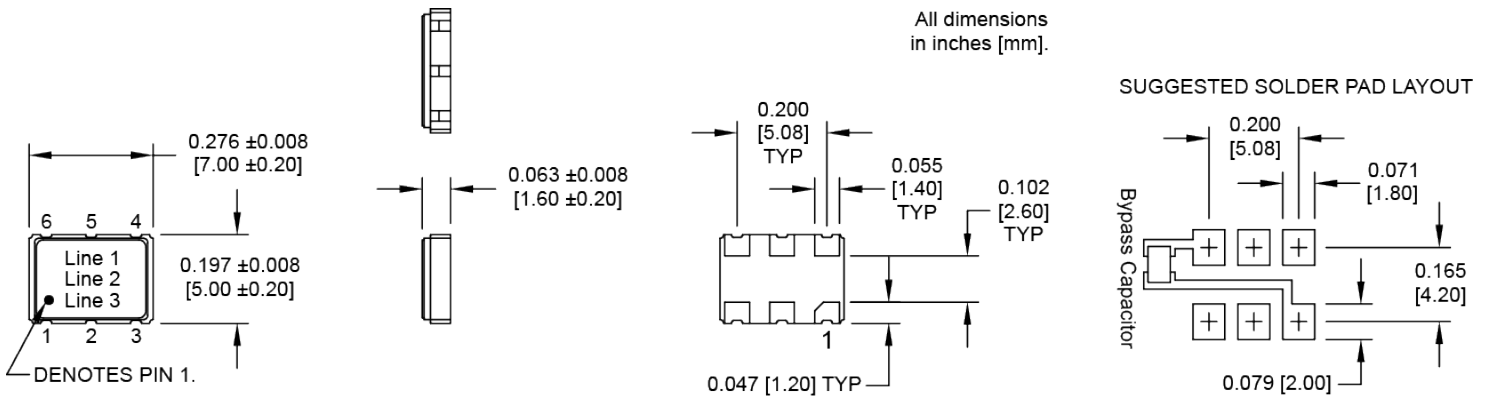
### Marking, Pin Out:

Pad	Function
1	Enable/Disable
2	No Connection
3	Ground
4	Output
5	Complementary Output
6	+V <sub>CC</sub>

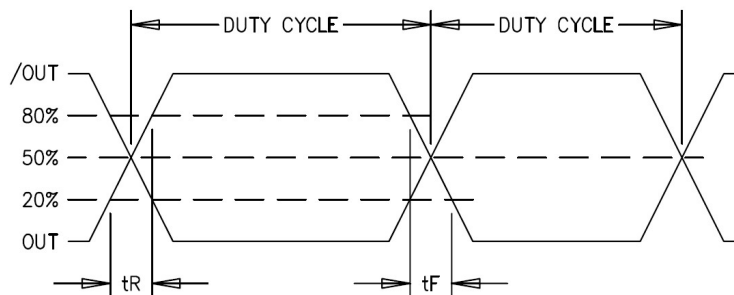
Part Marking	
Line 1	[part designation]
Line 2	FFFMFFFF
Line 3	M yy ww vv

Legend	
M	MtronPTI
F	Frequency
yy	Year
ww	Work Week
vv	Factory code

### Dimensions:



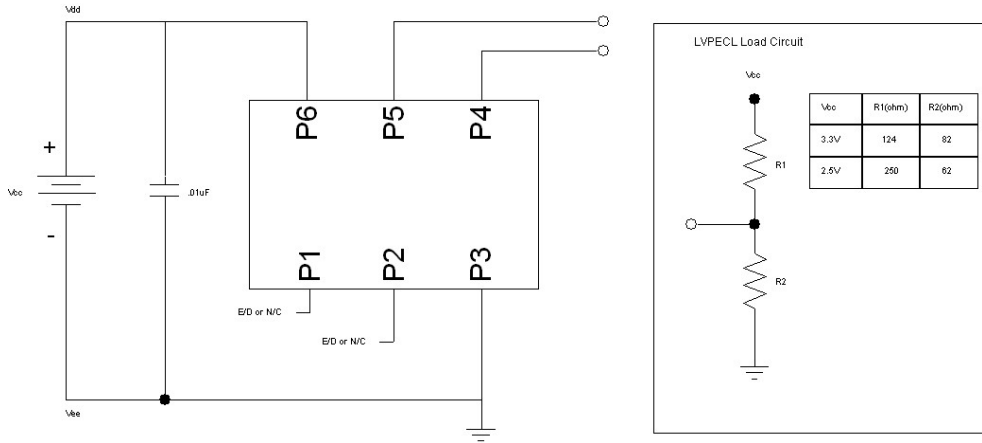
### Output Waveform:



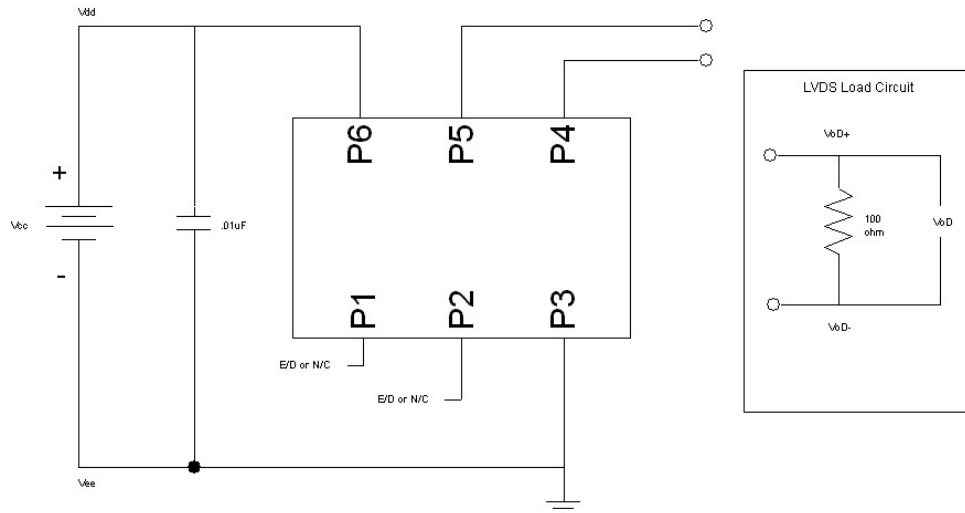


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### Typical LVPECL Test Circuit & Load Circuit Diagrams:



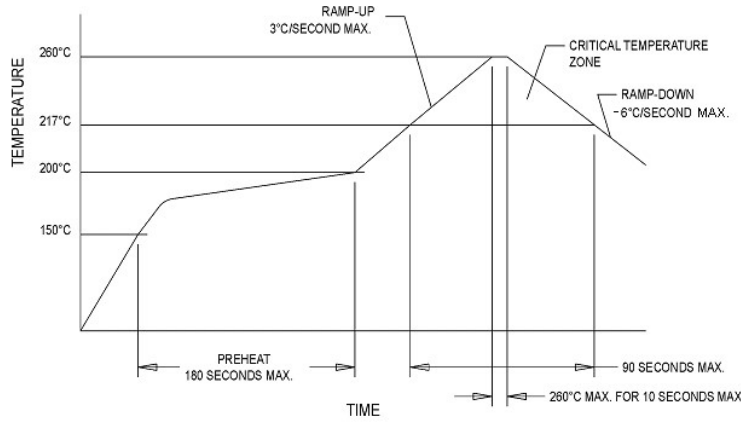
### Typical LVDS Test Circuit & Load Circuit Diagrams:





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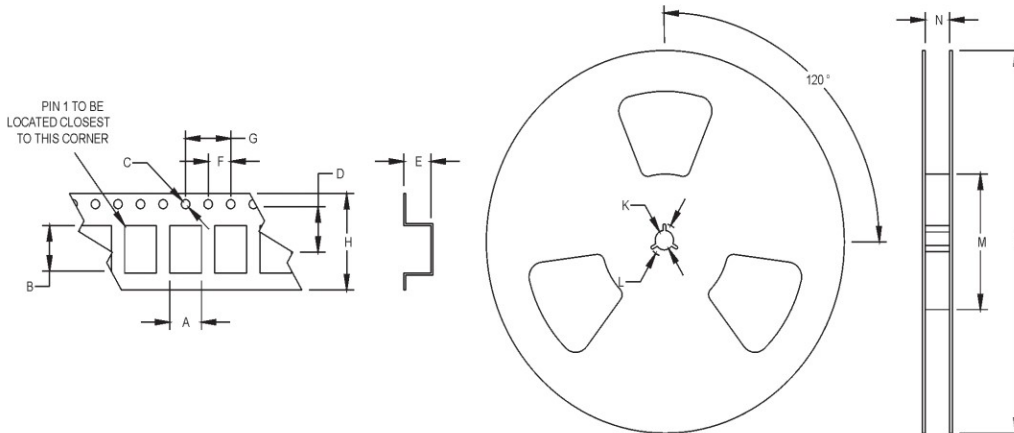
**Soldering Conditions:**



**Figure 1**

**Tape and Reel Specifications:**

All units in mm



Tape and Reel Specifications											
A	B	C	D	E	F	G	H	J	K	L	M
5.32	7.28	1.5	7.5	2.2	4	8	16	178	13.5	24.8	80