Integrated
Circuit
Systems, Inc.

ICS9169A-70

Frequency Generator for Workstation Systems

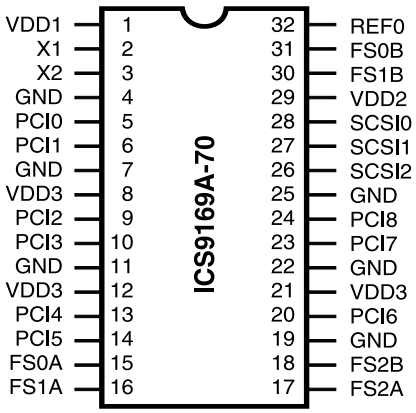
General Description

The **ICS9169A-70** is a low-cost frequency generator designed specifically for workstation or PC system clocks. The integrated buffer minimizes skew and provides all the clocks required. A 14.318 MHz XTAL oscillator provides the reference clock to generate standard Pentium frequencies. The CPU clock makes gradual frequency transitions without violating the PLL timing of internal microprocessor clock multipliers.

Features

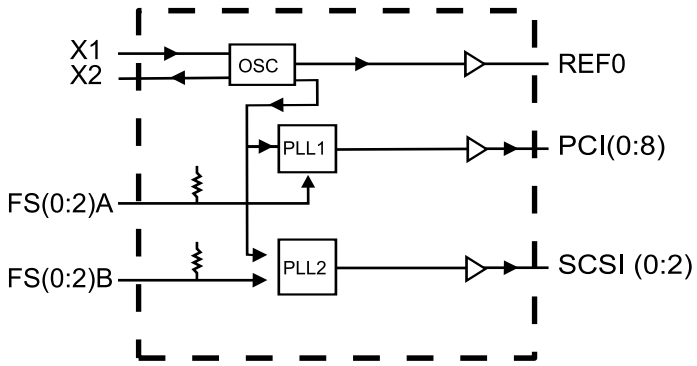
- 9 PCI outputs selectable from 30 to 66.6MHz
- 3 SCSI outputs, selectable from 10 to 80MHz
- 500ps skew window for all synchronous clock edges
- Integrated buffer outputs drive up to 30pF loads
- 500ps output to output skew window
- Buffers drive 30pF loads nominally 0.8V/ns skew rate
- 3.0V - 3.7Vsupply range
- 32-pin SOIC package
- 48 MHz clock for USB support and 24 MHz clock for FD

Pin Configuration



32-Pin SOIC

Block Diagram



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VDD1	PWR	Power for logic, PLL and output buffers.
2	X1	IN	XTAL or external reference frequency input. This input includes XTAL load capacitance and feedback bias for a 12-16 MHz crystal, nominally 14.31818 Mhz.
3	X2	OUT	XTAL output which includes XTAL load capacitance.
5,6,9,10,13,14,20,23,24	PCI(0:8)	OUT	PCI clock outputs
4,7,11,19,22,25	GND	PWR	Ground for logic, PLL and output buffers.
8,12,21	VDD3	PWR	Power for PCI clock outputs
15,16,17	FS(0:2)A	IN	Frequency multiplier select pins. See table above. These inputs have internal pull up devices.
29	VDD2	PWR	Power for SCSI clock outputs
28,27,26	SCSI (0:2)	OUT	SCSI clock outputs
31,30,18	FS(0:2)B	IN	Frequency multiplier select pins. See table next page. These inputs have internal pull up devices
32	REF0	OUT	REF is a buffered copy of the crystal oscillator or reference input clock, nominally 14.31818 MHz.

Note:
X1, X2 contain iternal 18pF crystal load cap. Intended to have external load caps of 15 to 18pF required for nominal crystal of 17 to 18pF crystal total load.

VDD = 3.3±10%, TA = 0 to 70°C
Crystal = 14.31818MHz

SCSI outputs: SCSI(0:2)

(Assume divide by 2 from VCO)

FS2B	FS1B	FS0B	Target MHz	Actual MHz	REF MHz
0	0	0	24	24	14.318
0	0	1	48	48.07	14.318
0	1	0	10	10.02	14.318
0	1	1	20	20.05	14.318
1	0	0	40	40.09	14.318
1	0	1	50	50.11	14.318
1	1	0	60	60.14	14.318
1	1	1	80	80.18	14.318

PCI outputs: PCI (0:8)

(Assume divide by 2 from VCO)

FS2A	FS1A	FS0A	Target MHz	Actual MHz	REF MHz
0	0	0	Tristate	Tristate	Tristate
0	0	1	REF/2	REF/2	REF
0	1	0	30	30.07	14.318
0	1	1	33.3	33.27	14.318
1	0	0	50	50.11	14.318
1	0	1	55	54.89	14.318
1	1	0	60	60.14	14.318
1	1	1	66.6	66.63	14.318

Note: When FS(0:2)A is 000 or 001, the Tristate and Test modes applies to all outputs for REF, PCI, and SCSI outputs.

FS2A	FS1A	FS0A	PCI	SCSI	REF
0	0	0	Tristate	Tristate	Tristate
0	0	1	REF/2[1]	REF/2[1]	REF[1]

Note: 1. In Test mode, each PLL is bypassed. The clock signal at X1 (externally driven clock or the crystal) is applied to the divider circuits.

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V

Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-10% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2.0	-	-	V
Input Low Voltage	V_{IL}		-	-	0.9	V
Input High Current	I_{IH1}	$V_{IN} = V_{DD}$	-5	0.2	5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V	-20	-50.0	-	mA
Supply Current	I_{DD}	C_L = 0 pF; Select @ 66M		50	110	mA
Input frequency	F_i	V_{DD} = 3.3 V;		14.318		MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27.0	36.0	45.0	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.		0.136	2.0	mS
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.		63.0	600	µS
Clock Overshoot[1]	T_{sh}			1.7	4.0	MHz
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	mS

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70C; $V_{DD} = V_{DDL}$ = 3.3 V +/-10%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -14 mA	2.4	2.9		V
Output Low Voltage	V_{OL1}	I_{OL} = 11 mA		0.3	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-43.0	23.0	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	20.0	31.0		mA
Rise Time	t_{r5}^1	V_{OL} = 0.8 V, V_{OH} = 2.4 V		0.7	1.5	nS
Fall Time	t_{f5}^1	V_{OH} = 2.4 V, V_{OL} = 0.8 V		0.6	1.5	nS
Duty Cycle	d_{t5}^1	V_T = 1.5 V	40	53	60	%
Jitter	t_{j1s5}^1	V_T = 1.5 V	-	182	400	pS
	t_{jabs5}^1	V_T = 1.5 V	-700	-	700	pS

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - SCSI

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-10%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -14 mA	2.4	2.9		V
Output Low Voltage	V_{OL1}	I_{OL} = 11 mA		0.3	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-43.0	23.0	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	20.0	31.0		mA
Rise Time	t_{r5}[1]	V_{OL} = 0.8 V, V_{OH} = 2.4 V		0.7	1.5	nS
Fall Time	t_{f5}[1]	V_{OH} = 2.4 V, V_{OL} = 0.8 V		0.6	1.5	nS
Duty Cycle	d_{t5}[1]	V_T = 1.5 V	45	50	55	%
Skew (window)	t_{sk1}[1]	V_T = 1.4 V	-250	-	250	pS
Jitter	t_{j1s5}[1]	V_T = 1.5 V; R_s= 33; (10 to 24 MHz Clocks)	-	200	300	pS
	t_{j1s5}[1]	V_T = 1.5 V; R_s= 33; (40 to 80 MHz Clocks)	-	90	150	pS
	t_{jabs5}[1]	V_T = 1.5 V; R_s= 33; (10 to 24 MHz Clocks)	-700	-	700	
	t_{jabs5}[1]	V_T = 1.5 V; R_s= 33; (40 to 80 MHz Clocks)	-400	-	400	pS

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - PCI

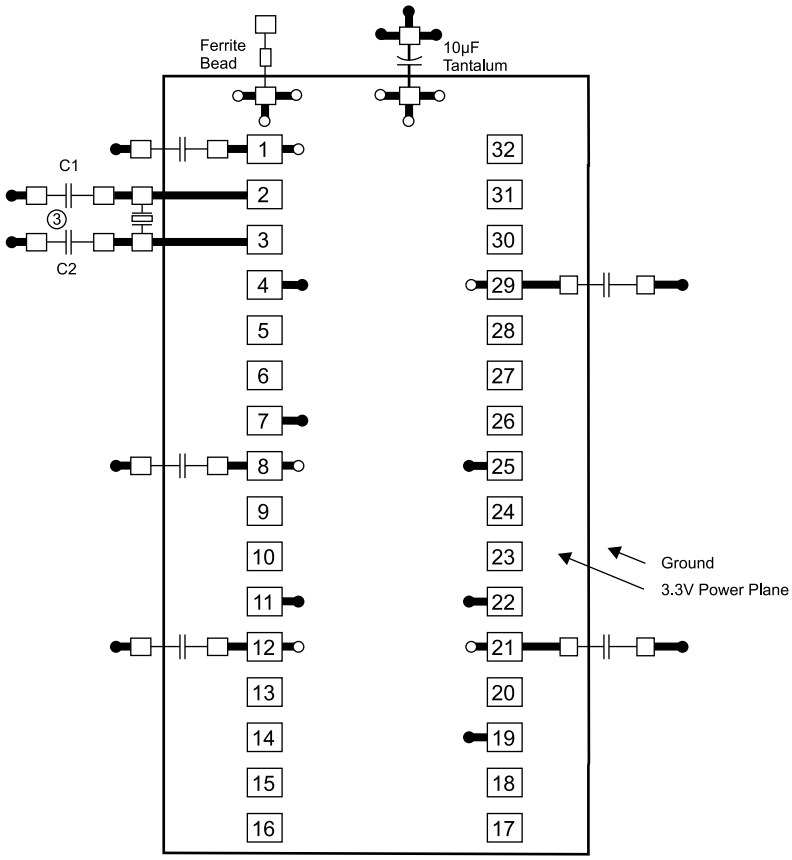
T_A = 0 - 70C; V_{DD} = 3.3 V +/-10%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -14 mA	2.4	2.9		V
Output Low Voltage	V_{OL1}	I_{OL} = 11 mA		0.3	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-43.0	23.0	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	20.0	31.0		mA
Rise Time	t_{r1}[1]	V_{OL} = 0.8 V, V_{OH} = 2.4 V		0.8	1.5	nS
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.8 V		0.9	1.5	nS
Duty Cycle	d_{t1}[1]	V_T = 1.4 V	45.0	51.0	55.0	%
Skew (window)	t_{sk1}[1]	V_T = 1.4 V	-250		250	pS
Jitter	t_{j1s1}[1]	V_T = 1.5 V; R_s= 33		88	150	pS
	t_{jabs1}[1]	V_T = 1.5 V; R_s= 33	-300		300	pS

[1]Guarenteed by design, not 100% tested in production.

General Layout Precautions:

1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
2) Make all power traces and vias as wide as possible to lower inductance.



● = Ground Plane Connection

○ = Power Plane Conncetion

□ = Solder Pads

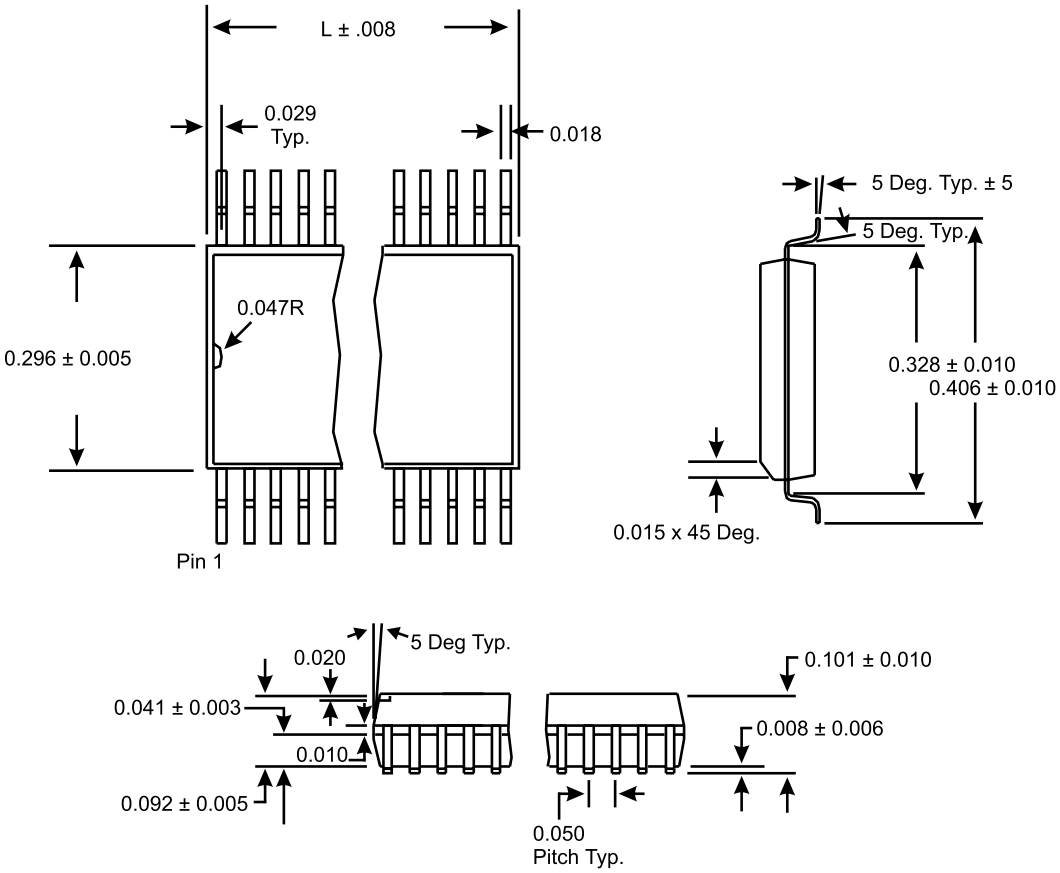
Notes:

1 All clock outputs should have series terminating resistor. Not shown in all places to improve readibility of diagram
2 Optional EMI capacitor should be used on all CPU, SDRAM, and PCI outputs.
3 Optional crystal load capacitors are recommended.

Capacitor Values:

C1, C2 : Crystal load values determined by user

All unmarked capacitors are 0.01µF ceramic



SOIC Package

LEAD COUNT	32L
DIMENSONL	.804

Ordering Information

ICS9169AM-70

Example:

ICS XXXX M - PPP

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  M=SOIC
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device