CY7C65213
CY7C65213A

USB-UART LP Bridge Controller

Features

- USB 2.0 certified, Full-Speed (12 Mbps)
  - Supports communication driver class (CDC), personal health care device class (PHDC), and vendor-device class
  - Battery charger detection (BCD) compliant with USB Battery Charging Specification Rev. 1.2 (peripheral detect only)
  - Integrated USB termination resistors
- Single-channel configurable UART interfaces
  - Supports 2-pin, 4-pin, 6-pin, 8-pin UART interface
  - Data rates up to 3 Mbps
  - 256 bytes for each transmit and receive buffer
  - Data format:
    - 7 or 8 data bits
    - 1 or 2 stop bits
    - No parity, even, odd, mark, or space parity
  - Supports parity, overrun, and framing errors
  - Supports flow control using CTS, RTS, DTR, DSR
  - Supports UART break signal
  - CY7C65213 supports single channel RS232/RS422 interfaces whereas CY7C65213A supports RS232/RS422/RS485 interfaces
- General-purpose input/output (GPIO): 8 pins
- Supports unique serial number feature for each device, which fixes the COM port number permanently when USB-UART LP Bridge controller device plugs in
- Configuration utility (Windows) to configure the following:
  - Vendor ID (VID), Product ID (PID), and Product and Manufacturer descriptors
  - UART
  - Charger detection
  - GPIO
- Driver support for VCOM and DLL
  - Windows 10: 32- and 64-bit versions
  - Windows 8.1: 32- and 64-bit versions
  - Windows 8: 32- and 64-bit versions
  - Windows 7: 32- and 64-bit versions
  - Windows Vista: 32- and 64-bit versions
  - Windows XP: 32- and 64-bit versions
  - Windows CE
  - Mac OS-X: 10.6, and later versions
  - Linux: Kernel version 2.6.35 and later versions
  - Android: Gingerbread and later versions
- 512-byte flash for storing configuration parameters
- Clocking: Integrated 48-MHz clock oscillator
- USB suspend mode for low power
- Supports bus-/self-powered configurations
- Compatible with USB 2.0 and USB 3.0 host controllers
- Operating voltage: 1.71 to 5.50 V
- Operating temperature:
  - Commercial: 0 °C to 70 °C
  - Industrial: –40 °C to 85 °C
- ESD protection: 2.2-kV HBM
- RoHS-compliant package
  - 28-pin SSOP (10 × 7.5 × 1.65 mm, 0.65-mm pitch)
  - 32-pin QFN (5 × 5 × 1 mm, 0.5-mm pitch)
- Ordering part number
  - CY7C65213-28PVXI
  - CY7C65213-32LTXI
  - CY7C65213A-28PVXI
  - CY7C65213A-32LTXI

Applications

- Blood glucose meter
- Battery-operated devices
- USB-to-UART cables
- Enables USB connectivity in legacy peripherals with UART
- Point-of-Sale (POS) terminals
- Industrial and T&M (Test and Measurement) devices

USB Compliant

The USB-UART LP Bridge controller (CY7C65213 and CY7C65213A) is fully compliant with the USB 2.0 specification, USB-IF Test-ID (TID) 40860041.

Table 1. CY7C65213 and CY7C65213-A Features Comparison

Features	CY7C65213	CY7C65213-A
RS-485 Support	No	Yes

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the document USB-Serial Bridge Controller Product Overview.

- Overview: USB Portfolio, USB Roadmap
- USB 2.0 Product Selectors: USB-Serial Bridge Controller, USB to UART Controller (Gen I)
- Knowledge Base Articles: Cypress offers a large number of USB knowledge base articles covering a broad range of topics, from basic to advanced level. Recommended knowledge base articles for getting started with USB-Serial Bridge Controller are:
  - KBA85909 – Key Features of the Cypress® USB-Serial Bridge Controller
  - KBA85921 – Replacing FT232R with CY7C65213 USB-UART LP Bridge Controller
  - KBA85920 – USB-UART and USB-Serial
  - KBA85913 – Voltage supply range for USB-Serial
  - KBA89355 – USB Serial Cypress Default VID and PID
  - KBA92641 – USB-Serial Bridge Controller Managing I/Os using API
  - KBA92442 – Non-Standard Baud Rates in USB-Serial Bridge Controllers
  - KBA91366 – Binding a USB-Serial Device to a Microsoft® CDC Driver
  - KBA92551 – Testing a USB-Serial Bridge Controller Configured as USB-UART with Linux®

For a complete list of knowledge base articles, click here.

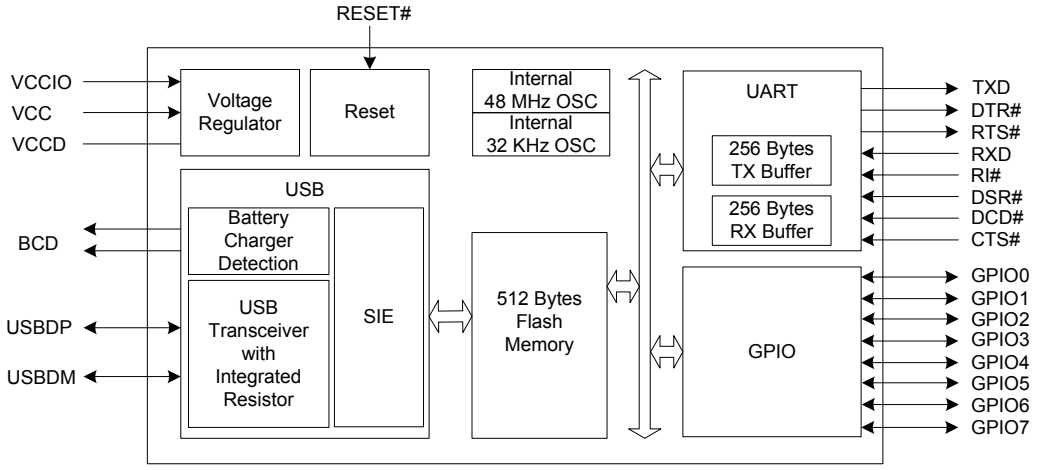
- Code Examples: USB Full-Speed
- Development Kits:
  - CYUSBS232, Cypress USB-UART LP Reference Design Kit
  - CYUSBS234, Cypress USB-Serial (Single Channel) Development Kit
  - CYUSBS236, Cypress USB-Serial (Dual Channel) Development Kit
- Models: IBIS

Cypress USB-UART LP Reference Design Kit

The Cypress USB-UART LP Reference Design Kit is a complete development resource. It provides a platform to develop and test custom projects. The development kit contains collateral materials for the firmware, hardware, and software aspects of a design.

Contents

Block Diagram – CY7C65213/CY7C65213A



Functional Overview

CY7C65213/CY7C65213A is a fully integrated USB-to-UART bridge that provides a simple method to upgrade UART-based devices to USB with a minimal number of components. CY7C65213/CY7C65213A includes a USB 2.0 Full-Speed controller, a UART transceiver, an internal regulator, an internal oscillator, and a 512-byte flash in a 32-pin QFN and 28-pin SSOP package.

The internal flash is used to store custom-specific USB descriptors and GPIO configuration. This is done in-system using a configuration utility that communicates over the USB interface.

Cypress provides royalty-free Virtual COM Port (VCP) device drivers. The drivers allow the device to appear as a COM port in PC applications. All UART signals, including handshaking and control signals, are implemented.

USB and Charger Detect

USB

CY7C65213/CY7C65213A has a built-in USB 2.0 Full-Speed transceiver. The transceiver incorporates an internal USB series termination resistor on the USB data lines and a 1.5-kΩ pull-up resistor on the USBDP.

Charger Detection

CY7C65213/CY7C65213A supports BCD for Peripheral Detect only and complies with the USB Battery Charging Specification, Rev. 1.2. It supports the following charging ports:

- Standard Downstream Port (SDP): Allows the system to draw up to 500-mA current from the host
- Charging Downstream Port (CDP): Allows the system to draw up to 1.5-A current from the host
- Dedicated Charging Port (DCP): Allows the system to draw up to 1.5-A of current from the wall charger

Serial Communication

CY7C65213/CY7C65213A has a serial communication block (SCB). Each SCB can implement UART interface. A 256-byte buffer is available in both the TX and RX lines.

UART Interface

The UART interface provides asynchronous serial communication with other UART devices operating at speeds of up to 3 Mbits/second. It supports 7 to 8 data bits, 1 to 2 stop bits, odd, even, mark, space, and no parity. The UART interface supports full-duplex communication with a signaling format compatible with the standard UART protocol. In CY7C65213, UART pins may be interfaced to industry standard RS232/RS422 transceivers whereas in CY7C65213A these UART pins may be interfaced to RS232/RS422/RS485 transceivers.

Common UART functions, such as parity error and frame error, are supported. A 256-byte buffer is available in both TX and RX directions. CY7C65213/CY7C65213A supports baud rates ranging from 300 baud to 3 Mbaud. UART baud rates can be set using the configuration utility.

Notes:

Parity error gets detected when UART transmitter device is configured for odd parity and UART receiver device is configured for even parity.

Frame error gets detected when UART transmitter device is configured for 7 bits data width and 1 stop bit, whereas UART receiver device is configured for 8 bit data width and 2 stop bits.

UART Flow Control

The CY7C65213/CY7C65213A device supports UART hardware flow control using control signal pairs, such as RTS# (Request to Send) / CTS# (Clear to Send) and DTR# (Data Terminal Ready) / DSR# (Data Set Ready).

The following sections describe the flow control signals:

- CTS# (Input) / RTS# (Output)

CTS# can pause or resume data transmission over the UART interface. Data transmission can be paused by de-asserting the CTS signal and resumed by using CTS# assertion. The pause and resume operation does not affect data integrity. With flow control enabled, receive buffer has a watermark level of 93%. After the data in the receive buffer reaches that level, the RTS# signal is de-asserted, instructing the transmitting device to stop data transmission. The start of data consumption by the

application reduces device data backlog. After it reaches the 75% watermark level, the RTS# signal is asserted to resume data reception.

- DSR# (Input) / DTR# (Output)

The DSR#/DTR# signals are used to establish a communication link with the UART. These signals complement each other in their functionality, similar to CTS# and RTS#.

GPIO Interface

CY7C65213/CY7C65213A has eight GPIOs. The configuration utility lets you configure the GPIO pins. The configurable options are as follows:

- TRISTATE: GPIO tristated
- DRIVE 1: Output static 1
- DRIVE 0: Output static 0
- POWER#: Power control for bus power designs
- TXLED#: Drives LED during USB transmit
- RXLED#: Drives LED during USB receive
- TX or RX LED#: Drives LED during USB transmit or receive. GPIO can be configured to drive LED at 8-mA drive strength.
- SLEEP#: Indicates USB suspend
- BCD0/1: Two-pin output to indicate the type of USB charger
- BUSDETECT: Connects VBUS pin for USB host detection

Memory

CY7C65213/CY7C65213A has a 512-byte flash. Flash is used to store USB parameters, such as VID/PID, serial number, and Product and Manufacturer Descriptors, which can be programmed by the configuration utility.

System Resources

Power System

CY7C65213/CY7C65213A supports the USB Suspend mode to control power usage. CY7C65213/CY7C65213A operates in bus-powered or self-powered modes over a range of 3.15 V to 5.5 V.

Clock System

CY7C65213/CY7C65213A has a fully integrated clock and does not require any external crystal. The clock system is responsible for providing clocks to all subsystems.

Internal 48-MHz Oscillator

The internal 48-MHz oscillator is the primary source of internal clocking in the CY7C65213/CY7C65213A device.

Internal 32-kHz Oscillator

The internal 32-kHz oscillator is the primary source of internal clocking in CY7C65213/CY7C65213A.

Reset

The reset block ensures reliable power-on reset and brings the device back to the default known state. The RESET# (active low) pin can be used by external devices to reset the CY7C65213/CY7C65213A.

Suspend and Resume

The CY7C65213/CY7C65213A device asserts the SLEEP# pin when the USB bus goes into the suspend state. This helps to meet the stringent suspend current requirements of the USB 2.0 specification, while using the device in bus-powered mode. The device resumes from the suspend state under either of the following two conditions:

1. Any activity is detected on the USB bus
2. The RI# (configured as wakeup) pin is asserted to generate remote wakeup to the host.

WAKEUP

The RI# (configured as wakeup) pin is used to generate the remote wakeup signal on the USB bus. The remote wakeup signal is sent only if the host enables this feature through the SET_FEATURE request. The device communicates support for the remote wakeup to the host through the configuration descriptor during the USB enumeration process. The CY7C65213 device allows enabling/disabling of the remote wakeup feature through the configuration utility.

Software

Cypress delivers a complete set of software drivers and a configuration utility to enable product configuration during system development.

Drivers for Linux Operating Systems

Cypress provides a User Mode USB driver library (*libcyusbserial.so*) that abstracts vendor commands for the UART interface and provides a simplified API interface for user applications. This library uses the standard open-source libUSB library to enable USB communication. The Cypress serial library supports the USB plug-and-play feature using the Linux ‘udev’ mechanism.

CY7C65213/CY7C65213A supports the standard USB CDC UART-class driver, which is bundled with the Linux kernel.

Android Support

The CY7C65213/CY7C65213A solution also includes an Android Java class–CyUsbSerial.java–which exposes a set of interface functions to communicate with the device.

Drivers for Mac OSx

Cypress delivers a dynamically linked shared library (*CyUSBSerial.dylib*) based on libUSB, which enables communication to the CY7C65213/CY7C65213A device.

In addition, the device also supports the native Mac OSx CDC UART-class driver.

Drivers for Windows Operating Systems

For Windows operating systems (XP, Vista, Win7, Win8 and Win8.1), Cypress delivers a User Mode dynamically linked library–CyUSBSerial DLL.This library abstracts the vendor-specific interface of the CY7C65213/CY7C65213A devices and provides convenient APIs to the user. It provides interface APIs for vendor-specific UART and class-specific APIs for PHDC.

USB-UART LP Bridge Controller works with the Windows-standard USB CDC UART class driver. A virtual COM port driver–CyUSBSerial.sys–is also delivered, which implements the USB CDC class driver. The Cypress Windows drivers are Windows hardware certification kit-compliant.

These drivers are bound to device through WU (Windows Update) services.

Cypress drivers also support Windows plug-and-play and power management and USB Remote Wake-up.

Windows-CE support

The CY7C65213/CY7C65213A solution includes a CDC UART driver library for Windows-CE platforms.

Device Configuration Utility (Windows only)

A Windows-based configuration utility is available to configure device initialization parameters. This graphical user application provides an interactive interface to define boot parameters stored in the device flash.

This utility allows the user to save a user-selected configuration to text or xml formats. It also allows users to load a selected configurations from text or xml formats. The configuration utility allows the following operations:

- View current device configuration
- Select and configure UART, battery charging, and GPIOs
- Configure USB VID, PID, and string descriptors
- Save or Load configuration

You can download the free configuration utility and drivers at www.cypress.com/go/usbserial.

Internal Flash Configuration

The internal flash memory can be used to store configuration parameters as shown in the following table. A free configuration utility is provided to configure the parameters listed in the table to meet application-specific requirements over a USB interface. The configuration utility can be downloaded at www.cypress.com/go/usbserial.

Table 2. Internal Flash Configuration for both CY7C65213 and CY7C65213A

Parameter	Default Value	Description
USB Configuration		
USB Vendor ID (VID)	0x04B4	Default Cypress VID. Can be configured to customer VID
USB Product ID (PID)	0x0003	Default Cypress PID. Can be configured to customer PID
Manufacturer string	Cypress	Can be configured with any string up to 64 characters
Product string	USB-UART LP	Can be configured with any string up to 64 characters
Serial string		Can be configured with any string up to 64 characters
Power mode	Bus powered	Can be configured to bus-powered or self-powered mode
Max current draw	100 mA	Can be configured to any value from 0 to 500 mA. The configuration descriptor will be updated based on this.
Remote wakeup	Enabled	Can be disabled. Remote wakeup is initiated by driving #RI low
USB interface protocol	CDC	Can be configured to function in CDC, PHDC, or Cypress vendor class
VCC voltage is 3.3 V	Disabled	This option should be checked if we need to bypass USB regulator in CY7C65213/CY7C65213A.
VCCIO voltage is less than 2 V	Disabled	This option should be checked if we need to bypass VCCIO regulator in CY7C65213/CY7C65213A.
Enable manufacturing interface	Enabled	This option enables an additional vendor class manufacturing mode interface to reconfigure the CY7C65213/CY7C65213A.
I/O Level	CMOS	Can be configured to either CMOS or LVTTL.
I/O Mode	Fast	Can be configured to either fast or slow for EMI considerations.
Baud Rate	115200	Can be configured in an editable drop-down combo box that lists the predefined, standard baud rates. You can also enter a specific baud rate in the combo box.
Type	8 pin	This option is nor re-configurable. Pre-configured to 8 pin type.
Data Width	8 bits	Can be configured to either 7 bits or 8 bits.
Stop Bits	1 bit	Can be configured to either 1 bit or 2 bits.
Parity	None	Can be configured to either None, Odd, Even, Mark, or Space.
Invert RTS	Disabled	By selecting this option in USB Serial Configuration Utility, the polarity of the RTS line can be inverted.
Invert CTS	Disabled	By selecting this option in USB Serial Configuration Utility, the polarity of the CTS line can be inverted.
Invert DTR	Disabled	By selecting this option in USB Serial Configuration Utility, the polarity of the DTR line can be inverted.
Invert DSR	Disabled	By selecting this option in USB Serial Configuration Utility, the polarity of the DSR line can be inverted.
Invert DCD	Disabled	By selecting this option in USB Serial Configuration Utility, the polarity of the DCD line can be inverted.
Invert RI	Disabled	By selecting this option in USB Serial Configuration Utility, the polarity of the RI line can be inverted.
Drop packets on RX error	Disabled	This parameter defines the behavior of the UART when an error is detected in the packet received (RX packet/byte). When this option is selected in USB Serial Configuration Utility, the data packet/byte in the RX buffer is discarded.

Table 2. Internal Flash Configuration for both CY7C65213 and CY7C65213A *(continued)*

Parameter	Default Value	Description
Disable CTS and DSR pull-up during suspend	Enabled	In an embedded system, this parameter can be selected in USB Serial Configuration Utility to reduce system current consumption during Suspend state. This parameter disables the CTS and DSR pull-up resistors in the Suspend state to meet USB 2.0 Specification current requirements.
BCD	Disabled	Charger detect is disabled by default. When BCD is enabled, three of the GPIOs must be configured for BCD.
GPIO Configuration		
GPIO0	TXLED#	GPIO can be configured as shown in Table 13 on page 14.
GPIO1	RXLED#	
GPIO2	TRISTATE	
GPIO3	POWER#	
GPIO4	SLEEP#	
GPIO5	BUSDETECT	
GPIO6	BCD0	
GPIO7	BCD1	

Electrical Specifications

Absolute Maximum Ratings

Exceeding maximum ratings [1] may shorten the useful life of the device.

Storage temperature ..... –55 °C to +100 °C

Ambient temperature with power supplied (Industrial) ..... –40 °C to +85 °C

Supply voltage to ground potential
V_{CCIO} ..... 6.0 V
V_{CC} ..... 6.0 V
V_{CCD} ..... 1.95 V
V_{GPIO} ..... V_{CCIO} + 0.5 V

Static discharge voltage ESD protection levels:

■ 2.2-kV HBM per JESD22-A114

Latch-up current ..... 140 mA

Maximum current per GPIO ..... 25 mA

Operating Conditions

T_A (ambient temperature under bias)
Industrial ..... –40 °C to +85 °C

V_{CC} supply voltage ..... 3.15 V to 5.25 V

V_{CCIO} supply voltage ..... 1.71 V to 5.50 V

V_{CCD} supply voltage ..... 1.71 V to 1.89 V

Device-Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 85 °C, T_J ≤ 100 °C, and 1.71 V to 5.50 V, except where noted.

Table 3. DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{CC}	V_{CC} supply voltage	3.15	3.30	3.45	V	Set and configure correct voltage range using the configuration utility for V_{CC}.
		4.35	5.00	5.25	V	
V_{CCIO}	V_{CCIO} supply voltage	1.71	1.80	1.89	V	Used to set I/O voltage. Set and configure the correct voltage range using the configuration utility for V_{CCIO}.
		2.0	3.3	5.5	V	
V_{CCD}	Output voltage (for core logic)	–	1.80	–	V	Do not use this supply to drive the external device. • 1.71 V ≤ VCCIO ≤ 1.89 V: Short V_{CCD} pin with the V_{CCIO} pin • V_{CCIO} > 2 V – connect a 1-µF capacitor (Cefc) between the V_{CCD} pin and ground
Cefc	External Regulator voltage bypass	1.00	1.30	1.60	µF	X5R ceramic or better
I_{CC1}	Operating supply current	–	13	18	mA	USB 2.0 FS, UART at 1-Mbps single channel, no GPIO switching at V_{CC} = 5 V, V_{CCIO} = 5 V
I_{CC2}	USB Suspend supply current	–	5	–	µA	Does not include current through the pull-up resistor on USBDP In USB suspend mode, the D+ voltage can go up to a maximum of 3.8 V.

Table 4. AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Z_{OUT}	USB driver output impedance	28	–	44	Ω	As CY7C65213 has internal termination resistors, external resistors are not required.
Twakeup	Wakeup from USB Suspend mode	–	25	–	µs	

Note
1. Usage above the absolute maximum conditions may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

GPIO

Table 5. GPIO DC Specification

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{IH}[2]	Input voltage high threshold	0.7 × V_{CCIO}	–	–	V	CMOS Input
V_{IL}	Input voltage low threshold	–	–	0.3 × V_{CCIO}	V	CMOS Input
V_{IH}[2]	LVTTL input, V_{CCIO}< 2.7 V	0.7 × V_{CCIO}	–	–	V	
V_{IL}	LVTTL input, V_{CCIO} < 2.7 V	–	–	0.3 × V_{CCIO}	V	
V_{IH}[2]	LVTTL input, V_{CCIO} ≥ 2.7 V	2	–	–	V	
V_{IL}	LVTTL input, V_{CCIO} ≥ 2.7 V	–	–	0.8	V	
V_{OH}	CMOS output voltage high level	V_{CCIO} – 0.4	–	–	V	I_{OH} = 4 mA, V_{CCIO} = 5 V +/- 10%
V_{OH}	CMOS output voltage high level	V_{CCIO} – 0.6	–	–	V	I_{OH} = 4 mA, V_{CCIO} = 3.3 V +/- 10%
V_{OH}	CMOS output voltage high level	V_{CCIO} – 0.5	–	–	V	I_{OH} = 1 mA, V_{CCIO} = 1.8 V +/- 5%
V_{OL}	CMOS output voltage low level	–	–	0.4	V	I_{OL} = 8 mA, V_{CCIO} = 5 V +/- 10%
V_{OL}	CMOS output voltage low level	–	–	0.6	V	I_{OL} = 8 mA, V_{CCIO} = 3.3 V +/- 10%
V_{OL}	CMOS output voltage low level	–	–	0.6	V	I_{OL} = 4 mA, V_{CCIO} = 1.8 V +/- 5%
Rpullup	Pull-up resistor	3.5	5.6	8.5	kΩ	
Rpulldown	Pull-down resistor	3.5	5.6	8.5	kΩ	
I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{CCIO} = 3.0 V
C_{IN}	Input Capacitance	–	–	7	pF	
Vhysttl	Input hysteresis LVTTL; V_{CCIO} > 2.7 V	25	40	–	mV	
Vhyscmos	Input hysteresis CMOS	0.05 × V_{CCIO}	–	–	mV	

Table 6. GPIO AC Specification

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{RiseFast1}$	Rise Time in Fast mode	2	–	12	ns	V_{CCIO} = 3.3 V/ 5.5 V, Cload = 25 pF
$T_{FallFast1}$	Fall Time in Fast mode	2	–	12	ns	V_{CCIO} = 3.3 V/ 5.5 V, Cload = 25 pF
$T_{RiseSlow1}$	Rise Time in Slow mode	10	–	60	ns	V_{CCIO} = 3.3 V/ 5.5 V, Cload = 25 pF
$T_{FallSlow1}$	Fall Time in Slow mode	10	–	60	ns	V_{CCIO} = 3.3 V/ 5.5 V, Cload = 25 pF
$T_{RiseFast2}$	Rise Time in Fast mode	2	–	20	ns	V_{CCIO} = 1.8 V, Cload = 25 pF
$T_{FallFast2}$	Fall Time in Fast mode	20	–	100	ns	V_{CCIO} = 1.8 V, Cload = 25 pF
$T_{RiseSlow2}$	Rise Time in Slow mode	2	–	20	ns	V_{CCIO} = 1.8 V, Cload = 25 pF
$T_{FallSlow2}$	Fall Time in Slow mode	20	–	100	ns	V_{CCIO} = 1.8 V, Cload = 25 pF

Note
2. V_{IH} must not exceed V_{CCIO} + 0.2 V.

Reset

Table 7. Reset DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{IH}	Input voltage high threshold	0.7 × V_{CCIO}	–	–	V	
V_{IL}	Input voltage low threshold	–	–	0.3 × V_{CCIO}	V	
Rpullup	Pull-up resistor	3.5	5.6	8.5	kΩ	
C_{IN}	Input capacitance	–	5	–	pF	
Vhysxres	Input voltage hysteresis	–	100	–	mV	

Table 8. Reset AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Tresetwidth	Reset pulse width	1	–	–	µs	

UART

Table 9. UART AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{UART}	UART bit rate	0.3	–	3,000	kbps	

Flash Memory

Table 10. Flash Memory Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Fend	Flash endurance	100K	–	–	cycles	
Fret	Flash retention. $T_A \leq 85$ °C, 10 K program/erase cycles	10	–	–	years	

Pin Description

Table 11. CY7C65213-28PVXI / CY7C65213A-28PVXI (28-pin SSOP) Pin Description

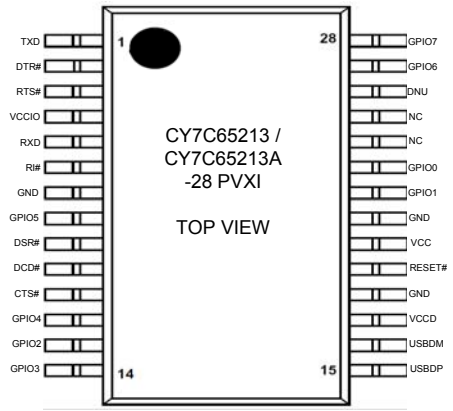
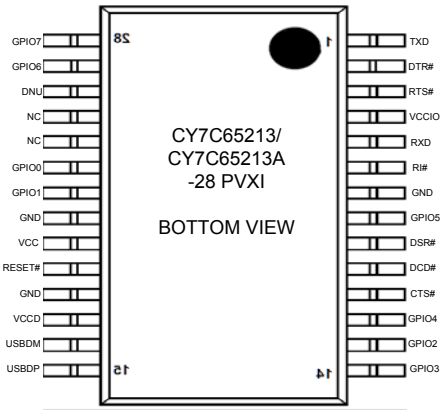
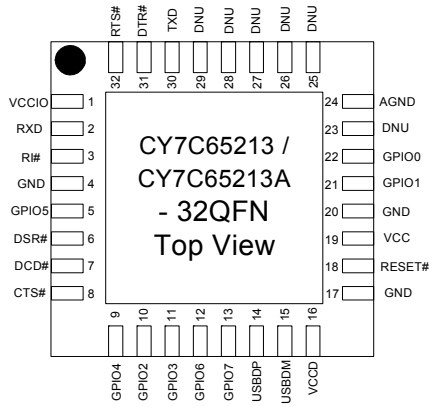
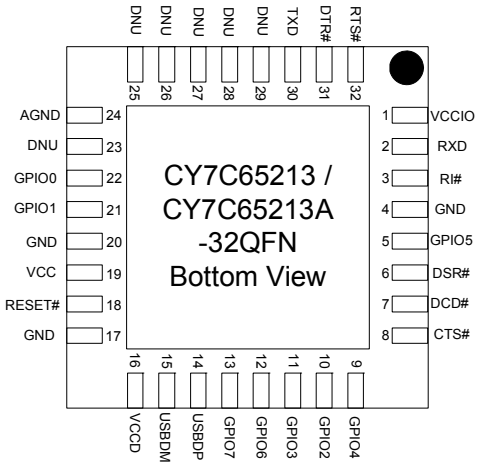
Pin	Name	Type	Default	Description	
1	TXD	Output	–	Transmit asynchronous data output	
2	DTR#	Output	–	Data terminal ready control output	
3	RTS#	Output	–	Request to send control output	
4	VCCIO	Power	–	Supply to the device core and Interface, 1.71 to 5.5 V	
5	RXD	Input	–	Receiving asynchronous data input	
6	RI#	Input	–	Ring indicator control input. Can be configured as wake-up; low signal on this pin is used to wake up the USB Host controller out of the suspend State	
7	GND	Power	–	Digital Ground	
8	GPIO5	I/O	Tristate	Configurable GPIO	
9	DSR#	Input	–	Data set ready control input	
10	DCD#	Input	–	Data carrier detect control input	
11	CTS#	Input	–	Clear to send control input	
12	GPIO4	I/O	Sleep#	Configurable GPIO	
13	GPIO2	I/O	Tristate	Configurable GPIO	
14	GPIO3	I/O	Power#	Configurable GPIO	
15	USBDP	USBIO	–	USB Data Signal Plus, integrating termination resistor and a 1.5-kΩ pull-up resistor	
16	USBDM	USBIO	–	USB Data Signal Minus, integrating termination resistor	
17	VCCD	Power	–	This pin is an output of an internal regulator and cannot drive external devices. Decouple this pin to ground using 1 µF capacitor when the VCCIO voltage is greater then 2 V. Connect this pin to VCCIO supply when the VCCIO voltage is less then 2 V.	
18	GND	Power	–	Digital Ground	
19	RESET#	XRES	–	Chip reset, active low. Can be left unconnected or have a pull-up resistor connected to VCCIO supply.	
20	VCC	Power	–	VBUS Supply voltage (USB) 3.15 to 5.25 V	
21	GND	Power	–	Digital Ground	
22	GPIO1	I/O	RXLED#	Configurable GPIO	
23	GPIO0	I/O	TXLED#	Configurable GPIO	
24	NC	–	–	No Connect	
25	NC	–	–	No Connect	
26	DNU	–	–	Do Not Use	
27	GPIO6	I/O	Tristate	Configurable GPIO	
28	GPIO7	I/O	Tristate	Configurable GPIO	

Table 12. CY7C65213-32LTXI / CY7C65213A-32LTXI (32-pin QFN) Pin Description [3, 4]

Pin	Name	Type	Default	Description	
1	VCCIO	Power	–	Supply to the device core and Interface, 1.71 to 5.5 V	
2	RXD	Input	–	Receiving asynchronous data input	
3	RI#	Input	–	Ring indicator control input. Can be configured as wake-up; low signal on this pin is used to wake up the USB Host controller out of the suspend state	
4	GND	Power	–	Digital Ground	
5	GPIO5	I/O	TRISTATE	Configurable GPIO. See Table 13.	
6	DSR#	Input	–	Data set ready control input	
7	DCD#	Input	–	Data carrier detect control input	
8	CTS#	Input	–	Clear to send control input	
9	GPIO4	I/O	SLEEP#	Configurable GPIO. See Table 13.	
10	GPIO2	I/O	TRISTATE	Configurable GPIO. See Table 13.	
11	GPIO3	I/O	POWER#	Configurable GPIO. See Table 13.	
12	GPIO6	I/O	TRISTATE	Configurable GPIO. See Table 13.	
13	GPIO7	I/O	TRISTATE	Configurable GPIO. See Table 13.	
14	USBDP	USBIO	–	USB Data Signal Plus, integrating termination resistor and a 1.5-kΩ pull-up resistor	
15	USBDM	USBIO	–	USB Data Signal Minus, integrating termination resistor	
16	VCCD	Power	–	This pin is an output of an internal regulator and cannot drive external devices. Decouple this pin to ground using 1 µF capacitor when the VCCIO voltage is greater then 2 V. Connect this pin to VCCIO supply when the VCCIO voltage is less then 2 V.	
17	GND	Power	–	Digital Ground	
18	RESET#	XRES	–	Chip reset, active low. Can be left unconnected or have a pull-up resistor connected to VCCIO supply.	
19	VCC	Power	–	Supply voltage (USB) 3.15 to 5.25 V	
20	GND	Power	–	Digital Ground	
21	GPIO1	I/O	RXLED#	Configurable GPIO. See Table 13.	
22	GPIO0	I/O	TXLED#	Configurable GPIO. See Table 13.	
23	DNU	–	–	Do Not Use	
24	AGND	Power	–	Analog Ground	

Notes
3. All active low signals for the signal name are indicated by a # in this document.
4. Any pin acting as an Input pin should not be left unconnected.

Table 12. CY7C65213-32LTXI / CY7C65213A-32LTXI (32-pin QFN) Pin Description *(continued)* [3, 4]

Pin	Name	Type	Default	Description	
25	DNU	–	–	Do Not Use	
26	DNU	–	–	Do Not Use	
27	DNU	–	–	Do Not Use	
28	DNU	–	–	Do Not Use	
29	DNU	–	–	Do Not Use	
30	TXD	Output	–	Transmit asynchronous data output	
31	DTR#	Output	–	Data terminal ready control output	
32	RTS#	Output	–	Request to send control output	

Table 13. GPIO Configuration

The following signal options can be configured on the GPIO pins using a Cypress-provided configuration utility, which you can download at www.cypress.com

GPIO Configuration Option	Description
TRISTATE	I/O tristated[5]
DRIVE 1	Output static 1
DRIVE 0	Output static 0
POWER#	This output is used to control power to an external logic through a switch to cut off power prior to USB configuration and during USB suspend. 0 - USB device in Configured state 1 - USB device in Unconfigured state or during USB suspend mode
TXLED#	Drives LED during USB transmit
RXLED#	Drives LED during USB receive
TX and RX LED#	Drives LED during USB transmit and receive
SLEEP#	When low indicates USB suspend
BCD0	Configurable battery charger detect pins to indicate the type of USB charger (SDP, CDP, or DCP) Configuration example: 00 - Draw up to 100 mA (Unconfigured state) 01 - SDP (up to 500 mA) 10 - CDP/DCP (up to 1.5 A) 11 - Suspend (up to 2.5 mA) This truth table can be configured using a configuration utility
BCD1	
BUSDETECT	VBUS detection. Connect VBUS to this pin for VBUS detection when using the BCD feature[6].

Notes
5. Any GPIO, configured as “Input” should either be pulled high or low. A floating input pin (Tristate) has an indeterminate voltage level that can cause excess internal current consumption. A 10 kΩ pull-up or pull-down resistor is recommended on each of the input pin.
6. When VBUS = VCCIO, connect VBUS to BUSDETECTION with a 10-K series resistor
When VBUS > VCCIO, connect VBUS to BUSDETECTION via the resistor divider network. Select R1 and R2 values as follows:
R1 ≥ 10 k
R2 / (R1 + R2) = VCCIO/VBUS

USB Power Configuration

The following section describes possible USB power configurations for the CY7C65213/CY7C65213A. Refer to the Pin Description on page 12 for signal details.

USB Bus-Powered Configuration

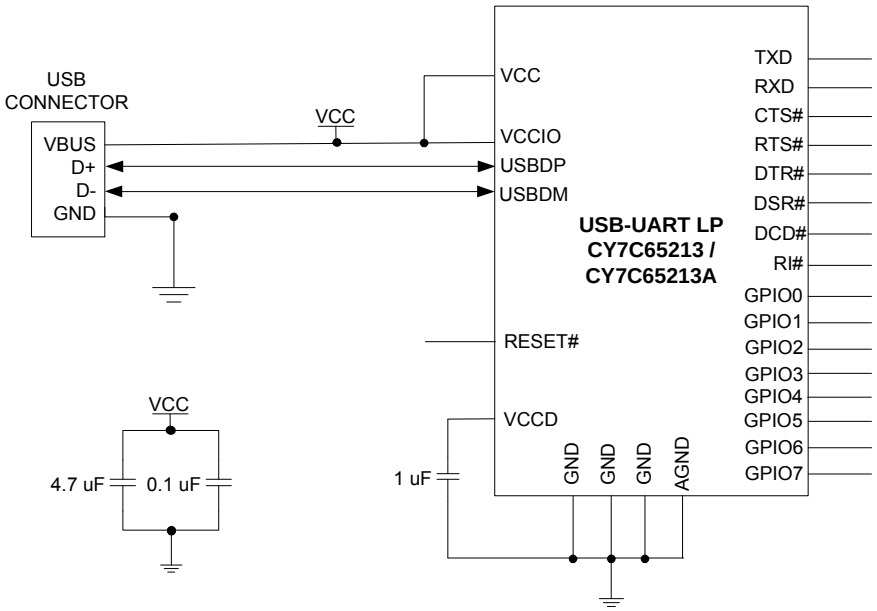
Figure 1 shows an example of the CY7C65213/CY7C65213A in a bus-powered design. VBUS is connected directly to the CY7C65213/CY7C65213A because it has an internal regulator.

The USB bus-powered system must comply with the following requirements:

1. The system should not draw more than 100 mA prior to USB enumeration (unconfigured state).
2. The system should not draw more than 2.5 mA during USB Suspend mode.
3. A high-power bus-powered system (can draw more than 100 mA when operational) must use POWER# (configured over GPIO) to keep the current consumption below 100 mA prior to USB enumeration and 2.5 mA during USB Suspend state.
4. The system should not draw more than 500 mA from the USB host.

The configuration descriptor in the CY7C65213 flash should be updated to indicate bus power and the maximum current required by the system using a configuration utility.

Figure 1. Bus-Powered Configuration



Self-Powered Configuration

Figure 2 shows an example of CY7C65213/CY7C65213A in a self-powered design.

In this configuration:

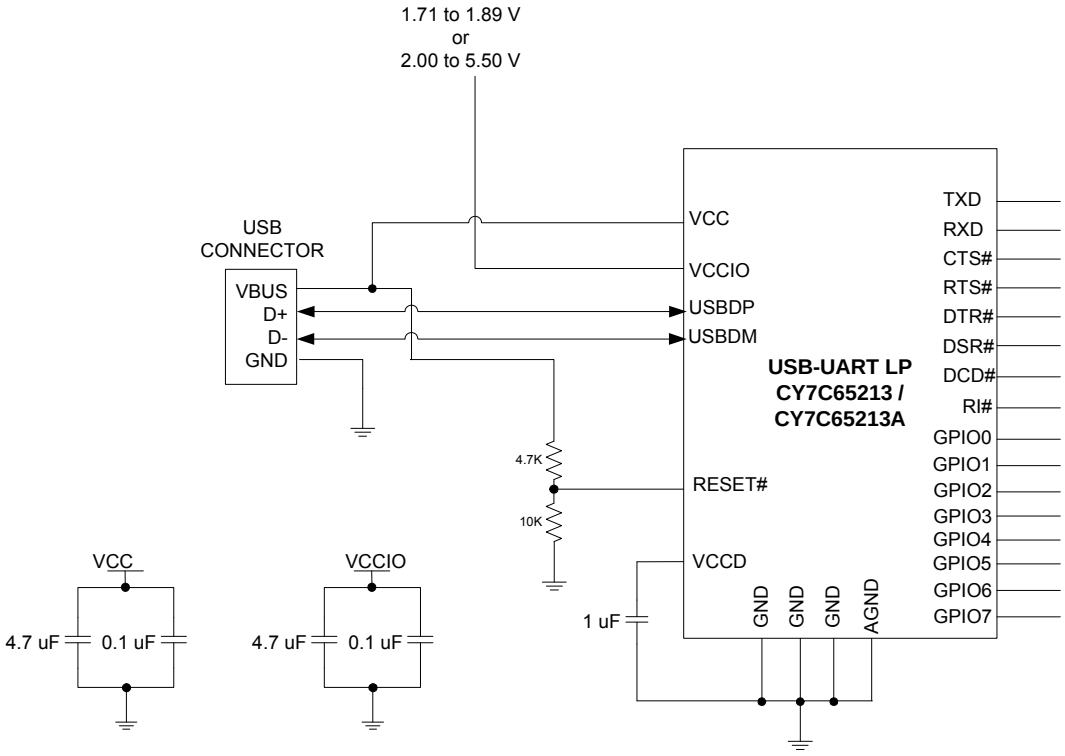
- VCC is powered from USB VBUS. VCC pin is also used to detect USB connection.
- VCCIO is powered from an external power supply.

The VBUS of the USB host is used to control the RESET# pin of CY7C65213/CY7C65213A. When the VBUS is present, reset to CY7C65213/CY7C65213A is de-asserted and the device enables an internal, 1.5-kΩ pull-up resistor on USBDP. When the VBUS is absent (the USB host is powered down), reset to CY7C65213/CY7C65213A is asserted, which causes the device to remove the 1.5-kΩ pull-up resistor on USBDP. This ensures that no current flows from the USBDP to the USB host through a 1.5-kΩ pull-up resistor, to comply with USB 2.0 specification.

When reset is asserted to CY7C65213/CY7C65213A, all the I/O pins are tristated.

Using the configuration utility, the configuration descriptor in the CY7C65213/CY7C65213A flash should be updated to indicate that it is self-powered.

Figure 2. Self-Powered Configuration



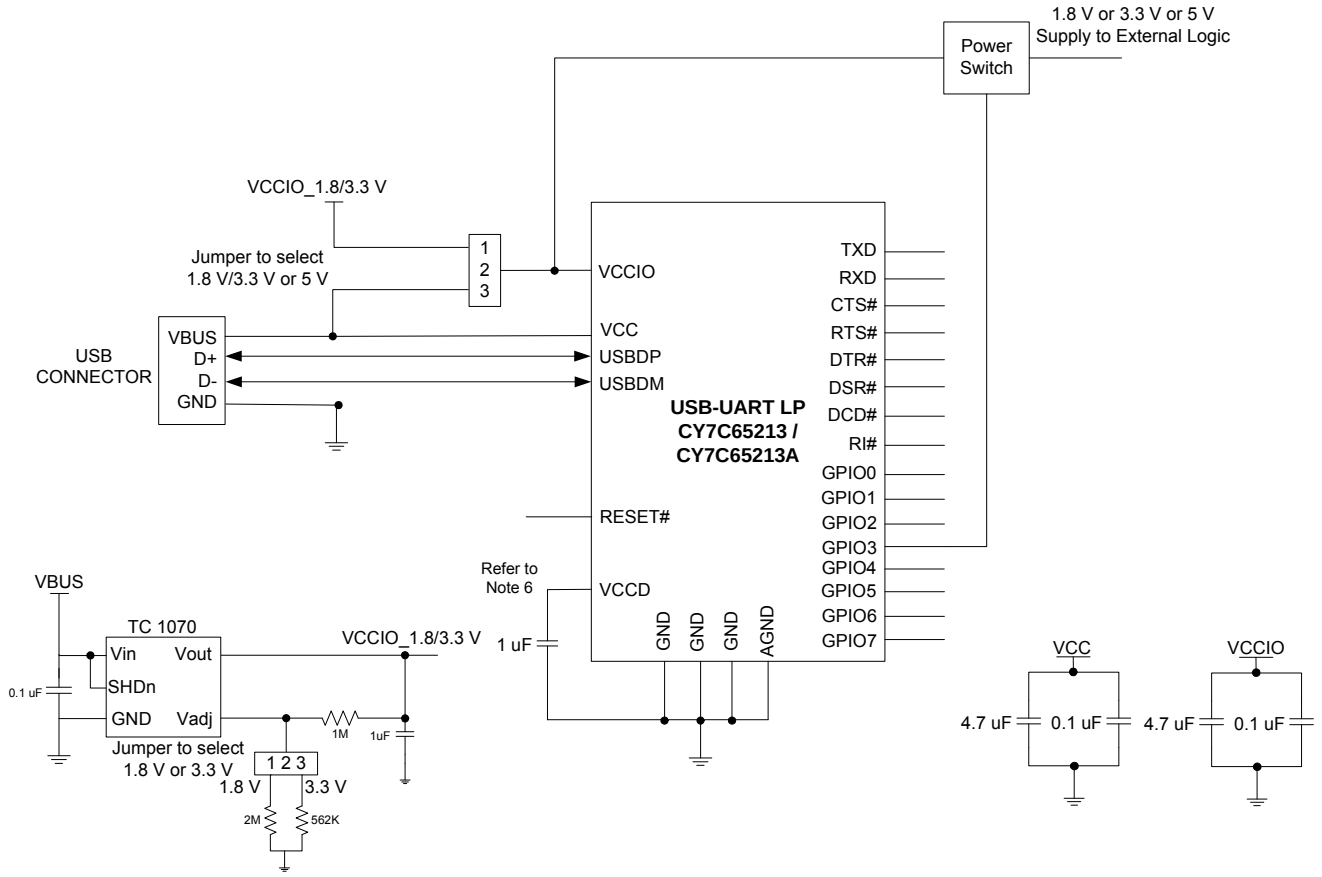
USB Bus Powered with Variable I/O Voltage

Figure 3 shows the CY7C65213/CY7C65213A in a bus-powered system with variable I/O voltage. A low dropout (LDO) regulator is used to supply 1.8 V or 3.3 V (using a jumper switch) the input of which is 5 V from the VBUS. Another jumper switch is used to select VCCIO_1.8/3.3 V or 5 V from the VBUS for the VCCIO pin of CY7C65213/CY7C65213A. This allows I/O voltage and supply to external logic to be selected among 1.8 V, 3.3 V, or 5 V.

The USB bus-powered system must comply with the following:

1. The system should not draw more than 100 mA prior to USB enumeration (Unconfigured state).
2. The system should not draw more than 2.5 mA during USB Suspend mode.
3. A hjgh-power bus-powered system (can draw more than 100 mA when operational) must use POWER# (configured over GPIO) to keep the current consumption below 100 mA prior to USB enumeration and 2.5 mA during USB Suspend state.

Figure 3. USB Bus-Powered with 1.8-V, 3.3-V, or 5-V Variable I/O Voltage [7]



Note

7. 1.71 V ≤ V_{CCIO} ≤ 1.89 V - Short V_{CCD} pin with V_{CCIO} pin; V_{CCIO} > 2 V - connect a 1-uF decoupling capacitor to the V_{CCD} pin.

Application Examples

The following section provides the CY7C65213/CY7C65213A application examples.

USB to RS232 Converter

CY7C65213/CY7C65213A can connect any embedded system, with a serial port, to a host PC through USB. CY7C65213/CY7C65213A enumerates as a COM port on the host PC.

The RS232 protocol follows bipolar signaling, that is, the output signal toggles between negative and positive polarity. The valid RS232 signal is either in the –3-V to –15-V range or in the +3-V to +15-V range, and the range between –3 V to +3 V is invalid. In RS232, Logic 1 is called “Mark” and corresponds to a negative voltage range. Logic 0 is called “Space” and corresponds to a positive voltage range. The RS232 level converter facilitates this polarity inversion and the voltage-level translation between the CY7C65213/CY7C65213A’s UART interface and RS232 signaling.

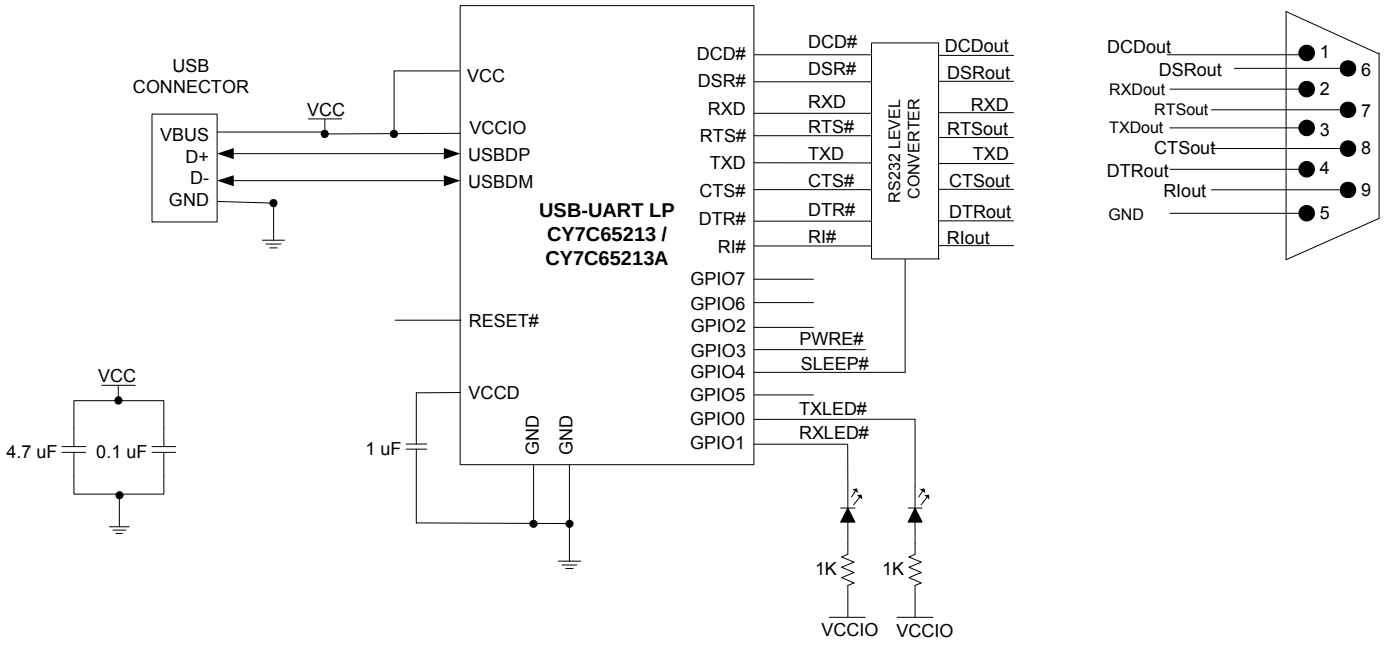
In this application, as shown in Figure 4, GPIO4 can be configured as SLEEP# or POWER# and connected to the SHDN# pin of the RS232-level converter. Default configuration of the GPIO4 in the device is SLEEP#. If GPIO4 is configured as SLEEP#, a low on this pin indicates USB suspend; if GPIO4 is configured as POWER#, a high on this pin indicates a state prior to USB configuration or USB suspend. GPIO0 and GPIO1 are configured as TXLED# and RXLED# to drive two LEDs, indicating data transmit and receive, respectively.

CY7C65213/CY7C65213A has been tested with Maxim’s MAX3245 transceiver.

A simple loop-back test can be performed on the USB-to-RS232 converter as follows: Connect the TX and RX lines of the RS232 interface with a jumper, transmit data to the converter through a COM Port communication terminal (such as Hyper Terminal or Tera Term), and verify if the same data is received.

For detailed steps to test a USB-to-RS232 solution, refer to the section ‘Testing a USB to RS232 solution’ in the application note AN85514.

Figure 4. USB to RS232 Converter



USB to RS485 Application

CY7C65213A can be configured as USB to UART interface. This UART interface operates at TTL level and it can be converted to RS485 interface using a GPIO and any half duplex RS485 transceiver IC (to convert TTL level to RS485 level) as shown in following figure1. This GPIO (TXDEN) enables and disables the transmission of data through RS485 transceiver IC based on availability of character in UART buffer of CY7C65213A. This GPIO can be configured using USB-Serial Configuration utility. Figure 6 shows timing diagram of this GPIO.

RS485 is a multi-drop network – that is, many devices can communicate with each other over a single two wire cable connection. The RS485 cable requires to be terminated at each end of the cable.

Figure 5. USB to RS485 Bridge

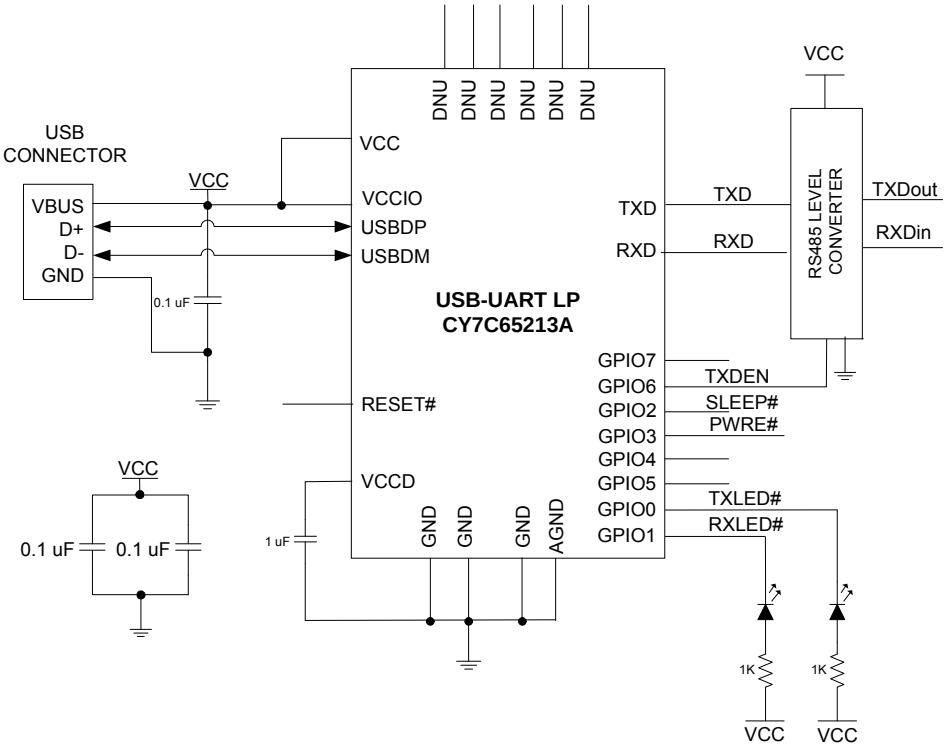
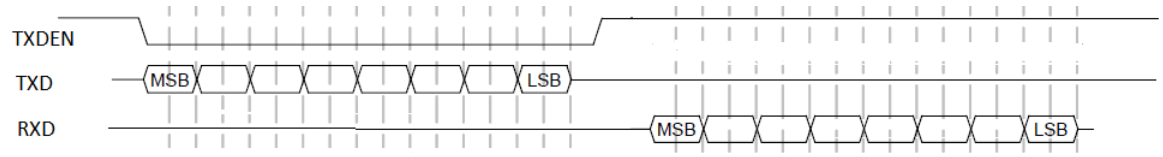


Figure 6. RS485 GPIO (TXDEN) Timing diagram



Battery Operated Bus-Powered USB to MCU with Battery Charge Detection

Figure 7 illustrates CY7C65213/CY7C65213A as a USB-to-microcontroller interface. The TXD and RXD lines are used for data transfer, and the RTS# and CTS# lines are used for handshaking. GPIO4 is configured as SLEEP# to indicate to the MCU if the device is in the USB Suspend mode, and the RI# pin is configured to wake up the USB host controller from the Suspend mode.

This application illustrates a battery-operated system, which is bus-powered. CY7C65213/CY7C65213A implements the battery charger detection functionality based on the USB Battery Charging Specification Rev. 1.2.

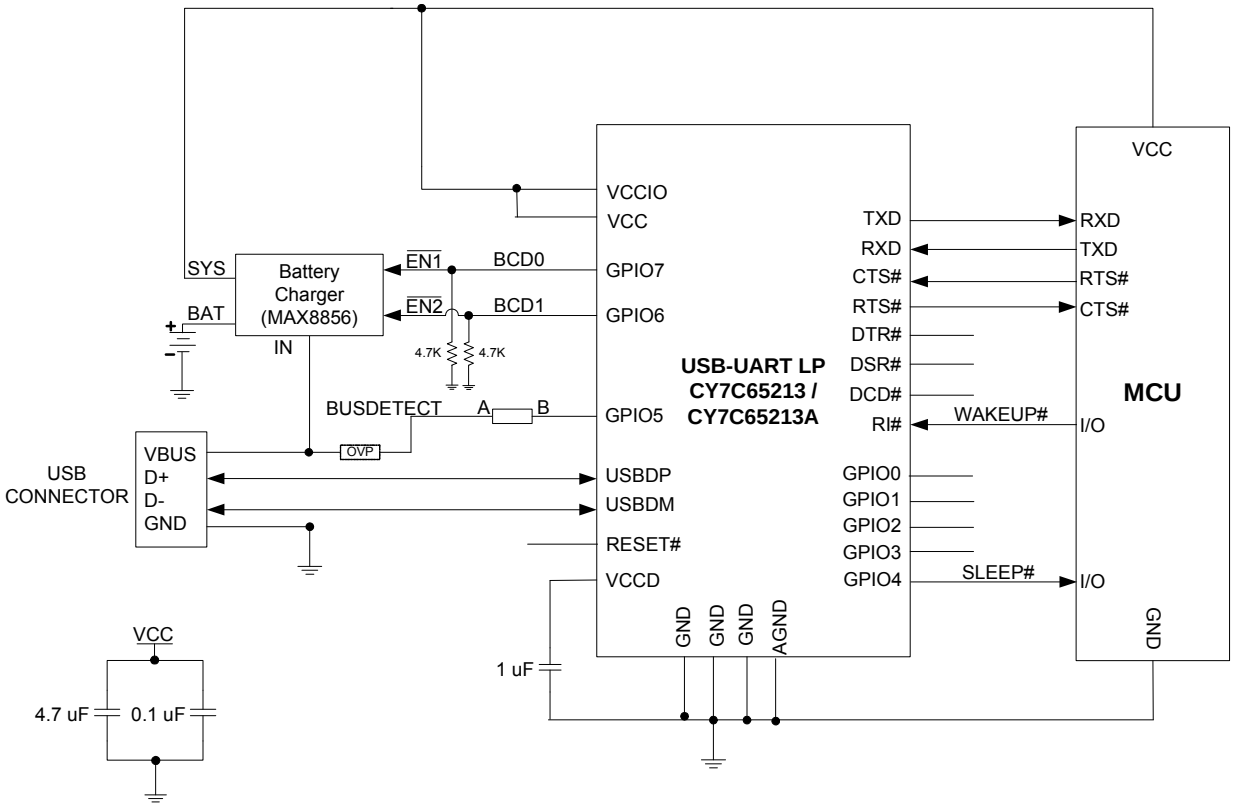
Battery-operated bus power systems must comply with the following conditions:

1. The system can be powered from the battery (if not discharged) and can be operational if the VBUS is not connected or powered down.
2. The system should not draw more than 100 mA from the VBUS prior to USB enumeration and USB Suspend.
3. The system should not draw more than 500 mA for SDP and 1.5 A for CDP/DCP.

To comply with the first requirement, the VBUS from the USB host is connected to the battery charger and to CY7C65213/CY7C65213A, as shown in Figure 7. When the VBUS is connected, CY7C65213/CY7C65213A initiates battery charger detection and indicates the type of USB charger over BCD0 and BCD1. If the USB charger is SDP or CDP, CY7C65213/CY7C65213A enables a 1.5-KΩ pull-up resistor on the USBDP for Full-Speed enumeration. When the VBUS is disconnected, CY7C65213/CY7C65213A indicates an absence of the USB charger over BCD0 and BCD1, and removes the 1.5-KΩ pull-up resistor on the USBDP. Removing this resistor ensures that no current flows from the supply to the USB host through the USBDP pin, to comply with the USB 2.0 specification.

To comply with the second and third requirements, the BCD0 and BCD1 signals are configured over GPIO to communicate the type of USB charger and the amount of current the battery charger can draw from the VBUS. The BCD0 and BCD1 signals can be configured using the configuration utility.

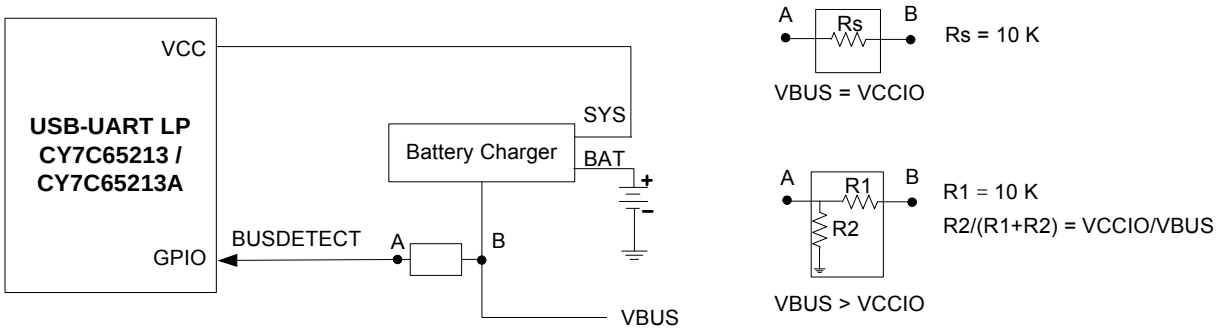
Figure 7. Battery-Operated Bus-Powered USB to MCU with Battery Charge Detection [8]



Note
8. Add a 100 KΩ pull-down resistor on the VBUS pin for quick discharge.

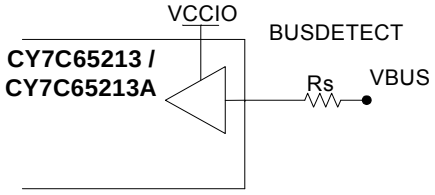
In a battery charger system, a 9-V spike on the VBUS is possible. The CY7C65213 VCC pin is intolerant to voltage above 6 V. In the absence of over-voltage protection (OVP) on the VBUS line, the VBUS should be connected to BUSDETECT (GPIO configured) using the resistive network and the output of the battery charger to the VCC pin of CY7C65213, as shown in the following figure.

Figure 8. GPIO VBUS Detect (BUSDETECT)



When VBUS and VCCIO are at the same voltage potential, the VBUS can be connected to GPIO using a series resistor (Rs). This is shown in the following figure. If there is a charger failure and the VBUS becomes 9 V, then the 10-kΩ resistor plays two roles. It reduces the amount of current flowing into the now forward-biased diodes in the GPIO, and it reduces the voltage seen on the pad.

Figure 9. GPIO VBUS Detection, VBUS = VCCIO



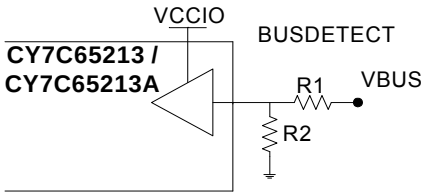
When VBUS > VCCIO, a resistor voltage divider is required to reduce the voltage from the VBUS down to VCCIO for the GPIO sensing the VBUS voltage. This is shown in Figure 10.

The resistors should be sized as follows:

- R1 ≥ 10 k
- R2 / (R1 + R2) = VCCIO / VBUS

The first condition limits the voltage and current for the charger failure situation, as described in the previous paragraph, while the second condition allows for normal-operation VBUS detection.

Figure 10. GPIO VBUS Detection, VBUS > VCCIO



LED Interface

Any GPIO can be configured to drive an LED. Three configuration options (TXLED#, RXLED#, and TX or RX LED#) are available for driving LEDs. Refer to Table 13 on page 14.

The following figure shows an example of the CY7C65213 drive single-LED configuration and dual-LED configurations, respectively. In the single-LED configuration, the GPIO pin is used to indicate when data is transmitted or received over USB by the device (TX or RX LED#). In the dual-LED configuration, when data is transmitted or received over USB, the respective GPIO pins will drive the LED to indicate the transfer.

Figure 11. Single-LED Configuration

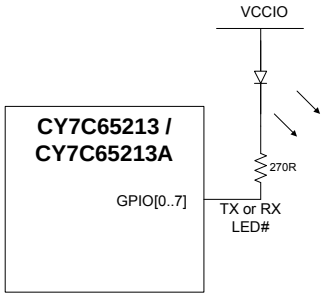
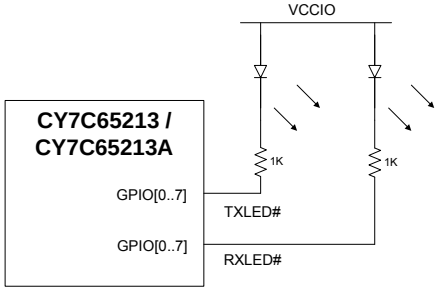


Figure 12. Double-LED Configuration



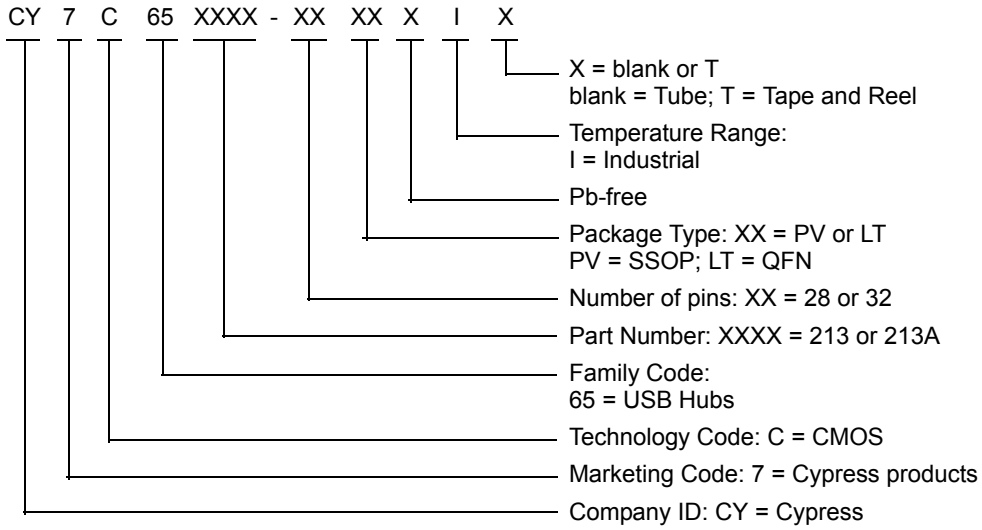
Ordering Information

Table 14 lists the CY7C65213 key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are seeking, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

Table 14. Key Features and Ordering Information

Package	Ordering Code	Operating Range
28-pin SSOP (10 × 7.5 × 1.65 mm, 0.65 mm pitch)	CY7C65213-28PVXI	Industrial
32-pin QFN (5 × 5 × 1 mm, 0.5 mm pitch) (Pb-free)	CY7C65213-32LTXI	Industrial
32-pin QFN (5 × 5 × 1 mm, 0.5 mm pitch) (Pb-free) – Tape and Reel	CY7C65213-32LTXIT	Industrial
28-pin SSOP (10 × 7.5 × 1.65 mm, 0.65 mm pitch)	CY7C65213A-28PVXI	Industrial
32-pin QFN (5 × 5 × 1 mm, 0.5 mm pitch) (Pb-free)	CY7C65213A-32LTXI	Industrial
32-pin QFN (5 × 5 × 1 mm, 0.5 mm pitch) (Pb-free) – Tape and Reel	CY7C65213A-32LTXIT	Industrial

Ordering Code Definitions



Package Information

Figure 13. 32-pin QFN (5 × 5 × 1.0 mm) LT32B 3.5 × 3.5 E-Pad (Sawn) Package Outline, 001-30999

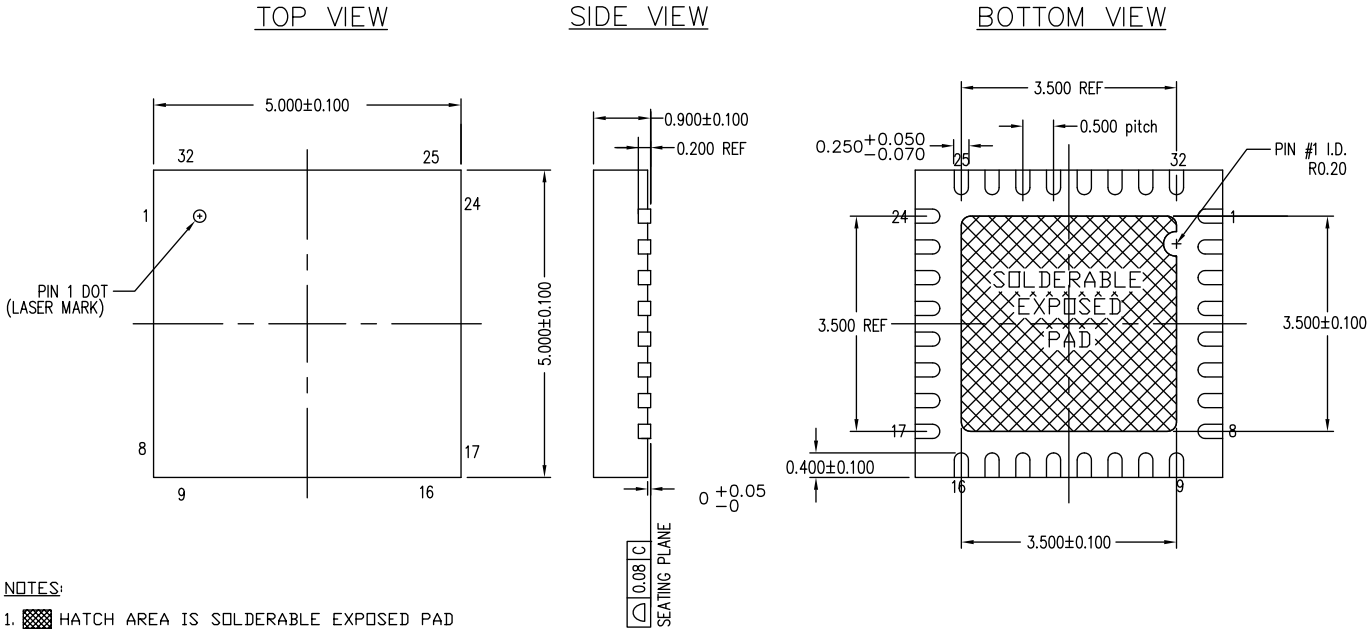


Figure 14. 28-pin SSOP (210 Mils) Package Outline, 51-85079

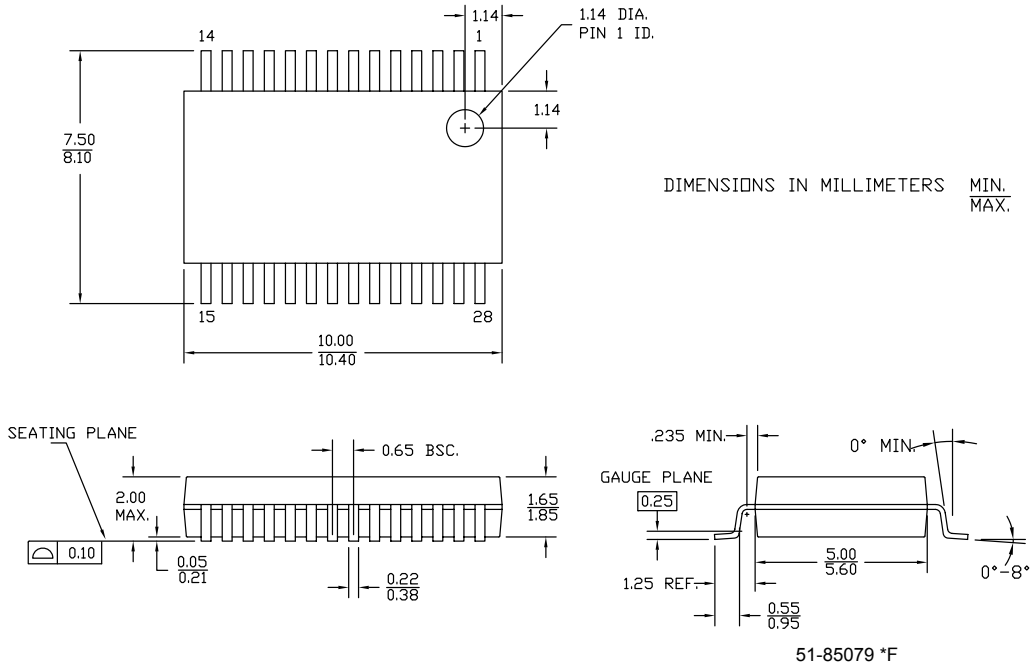


Table 15. Package Characteristics

Parameter	Description	Min	Typ	Max	Units
T_A	Operating ambient temperature	–40	25	85	°C
THJ	Package θ_{JA} (32-pin QFN)	–	19	–	°C/W
	Package θ_{JA} (28-pin SSOP)	–	62	–	°C/W

Table 16. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
32-pin QFN	260 °C	30 seconds
28-pin SSOP	260 °C	30 seconds

Table 17. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
32-pin QFN	MSL3
28-pin SSOP	MSL3

Acronyms

Table 18. Acronyms Used in this Document

Acronym	Description
BCD	battery charger detection
CDC	communication driver class
CDP	charging downstream port
DCP	dedicated charging port
DLL	dynamic link library
ESD	electrostatic discharge
GPIO	general-purpose input/output
HBM	human-body model
MCU	microcontroller unit
OSC	oscillator
PHDC	personal health care device class
PID	product identification
SDP	standard downstream port
SIE	serial interface engine
VCOM	virtual communication port
USB	Universal Serial Bus
UART	universal asynchronous receiver transmitter
VID	vendor identification

Document Conventions

Units of Measure

Table 19. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
DMIPS	Dhrystone million instructions per second
kΩ	kilo-ohm
KB	kilobyte
kHz	kilohertz
kV	kilovolt
Mbps	megabits per second
MHz	megahertz
mm	millimeter
V	volt

Document History Page

Document Title: CY7C65213/CY7C65213A, USB-UART LP Bridge Controller Document Number: 001-81011				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E	4019327	ZKR	06/13/2013	Changed status from Preliminary to Final.
*F	4105000	SAMT	08/26/2013	Final production release of datasheet.
*G	4250679	MVTA	01/17/2014	Updated Features. Updated Functional Overview: Updated description. Updated UART Interface: Updated UART Flow Control: Updated description. Updated System Resources: Updated Power System: Updated description. Updated Software: Updated Windows-CE support: Updated description. Updated Internal Flash Configuration: Updated description. Updated Table 2. Updated Electrical Specifications: Updated Device-Level Specifications: Updated Table 4. Updated GPIO: Updated Table 5. Updated Pin Description: Added Table 11. Updated Table 12. Updated USB Power Configuration: Updated USB Bus-Powered Configuration: Updated Figure 1. Updated Self-Powered Configuration: Updated Figure 2. Updated USB Bus Powered with Variable I/O Voltage: Updated Figure 3. Updated Application Examples: Updated USB to RS232 Converter: Updated description. Added Figure 4. Removed the figure “USB to RS232 Converter (32-pin QFN package)”. Updated Battery Operated Bus-Powered USB to MCU with Battery Charge Detection: Updated description. Added Figure 7. Removed the figure “Battery-Operated Bus-Powered USB to MCU with Battery Charge Detection (32-pin QFN package)”. Updated Ordering Information (Updated part numbers). Updated Package Information: Added Figure 14. Updated Table 15, Table 16, Table 17.
*H	4287738	SAMT	02/21/2014	Updated Ordering Information (Updated part numbers).

Document History Page *(continued)*

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Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*I	4430603	MVTA	07/11/2014	Updated Features. Updated Functional Overview: Updated Software: Updated Drivers for Windows Operating Systems: Updated description. Updated Internal Flash Configuration: Updated Table 2: Updated details in “Description” column of “Type” parameter. Updated Electrical Specifications: Updated Device-Level Specifications: Updated Table 3: Updated details in “Details/Conditions” column of V_{CC} and V_{CCIO} parameters. Updated typical and maximum values of I_{CC1} parameter. Updated details in “Details/Conditions” column of I_{CC1} parameter. Updated USB Power Configuration: Updated USB Bus-Powered Configuration: Updated Figure 1. Updated Self-Powered Configuration: Updated description. Updated Figure 2. Completing Sunset Review.
*J	4455825	MVTA	01/19/2015	Added More Information. Updated Package Information: spec 51-85079 – Changed revision from *E to *F. Updated to new template.
*K	4807404	MVTA / RRSH	06/23/2015	Updated Features. Updated Applications. Updated Functional Overview: Updated Serial Communication: Updated UART Interface: Updated description. Updated System Resources: Updated Power System: Updated description. Updated Internal 32-kHz Oscillator: Updated description. Updated Reset: Updated description. Updated Software: Updated Drivers for Windows Operating Systems: Updated description. Updated Windows-CE support: Updated description. Updated Electrical Specifications: Updated Operating Conditions: Updated details corresponding to “V_{CC} supply voltage”. Updated Device-Level Specifications: Updated Table 3: Changed maximum value of V_{CC} parameter from 5.25 V to 5.5 V. Updated GPIO: Updated Table 5: Updated details in “Description” column of V_{OH} and V_{OL} parameters.

Document History Page *(continued)*

Document Title: CY7C65213/CY7C65213A, USB-UART LP Bridge Controller Document Number: 001-81011				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*K (cont.)	4807404	MVTA / RRSH	06/23/2015	Updated Pin Description: Updated Table 11: Updated details in “Description” column of pin 20. Updated Table 12: Updated details in “Description” column of pin 19. Updated Table 13: Added Note 5 and referred the same note in description of “TRISTATE” GPIO Configuration Option. Updated USB Power Configuration: Updated USB Bus-Powered Configuration: Updated Figure 1. Updated Self-Powered Configuration: Updated Figure 2. Updated USB Bus Powered with Variable I/O Voltage: Updated Figure 3. Updated Application Examples: Updated USB to RS232 Converter: Updated Figure 4. Updated Battery Operated Bus-Powered USB to MCU with Battery Charge Detection: Updated Figure 7. Updated to new template. Completing Sunset Review.
*L	5063358	MVTA	12/24/2015	Updated Document Title to read as “CY7C65213/CY7C65213A, USB-UART LP Bridge Controller”. Included details of CY7C65213A part number in all instances across the document. Updated Features: Updated description. Updated More Information: Updated description. Updated Functional Overview: Updated Serial Communication: Updated UART Interface: Updated description. Updated UART Flow Control: Updated description. Updated Electrical Specifications: Updated Operating Conditions: Updated details corresponding to “V_{CC} supply voltage”. Updated Device-Level Specifications: Updated Table 3: Changed maximum value of V_{CC} parameter from 5.5 V to 5.25 V. Updated details in “Details/Conditions” column corresponding to I_{CC2} parameter. Updated Pin Description: Updated details in “Description” column corresponding to VCC pin. Updated Application Examples: Added USB to RS485 Application. Updated Ordering Information: Updated part numbers. Updated Ordering Code Definitions.
*M	5396700	MVTA	08/09/2016	Added CY7C65213 and CY7C65213-A Features Comparison. Updated the Cypress logo and copyright information. Updated Sales, Solutions, and Legal Information.

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