

## 128Kx24 SRAM 3.3 Volt FEATURES

- 128Kx24 bit CMOS Static
- Random Access Memory Array
  - Fast Access Times: 10, 12, and 15ns
  - Master Output Enable and Write Control
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- Surface Mount Package
  - 119 Lead BGA (JEDEC MO-163), No. 391
  - Small Footprint, 14mm x 22mm
  - Multiple Ground Pins for Maximum
- Noise Immunity
- Single +3.3V (±5%) Supply Operation
- DSP Memory Solution
- Motorola DSP5630xTM
- Analog Devices SHARCTM

## DESCRIPTION

The EDI8L24129VxxBC is a 3.3V, three megabit SRAM constructed with three 128Kx8 die mounted on a multi-layer laminate substrate. With 10 to 15ns access times, x24 width and a 3.3V operating voltage, the EDI8L24129V is ideal for creating a single chip memory solution for the Motorola DSP5630x (Figure 3) or a two chip solution for the Analog Devices SHARCTM DSP (Figure 4).

The single or dual chip memory solutions offer improved system performance by reducing the length of board traces and the number of board connections compared to using multiple monolithic devices. For example, the capacitance load on the data lines for the BGA package is 58% less than a monolithic SOJ solution.

The JEDEC Standard 119 lead BGA provides a 44% space savings over using 128Kx8, 300mil wide SOJs and the BGA package has a maximum height of 100 mils compared to 148 mils for the SOJ packages. The BGA package also allows the use of the same manufacturing and inspection techniques as the Motorola DSP, which is also in a BGA package.

### PIN CONFIGURATION

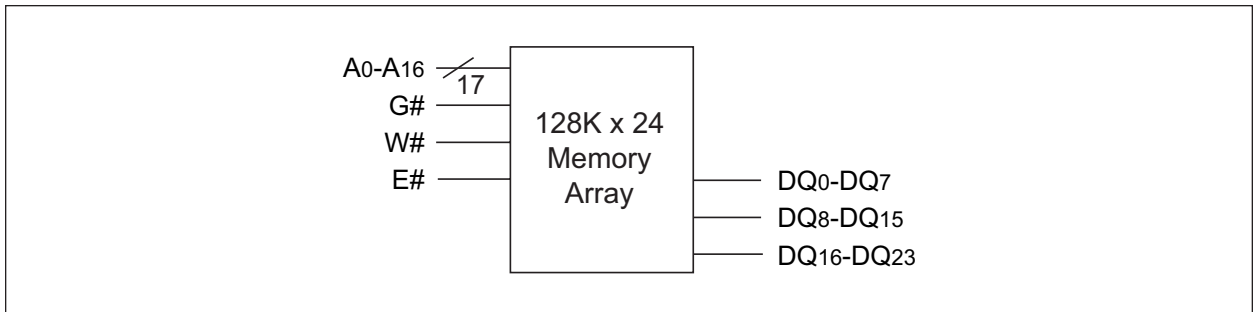
|          | 1     | 2               | 3               | 4   | 5               | 6               | 7     |
|----------|-------|-----------------|-----------------|-----|-----------------|-----------------|-------|
| <b>A</b> | NC    | AO              | A1              | A2  | A3              | A4              | NC    |
| <b>B</b> | NC    | A5              | A6              | E#  | A7              | A8              | NC    |
| <b>C</b> | I/012 | NC              | NC              | NC  | NC              | NC              | I/00  |
| <b>D</b> | I/013 | V <sub>CC</sub> | GND             | GND | GND             | V <sub>CC</sub> | I/01  |
| <b>E</b> | I/014 | GND             | V <sub>CC</sub> | GND | V <sub>CC</sub> | GND             | I/02  |
| <b>F</b> | I/015 | V <sub>CC</sub> | GND             | GND | GND             | V <sub>CC</sub> | I/03  |
| <b>G</b> | I/016 | GND             | V <sub>CC</sub> | GND | V <sub>CC</sub> | GND             | I/04  |
| <b>H</b> | I/017 | V <sub>CC</sub> | GND             | GND | GND             | V <sub>CC</sub> | I/05  |
| <b>I</b> | NC    | GND             | V <sub>CC</sub> | GND | V <sub>CC</sub> | GND             | NC    |
| <b>J</b> | I/018 | V <sub>CC</sub> | GND             | GND | GND             | V <sub>CC</sub> | I/06  |
| <b>K</b> | I/019 | GND             | V <sub>CC</sub> | GND | V <sub>CC</sub> | GND             | I/07  |
| <b>L</b> | I/020 | V <sub>CC</sub> | GND             | GND | GND             | V <sub>CC</sub> | I/08  |
| <b>M</b> | I/021 | GND             | V <sub>CC</sub> | GND | V <sub>CC</sub> | GND             | I/09  |
| <b>N</b> | I/022 | V <sub>CC</sub> | GND             | GND | GND             | V <sub>CC</sub> | I/010 |
| <b>O</b> | I/023 | NC              | NC              | NC  | NC              | NC              | I/011 |
| <b>P</b> | NC    | A9              | A10             | W#  | A11             | A12             | NC    |
| <b>Q</b> | NC    | A13             | A14             | G#  | A15             | A16             | NC    |

### PIN NAMES

|                 |                          |
|-----------------|--------------------------|
| A0-A16          | Address Inputs           |
| E#              | Chip Enable              |
| W#              | Master Write Enable      |
| G#              | Master Output Enable     |
| DQ0-DQ23        | Common Data Input/Output |
| V <sub>CC</sub> | Power (3.3V±5%)          |
| GND             | Ground                   |
| NC              | No Connection            |



**BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

|  |                 |
|--|-----------------|
| Voltage on any pin relative to V <sub>SS</sub> | -0.5V to 4.6V   |
| Operating Temperature TA (Ambient)             | 0°C to +70°C    |
| Commercial                                     | 0°C to +70°C    |
| Industrial                                     | -40°C to +85°C  |
| Storage Temperature                            | -55°C to +125°C |
| Power Dissipation                              | 1.5 Watts       |
| Output Current.                                | 50 mA           |
| Junction Temperature, T <sub>J</sub>           | 175°C           |

\* Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED OPERATING CONDITIONS**

| Parameter          | Sym             | Min   | Typ | Max                  | Units |
|--------------------|-----------------|-------|-----|----------------------|-------|
| Supply Voltage     | V <sub>CC</sub> | 3.135 | 3.3 | 3.465                | V     |
| Supply Voltage     | V <sub>SS</sub> | 0     | 0   | 0                    | V     |
| Input High Voltage | V <sub>IH</sub> | 2.2   | –   | V <sub>CC</sub> +0.3 | V     |
| Input Low Voltage  | V <sub>IL</sub> | -0.3  | –   | 0.8                  | V     |

**TRUTH TABLE**

| G# | E# | W# | Mode            | Output | Power                               |
|----|----|----|-----------------|--------|-------------------------------------|
| X  | H  | X  | Standby         | High Z | I <sub>CC2</sub> , I <sub>CC3</sub> |
| H  | L  | H  | Output Deselect | High Z | I <sub>CC1</sub>                    |
| L  | L  | H  | Read            | DOUT   | I <sub>CC1</sub>                    |
| X  | L  | L  | Write           | DIN    | I <sub>CC1</sub>                    |

**CAPACITANCE**

f=1.0MHz, V<sub>IN</sub>=V<sub>CC</sub> or V<sub>SS</sub>

| Parameter                   | Sym     | Max | Unit |
|-----------------------------|---------|-----|------|
| Address Lines               | CA      | 8   | pF   |
| Data Lines                  | CD/Q    | 10  | pF   |
| Write & Output Enable Lines | W#, G#  | 8   | pF   |
| Chip Enable Lines           | E0#-E2# | 8   | pF   |

These parameters are sampled, not 100% tested.

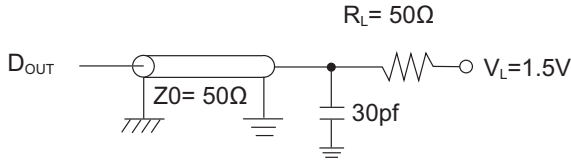


**DC ELECTRICAL CHARACTERISTICS**

| Parameter                        | Sym              | Conditions  | Min | Max  |         | Units |
|----------------------------------|------------------|---|-----|------|---------|-------|
|                                  |                  |   |     | 10ns | 12-15ns |       |
| Operating Power Supply Current   | I <sub>CC1</sub> | W# = V <sub>IL</sub> , I/I/O = 0mA,<br>Min Cycle  |     | 420  | 360     | mA    |
| Standby (TTL) Supply Current     | I <sub>CC2</sub> | E# > V <sub>IH</sub> , V <sub>IN</sub> < V <sub>IL</sub> or<br>V <sub>IN</sub> > V <sub>IH</sub> , f=ØMHz |     | 90   | 75      | mA    |
| Full Standby CMOS Supply Current | I <sub>CC3</sub> | E# > V <sub>CC</sub> -0.2V<br>V <sub>IN</sub> > V <sub>CC</sub> -0.2V or<br>V <sub>IN</sub> < 0.2V        |     | 10   | 10      | mA    |
| Input Leakage Current            | I <sub>LI</sub>  | V <sub>IN</sub> = 0V to V <sub>CC</sub>   |     | ±10  | ±10     | µA    |
| Output Leakage Current           | I <sub>LO</sub>  | V I/O = 0V to V <sub>CC</sub>   |     | ±10  | ±10     | µA    |
| Output High Voltage              | V <sub>OH</sub>  | I <sub>OH</sub> = -4.0mA  | 2.4 |      |         | V     |
| Output Low Voltage               | V <sub>OL</sub>  | I <sub>OL</sub> = 8.0mA   |     | 0.4  | 0.4     | V     |

**AC TEST CIRCUIT**

**Figure 1**

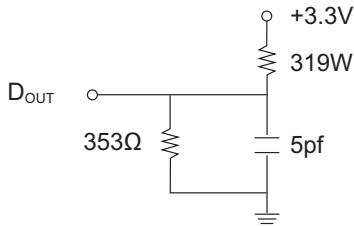


**AC TEST CONDITIONS**

|                                |                         |
|--------------------------------|-------------------------|
| Input Pulse Levels             | V <sub>SS</sub> to 3.0V |
| Input Rise and Fall Times      | 5ns                     |
| Input and Output Timing Levels | 1.5V                    |
| Output Load                    | Figure 1                |

(NOTE: For t<sub>EH0Z</sub>, t<sub>GH0Z</sub> and t<sub>W0Z</sub>, Figure 2)

**Figure 2**



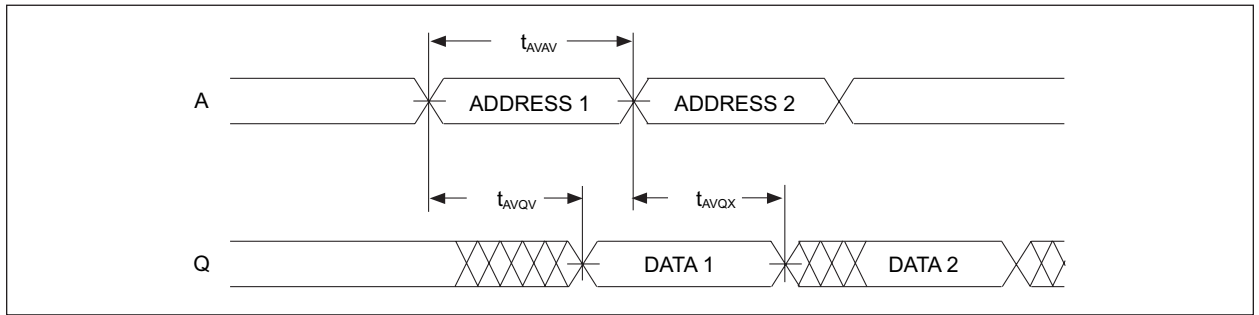


AC CHARACTERISTICS – READ CYCLE

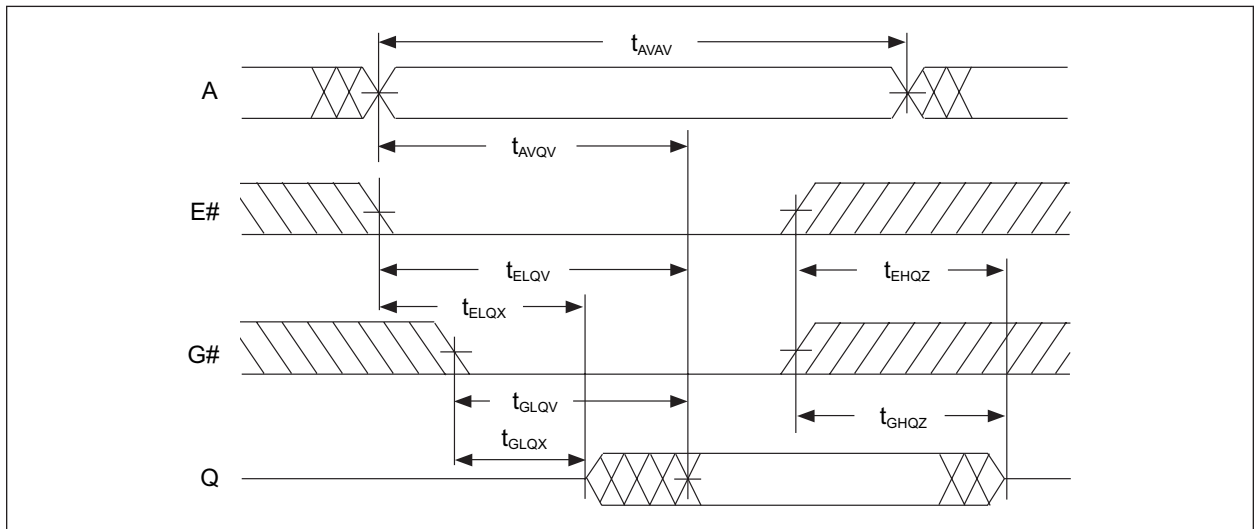
| Parameter                             | Symbol            |                  | 10ns |     | 12ns |     | 15ns |     | Units |
|---------------------------------------|-------------------|------------------|------|-----|------|-----|------|-----|-------|
|                                       | JEDEC             | Alt.             | Min  | Max | Min  | Max | Min  | Max |       |
| Read Cycle Time                       | t <sub>AVAV</sub> | t <sub>RC</sub>  | 10   |     | 12   |     | 15   |     | ns    |
| Address Access Time                   | t <sub>AVQV</sub> | t <sub>AA</sub>  |      | 10  |      | 12  |      | 15  | ns    |
| Chip Enable Access Time               | t <sub>ELQV</sub> | t <sub>ACS</sub> |      | 10  |      | 12  |      | 15  | ns    |
| Chip Enable to Output in Low Z (1)    | t <sub>ELQX</sub> | t <sub>CLZ</sub> | 3    |     | 3    |     | 3    |     | ns    |
| Chip Disable to Output in High Z (1)  | t <sub>EHQZ</sub> | t <sub>CHZ</sub> |      | 5   |      | 6   |      | 7   | ns    |
| Output Hold from Address Change       | t <sub>AVQX</sub> | t <sub>OH</sub>  | 3    |     | 3    |     | 3    |     | ns    |
| Output Enable to Output Valid         | t <sub>GLQV</sub> | t <sub>OE</sub>  |      | 5   |      | 6   |      | 7   | ns    |
| Output Enable to Output in Low Z (1)  | t <sub>GLQX</sub> | t <sub>OLZ</sub> | 0    |     | 0    |     | 0    |     | ns    |
| Output Disable to Output in High Z(1) | t <sub>GHQZ</sub> | t <sub>OHZ</sub> |      | 5   |      | 6   |      | 7   | ns    |

Note 1: Parameter guaranteed, but not tested.

READ CYCLE – W# HIGH, G#, E# LOW



READ CYCLE 2 – W# HIGH



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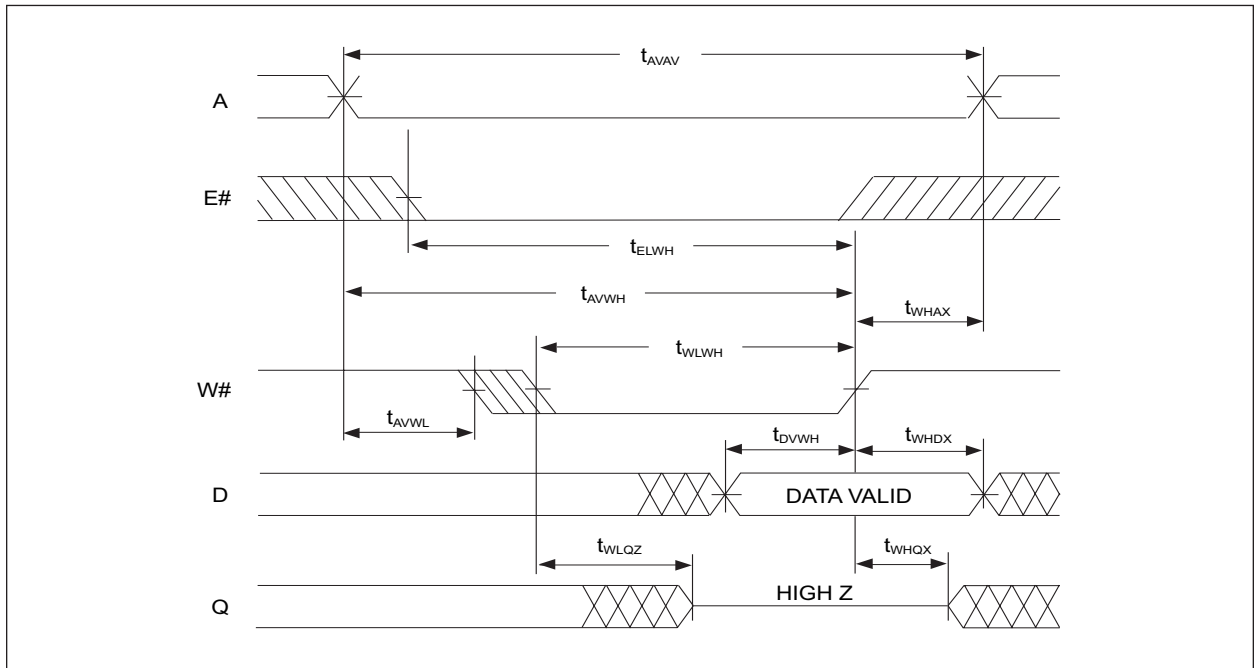


AC CHARACTERISTICS – WRITE CYCLE

| Parameter                           | Symbol            |                  | 10ns |     | 12ns |     | 15ns |     | Units |
|-------------------------------------|-------------------|------------------|------|-----|------|-----|------|-----|-------|
|                                     | JEDEC             | Alt.             | Min  | Max | Min  | Max | Min  | Max |       |
| Write Cycle Time                    | t <sub>AVAV</sub> | t <sub>WC</sub>  | 10   |     | 12   |     | 15   |     | ns    |
| Chip Enable to End of Write         | t <sub>ELWH</sub> | t <sub>CW</sub>  | 8    |     | 9    |     | 9    |     | ns    |
|                                     | t <sub>ELEH</sub> | t <sub>CW</sub>  | 8    |     | 9    |     | 9    |     | ns    |
| Address Setup Time                  | t <sub>AVWL</sub> | t <sub>AS</sub>  | 0    |     | 0    |     | 0    |     | ns    |
|                                     | t <sub>AVEL</sub> | t <sub>AS</sub>  | 0    |     | 0    |     | 0    |     | ns    |
| Address Valid to End of Write       | t <sub>AVWH</sub> | t <sub>AW</sub>  | 8    |     | 9    |     | 10   |     | ns    |
|                                     | t <sub>AVEH</sub> | t <sub>AW</sub>  | 8    |     | 9    |     | 10   |     | ns    |
| Write Pulse Width                   | t <sub>WLWH</sub> | t <sub>WP</sub>  | 8    |     | 10   |     | 11   |     | ns    |
|                                     | t <sub>WLEH</sub> | t <sub>WP</sub>  | 8    |     | 10   |     | 11   |     | ns    |
| Write Recovery Time                 | t <sub>WHAX</sub> | t <sub>WR</sub>  | 0    |     | 0    |     | 0    |     | ns    |
|                                     | t <sub>EHAX</sub> | t <sub>WR</sub>  | 0    |     | 0    |     | 0    |     | ns    |
| Data Hold Time                      | t <sub>WHDX</sub> | t <sub>DH</sub>  | 0    |     | 0    |     | 0    |     | ns    |
|                                     | t <sub>EHDX</sub> | t <sub>DH</sub>  | 0    |     | 0    |     | 0    |     | ns    |
| Write to Output in High Z (1)       | t <sub>WLQZ</sub> | t <sub>WHZ</sub> | 0    | 5   | 0    | 6   | 0    | 7   | ns    |
| Data to Write Time                  | t <sub>DVWH</sub> | t <sub>DW</sub>  | 6    |     | 6    |     | 7    |     | ns    |
|                                     | t <sub>DVEH</sub> | t <sub>DW</sub>  | 6    |     | 6    |     | 7    |     | ns    |
| Output Active from End of Write (1) | t <sub>WHQX</sub> | t <sub>WLZ</sub> | 3    |     | 3    |     | 3    |     | ns    |

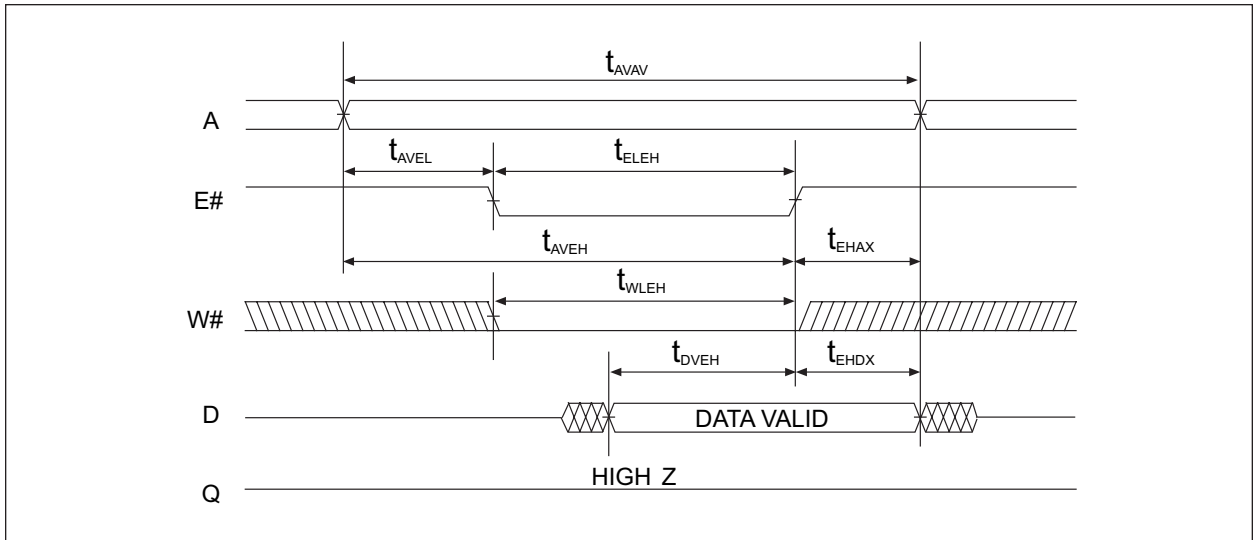
Note 1: Parameter guaranteed, but not tested.

WRITE CYCLE – W# CONTROLLED





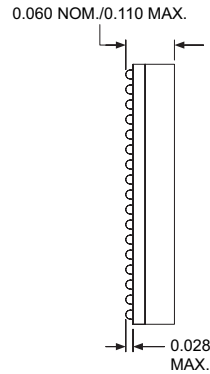
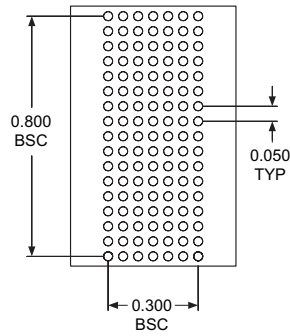
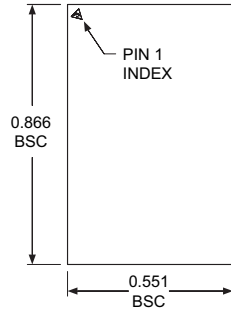
WRITE CYCLE 2 – E# CONTROLLED





**PACKAGE DESCRIPTION**

Package No. 391  
119 Lead BGA  
JEDEC MO-163



**ORDERING INFORMATION**

**Commercial (0°C to +70°C)**

| Part Number     | Speed (ns) | Package No. |
|-----------------|------------|-------------|
| EDI8L24129V10BC | 10         | 391         |
| EDI8L24129V12BC | 12         | 391         |
| EDI8L24129V15BC | 15         | 391         |

**Industrial (-40°C to +85°C)**

| Part Number     | Speed (ns) | Package No. |
|-----------------|------------|-------------|
| EDI8L24129V10BI | 10         | 391         |
| EDI8L24129V12BI | 12         | 391         |
| EDI8L24129V15BI | 15         | 391         |

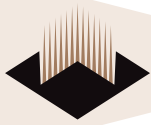


FIGURE 3 – INTERFACING THE MOTOROLA DSP5630X DSP FAMILY WITH THE EDI8L24129V (128KX24)

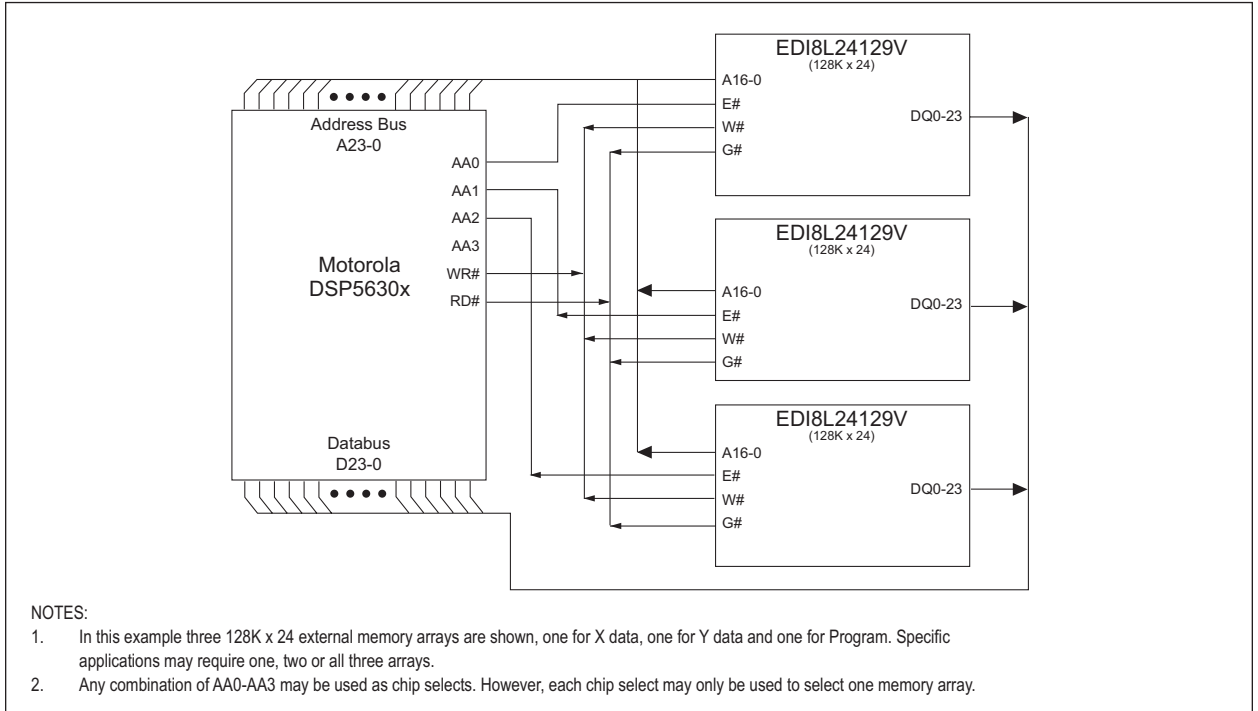


FIGURE 4 – INTERFACING THE 21060L OR THE 21062L TO THE EDI8L24129V, 119 BGA (CREATING A 128KX48 MEMORY ARRAY)

