Three Phase Multifunction Energy Metering IC with SPI Interface

SA9904B

FEATURES

- Bidirectional active and reactive power/energy measurement
- RMS voltage and frequency measurement
- Individual Phase information
- SPI communication bus
- Meets the IEC 61036 Specification requirements for Class 1 AC Watt hour meters

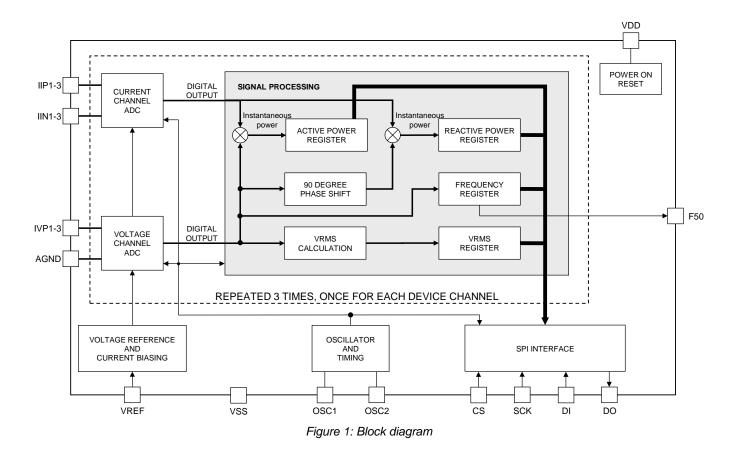
DESCRIPTION

The SA9904B is a three phase bidirectional energy/power metering integrated circuit that has been designed to measure active and reactive energy, RMS mains voltage and mains frequency. The SA9904B has an integrated SPI serial interface for communication with a microcontroller. Measured values for active and reactive energy, the mains voltage and frequency for each phase are accessible through the SPI interface from 24 bit registers. The SA9904B active and reactive energy registers are capable of holding at least 52 seconds of accumulated energy at full load. A mains voltage zero crossover is available on the F50 output.

- Meets the IEC 61268 Specification requirements for Class 2 AC VAR hour meters
- Protected against ESD
- Total power consumption rating below 60mW
- Uses current transformers for current sensing
- Operates over a wide temperature range
- Precision on-chip voltage reference
- Measures AC inputs only

The SA9904B includes all the required functions for three phase power and energy measurement such as oversampling A/D converters for the voltage and current sense inputs, power calculation and energy integration. This innovative universal three phase power/energy metering integrated circuit is ideally suited for energy calculations in applications such as electricity dispensing systems, residential metering and factory energy metering and control.

The SA9904B integrated circuit is available in a 20 pin small outline (SOIC20) RoHS compliant package.







ELECTRICAL CHARACTERISTICS

 $(V_{DD} - V_{SS} = 5V \pm 10\%)$, over the temperature range -40°C to +85°C, unless otherwise specified. Refer to Figure 2 "Test circuit for electrical characteristics".)

Parameter	Symbol	Min	Тур	Max	Unit	Condition
General		•	•			
Supply Voltage: Positive	V _{DD}	2.25	2.5	2.75	V	With respect to AGND
Supply Voltage: Negative	Vss	-2.75	-2.5	-2.25	V	With respect to AGND
Supply Current: Positive	lod		9.5	11	mA	
Supply Current: Negative	lss		-9.5	-11	mA	
Analog Inputs						
Current Sensor Inputs (Differential)						
Input Current Range	IR11P1, IR11P2, IR11P3, IR11N1, IR11N2, IR11N3	-25		25	μA	Peak value
Offset Voltage	VOIIP1, VOIIP2, VOIIP3, VOIIN1, VOIIN2, VOIIN3	-4		4	mV	With R = $4.7k\Omega$ connected to AGND
Voltage Sensor Inputs (Asymmetrical)						
Input Current Range	IRIVP1, IRIVP2, IRIVP3	-25		25	μA	Peak value
Offset Voltage	VOIVP1, VOIVP2, VOIVP3	-4		4	mV	With R = $4.7k\Omega$ connected to AGND
Digital Inputs		•	•			•
SCK, CS, DI Input High Voltage V _{IH} Input Low Voltage V _{IL}		V _{DD} -1		V _{SS} +1	V V	
SCKMaximum clock frequency f_{SCK} Minimum clock low time t_{LO} Minimum clock high time t_{HI}		0.6 0.6		800	kHz μs μs	
Digital Outputs						
F50, DOOutput High VoltageVонOutput Low VoltageVоL		V _{DD} -1		V _{SS} +1	V V	Isource = 5mA Isink = 5mA

During manufacturing, testing and shipment we take great care to protect our products against potential external environmental damage such as Electrostatic Discharge (ESD). Although our products have ESD protection circuitry, permanent damage may occur on products subjected to high-energy electrostatic discharges accumulated on the human body and/or test equipment that can discharge without detection. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality during product handling.





ELECTRICAL CHARACTERISTICS (continued)

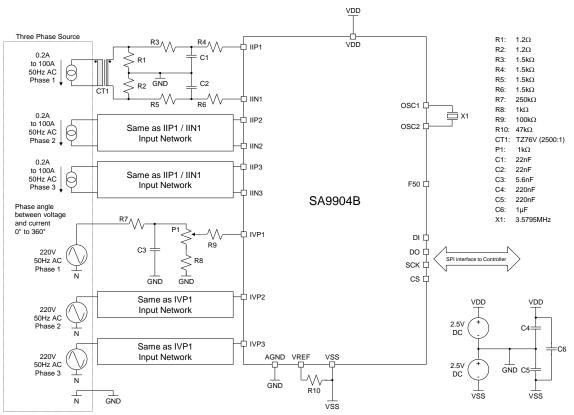
 $(V_{DD} - V_{SS} = 5V \pm 10\%)$, over the temperature range -40°C to +85°C, unless otherwise specified. Refer to Figure 2 "Test circuit for electrical characteristics".)

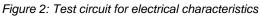
Parameter	Symbol	Min	Тур	Max	Unit	Condition
On-chip Voltage Reference						
Reference Voltage	VR	1.15	1.20	1.25	V	
Reference Current	-I _R	24.4	25.5	26.6	μA	With R = $47k\Omega$ connected to V _{SS}
Temperature Coefficient	TCR		10	70	ppm/⁰C	
Oscillator						•
Recommended crystal	fosc		3.5795		MHz	TV colour burst crystal

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Min	Мах	Unit
Supply Voltage	V _{DD} - V _{SS}		6	V
Current on any Pin	I _{PIN}	-150	150	mA
Storage Temperature	T _{STG}	-60	+125	٥C
Specified Operating Temperature Range	To	-40	+85	٥C
Limit Range of Operating Temperature	Tlimit	-40	+85	٥C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other condition above those indicated in the operational sections of this specification, is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

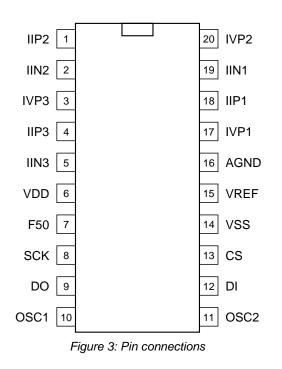






PIN DESCRIPTION

Designation	Pin No.	Description
AGND	16	Analog Ground. This is the reference pin for the current and voltage signal sensing networks. The supply voltage to this pin should be mid-way between V_{DD} and V_{SS} .
V _{DD}	6	Positive Supply Voltage. The voltage to this pin should be +2.5V \pm 10% with respect to AGND.
Vss	14	Negative Supply Voltage. The voltage to this pin should be -2.5V \pm 10% with respect to AGND.
IVP1, IVP2, IVP3	17, 20, 3	Analog Inputs for Voltages. The nominal current into the voltage sense inputs IVP should be set at $14\mu A_{RMS}$. The voltage sense inputs saturate at an input current of $\pm 25\mu A$ peak.
IIP1, IIN1, IIP2, IIN2, IIP3, IIN3	18, 19, 1, 2, 4, 5	Analog Inputs for Currents. The maximum current into the current sense inputs IIP/IIN should be set at $16\mu A_{RMS}$. The current sense inputs saturate at an input current of $\pm 25\mu A$ peak.
VREF	15	This pin provides the connection for the reference current setting resistor. A $47k\Omega$ resistor connected to V _{SS} sets the optimum operating conditions.
OSC1, OSC2	10, 11	Connection for crystal
SCK	8	SPI Serial Clock input. This pin is used to strobe data in and out of the SA9904B
CS	13	SPI Chip Select input. This input pin enables the SPI interface. It is active high.
DI	12	SPI Data In input. Input data is accepted on this pin at the rising clock edge on SCK when CS is active.
DO	9	SPI Data Out output. Output data is strobed out on this pin at the rising clock edge on SCK when CS is active. DO is not driven when CS is inactive.
F50	7	Voltage zero crossover. The F50 output generates a pulse on every rising edge of the mains voltage of an active channel.



ORDERING INFORMATION

Part Number	Package
SA9904BSAR	SOIC20 (RoHS compliant)

TERMINOLOGY

Positive Energy

Positive energy is defined when the phase difference between the input signals IIP and IVP is less than 90 degrees (-90..90 degrees).

Negative Energy

Negative energy is defined when the phase difference between the input signals IIP and IVP is greater than 90 degrees (90..270 degrees).

Percentage Error*

Percentage error is given by the following formula:

 $\% Error = \frac{Energy \ registered - True \ Energy}{True \ Energy} \times 100$

NOTE: Since the true value cannot be determined, it is approximated by a value with a stated uncertainty that can be traced to standards agreed upon between manufacturer and user or to national standards.

Rated Operating Conditions*

Set of specified measuring ranges for performance characteristics and specified operating ranges for influence quantities, within which the variations or operating errors of a meter are specified and determined.

Specified Measuring Range*

Set of values of a measured quantity for which the error of a meter is intended to lie within specified limits.

Specified Operating Range*

A range of values of a single influence quantity, which forms a part of the rated operating conditions.

Limit Range of Operation*

Extreme conditions which an operating meter can withstand without damage and without degradation of its metrological characteristics when it is subsequently operated under its rated operating conditions.

Maximum Rated Mains Current (IMAX)

Maximum rated mains current is the specified maximum current flowing through the energy meter at rated operating conditions.

Constant*

Value expressing the relation between the active energy registered by the meter and the corresponding value of the test output. If this value is a number of pulses, the constant should be either pulses per kilowatt-hour (imp/kWh) or watt-hours per pulse (Wh/imp).

Nominal Mains Voltage (VNOM)

Nominal mains voltage (V_{NOM}) is the voltage specified for the energy meter at rated operating conditions.

Maximum Channel Energy (EMAX)

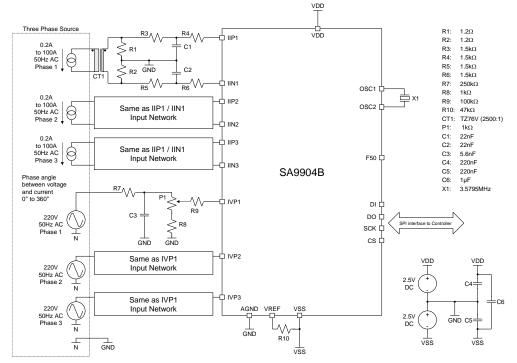
The maximum channel energy is defined as the energy registered on the active register on one channel of the SA9904B when 14μ A_{RMS} and 16μ A_{RMS} input current with zero phase shift are applied to the voltage and current inputs respectively. Both the voltage and current inputs saturate at an input current magnitude of 25μ A, or at 17.68μ A_{RMS} when using sine waves. The maximum input current on any channel is therefore defined to be 16μ A_{RMS}, which leaves about 10% headroom to the saturation point. An additional headroom of 15% is reserved on the voltage channels to account for mains voltage fluctuations. The nominal output frequency of 320000 counts per second per channel is achieved under such conditions.

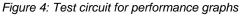
* IEC 62052-11, 2003. Electricity Metering Equipment (AC) – General Requirements, Test and Test Conditions

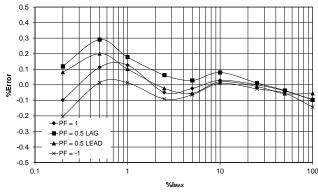


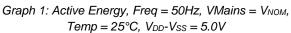


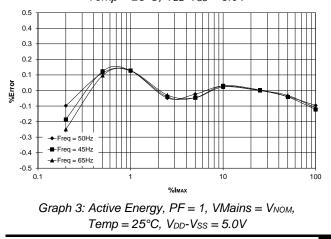
PERFORMANCE GRAPHS

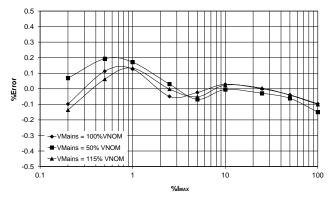




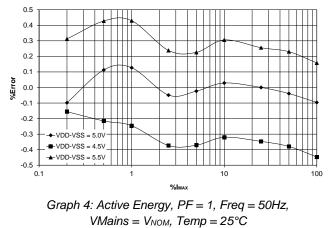


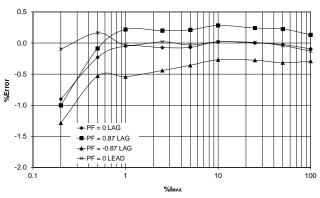


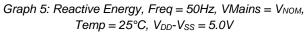


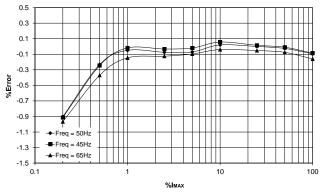


Graph 2: Active Energy, PF = 1, Freq = 50Hz, Temp = 25°C, V_{DD} - $V_{SS} = 5.0V$

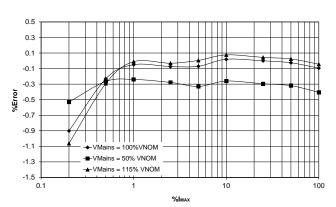




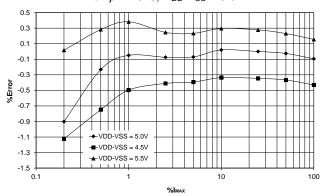




Graph 7: Reactive Energy, PF = 0 LAG, $VMains = V_{NOM}$, Temp = 25°C, V_{DD} - $V_{SS} = 5.0V$



Graph 6: Reactive Energy, PF = 0 LAG, Freq = 50Hz, Temp = 25°C, V_{DD} - $V_{SS} = 5.0\text{V}$



Graph 8: Reactive Energy, PF = 0 LAG, Freq = 50Hz, VMains = V_{NOM} , Temp = 25°C

FUNCTIONAL DESCRIPTION

The SA9904B is a CMOS mixed signal integrated circuit, which performs the measurement of active power, reactive power, RMS voltage and mains frequency. The integrated circuit includes all the required functions for three phase power and energy measurement such as oversampling A/D converters for the voltage and current sense inputs, power calculation and energy integration.

The SA9904B integrates instantaneous active and reactive power into 24 bit registers. RMS voltage and frequency are continuously measured and stored in the respective registers. The mains voltage zero crossover is available on the F50 output. The SPI interface of the SA9904B has a tri-state output that allows connection of more than one metering device on a single SPI bus.

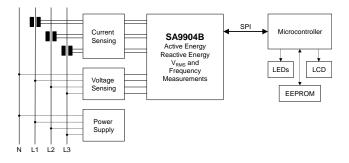


Figure 5: Typical architecture of an energy meter using the SA9904B

In the typical meter architecture, a microcontroller is used in conjunction with the SA9904B. In addition to communicating with the SA9904B the controller is used to read/write parameters to the EEPROM, output pulses for fast calibration and to display the consumed active and reactive power, V_{RMS} and mains frequency information. Other parameters such as I_{RMS}, phase angle etc. can be accurately calculated.

Theory of Operation

The SA9904B includes all the required functions for three channel multifunction power and energy measurement. Three pairs of identical AD converters sample the three phase voltage and current input signals. The three pairs of digital signals, accurately representing the voltage and current inputs, are used to calculate active energy, reactive energy, V_{RMS} and the mains frequency. These quantities are stored in 24 bit registers that can be accessed via the SPI bus. The energy registers accumulate instantaneous energy.

For given voltage and current signals the instantaneous active power is calculated by:

 $p(t) = v(t) \times i(t)$ $p(t) = V_M \cos(\omega t + \theta) \times I_M \cos(\omega t + \psi)$

Let
$$\phi = \theta - \psi$$
, and $V_{RMS} = \frac{V_M}{\sqrt{2}}$ and $I_{RMS} = \frac{I_M}{\sqrt{2}}$ then

 $p(t) = V_M \cos(\omega t + \theta) \times I_M \cos(\omega t + \theta - \phi)$ $p(t) = V_{RMS} I_{RMS} (\cos \phi + \cos(2(\omega t + \theta) - \phi))$

where

p(t) is the instantaneous power, v(t) is the instantaneous voltage signal, i(t) is the instantaneous current signal, V_M is the amplitude of the voltage signal, I_M is the amplitude of the current signal, θ is the phase angle of the voltage signal and ψ is the phase angle of the current signal.

The instantaneous power is integrated in the active energy registers. Over time this removes the double mains frequency component $\cos(2(\omega t+\theta)-\phi)$ to provide the average power information

$$P = \frac{1}{T} \int_0^T p(t) dt$$
$$P = V_{RMS} I_{RMS} \cos \phi$$

where P is the average power and $cos\phi$ is the power factor.

Reactive power is calculated by applying a 90 degree phase shift to the voltage signal before multiplication:

$$q(t) = v(t - T/_{4}) \times i(t)$$

$$q(t) = V_{M} \cos(\omega t + \theta - \pi/_{2}) \times I_{M} \cos(\omega t + \psi)$$

$$q(t) = V_{M} \sin(\omega t + \theta) \times I_{M} \cos(\omega t + \theta - \phi)$$

$$q(t) = V_{RMS} I_{RMS} (\sin \phi + \sin(2(\omega t + \theta) - \phi))$$

The instantaneous reactive power is integrated in the reactive energy registers. Over time this removes the double mains frequency component $sin(2(\omega t+\theta)-\phi)$ to provide the average reactive power information

$$Q = \frac{1}{T} \int_0^T q(t) dt$$

 $Q = V_{RMS} I_{RMS} \sin \phi$

where Q is the average reactive power.

Linearity

The SA9904B is a CMOS integrated circuit, which performs power/energy calculations across a dynamic range of 500:1 to an accuracy that exceeds the IEC62053.

Analog Inputs

The input circuitry of the current and voltage sensor inputs is illustrated in Figure 6. These inputs are protected against electrostatic discharge through clamping diodes. The feedback loops from the outputs of the amplifiers A_I and A_V generate virtual short circuits between IIP and IIN as well as IVP and AGND. The current sense inputs (IIP and IIN) are identical and balanced. The AD converters convert the signals on the voltage and current sense inputs to a digital format for further processing. All internal offsets are eliminated through the use of various cancellation techniques.

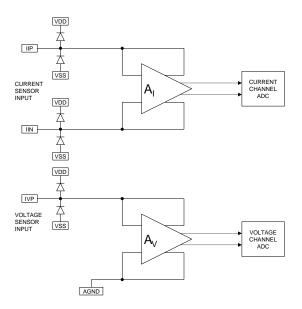


Figure 6: Analog input configuration

Power-On Reset

The SA9904B has a power-on reset circuitry that activates whenever the voltage between V_{DD} and V_{SS} is less than 3.6V \pm 8%.

Power Consumption

The power consumption of the SA9904B integrated circuit is less than 50mW.

INPUT SIGNALS Voltage Reference (VREF)

A bias resistor of $47k\Omega$ sets optimum bias and reference conditions on chip.

Current Sense Inputs (IIP1/IIN1, IIP2/IIN2, IIP3/IIN3)

Figure 7 shows the typical connections for the current sensor input for one channel. The circuit has to be repeated for the other two channels. At maximum rated mains current (I_{MAX}) the resistor values should be selected for input currents of 16µA_{RMS}. The current sense inputs saturate at an input current of ±17.6µA_{RMS} (±25µA_{PEAK}), so this allows about 10% headroom until saturation occurs. The resistors RA and RB form the current transformers termination resistor. The reference level is connected in the centre of the termination resistor to achieve purely differential input currents. The voltage drop across the termination resistors at maximum rated mains current (I_{MAX}) should be in the order of 100mV_{RMS}. The termination resistance should also be significantly smaller than the DC resistance of the current transformers secondary winding.

The resistors R1 to R4 define the current flowing into the device. For best performance the SA9904B requires antialias filters on the current sense inputs. These filters are realized by means of the capacitors C1 and C2. The typical cut-off frequency of these filters should be between 10kHz and 20kHz. The optimum input network is achieved by setting the input resistors equal, i.e. setting R1 = R2 = R3 = R4 = Rc. This sets the equivalent resistance associated with each capacitor to Rc/2.

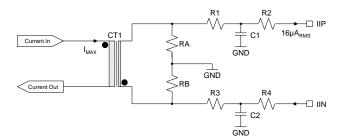


Figure 7: Current sense input configuration

Voltage Sense Inputs (IVP1, IVP2, IVP3)

Figure 8 shows the voltage sense input configuration for one channel. The circuit is identical for the other two channels. The voltage sense input saturates at an input current of $\pm 17.6 \mu A_{RMS} (\pm 25 \mu A_{PEAK})$. The current into the voltage sense input should therefore be set to $14 \mu A_{RMS}$ at nominal mains voltage (V_{NOM}) to allow for a mains voltage variation of up to $\pm 15\%$ and $\pm 50\%$ without saturating the voltage sense input.

For best performance the SA9904B also requires an antialias filter on the voltage sense inputs. Referring to Figure 8, the capacitor C1 is used to both implement the anti-alias filter as well as compensating for any phase shift caused by the current transformer. The resistor R4 defines the input current into the device. The optimum input network is achieved by setting R4 in the order of $100k\Omega$. If R4 is made too large the capacitor C1 will be very small and the accuracy of the phase compensation could be affected by stray capacitances.

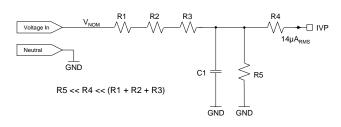


Figure 8: Voltage sense input configuration

Serial Clock (SCK)

The SCK pin is used to synchronize data interchange between the microcontroller and the SA9904B. The clock signal on this pin is generated by the microcontroller and determines the data transfer rate of the DO and DI pins.

Serial Data In (DI)

The DI pin is the serial data input pin for the SA9904B. Data will be input at a rate determined by the Serial Clock (SCK). Data will be strobed by the SA9904B on the rising edge of SCK only during an active chip select (CS).

Chip Select (CS)

The CS input is used to address the SA9904B. A high level on this pin enables the SA9904B to initiate data exchange.

OUTPUT SIGNALS Serial Data Out (DO)

The DO pin is the serial data output pin for the SA9904B. The Serial Clock (SCK) determines the data output rate. Data is only transferred out on the rising edge of SCK during active chip select (CS). This output is tri-state when CS is inactive (low). It is recommended to use an external pull-up or pulldown resistor on DO to ensure its state is always valid.

Mains Voltage Zero Crossover (F50)

The F50 output generates a signal, which follows the mains voltage zero crossings as shown in Figure 9. This output generates a pulse on the rising edge of the mains voltage zero crossing point. The pulse width is between 1ms and 2ms. Internal logic ensures that this signal is generated from a valid phase. Should all three phases be missing but power still applied to the SA9904B this output will generate a constant 54Hz signal. The microcontroller can use this signal to extract the mains timing or synchronize to the mains voltage.

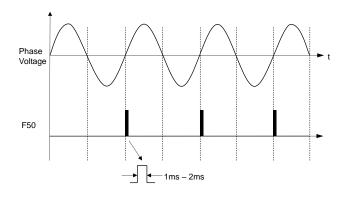


Figure 9: Mains voltage zero crossover

SPI INTERFACE Description

A serial peripheral interface bus (SPI) is a synchronous bus used for data transfers between a microcontroller and the SA9904B. The pins DO (Serial Data Out), DI (Serial Data In), CS (Chip Select), and SCK (Serial Clock) are used in the bus implementation. The SA9904B is the slave device with the microcontroller being the bus master. The CS input initiates and terminates data transfers. A SCK signal (generated by the microcontroller) strobes data between the microcontroller and the SA9904B. The DI and DO pins are the serial data input and output pins for the SA9904B respectively.

Register Access

Table 1 lists the various register addresses. The SA9904B contains nine 24 bit registers representing the active energy, reactive energy and the mains voltage for each phase. A tenth 24 bit register represents the mains frequency for any valid phase. The frequency register has been mapped to three addresses any of the three can be used to access it.

ID	Register		Header			Address Bits				
	Negister	E	Bits		5	4	3	2	1	0
1	Active energy, Channel 1	1	1	0	Х	Х	0	0	0	0
2	Reactive energy, Channel 1	1	1	0	Х	Х	0	0	0	1
3	Voltage, Channel 1	1	1	0	Х	Х	0	0	1	0
4	Frequency		1	0	Х	Х	0	0	1	1
5	Active energy, Channel 2	1	1	0	Х	Х	0	1	0	0
6	Reactive energy, Channel 2		1	0	Х	Х	0	1	0	1
7	Voltage, Channel 2	1	1	0	Х	Х	0	1	1	0
8	Frequency	1	1	0	Х	Х	0	1	1	1
9	Active energy, Channel 3	1	1	0	Х	Х	1	0	0	0
10	Reactive energy, Channel 3	1	1	0	Х	Х	1	0	0	1
11	Voltage, Channel 3	1	1	0	Х	Х	1	0	1	0
12	Frequency	1	1	0	Х	Х	1	0	1	1

The header bits 110 (0x06) form the read command must precede the 6 bit address of the register being accessed. When CS is high, data on the DI pin is clocked into the SA9904B on the rising edge of SCK. Figure 11 shows the data clocked into DI comprising of:

1 1 0 A5 A4 A3 A2 A1 A0

Address locations A5 and A4 are included for compatibility with future developments. Their state is ignored at present but it is best to set them to zero. The 9 bits needed for register addressing can be padded with leading zeros when the microcontroller requires an 8 bit SPI word length. The following sequence is valid:

0 0 0 0 0 0 0 1 1 0 A5 A4 A3 A2 A1 A0



Registers may be read individually and in any order. After a register has been read, the contents of the next register will be shifted out on the DO pin with every SCK clock cycle. This allows multiple subsequent registers to be read. Data output on DO will continue until CS is inactive. The DO pin is tri-state when CS is inactive, allowing multiple SPI devices to be connected to the bus. The content of each register consists of 24 bits of data. The most significant bit is shifted out first.

Data Format

Figure 11 shows the SPI waveforms and Figure 10 and Table 2 the timing information. After the least significant digit of the address has been entered on the rising edge of SCK, the output DO goes low. Each subsequent rising edge transition on the SCK pin will validate the next data bit on the DO pin. For best reliability of the SPI interface it is recommended to change CS and DI together with the falling edge of SCK and strobe DO on the falling edge of SCK as well, as shown in Figure 11.

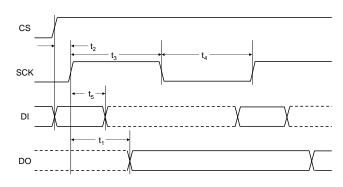
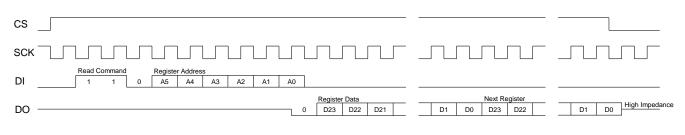


Figure 10: SPI waveform timing diagram

Parameter	Description	Min	Max
t1	SCK rising edge to DO valid	625ns	1.16µs
t2	Setup time for DI and CS before rising edge of SCK	20ns	
t3	SCK minimum high time	625ns	
t4	SCK minimum low time	625ns	
t5	Hold time for DI and CS after rising edge of SCK	625ns	





REGISTER DESCRIPTION

Active and Reactive Registers

The active and reactive energy measured on each channel of the SA9904B is accumulated in 6 distinct registers. Each channel has its own active and reactive energy register. These registers are 24 bit up/down counters, that increment or decrement at a rate of 320000 counts per second at rated conditions (nominal mains voltage V_{NOM} and maximum rated mains current I_{MAX}). The register values will increment for positive energy flow and decrement for negative energy flow.

The active and reactive registers are not reset after access, so in order to determine the correct register value the previous value read must be subtracted from the current reading. The data read from the registers represents the active or reactive power integrated over time. The increase or decrease between readings represents the measured energy consumption since the previous register access. At rated conditions, the active and reactive registers will wrap around every 52 seconds. The microcontroller software needs to take this condition into account when calculating the difference between register values. The register difference is always computed correctly if 24 bit arithmetic is used, regardless if a wrap-around has occurred or not. If the controller software uses 32 bit arithmetic, the 24 bit register readings should be sign extended to 32 bits. This ensures that the difference is computed correctly even if a register wrap-around has occurred.

The active and reactive energy measured per register count can be calculated by applying the following formula:

 $Energy \ per \ count = \frac{V_{NOM} \times I_{MAX}}{320000}$

where

 V_{NOM} is the nominal rated mains voltage of meter and I_{MAX} is the maximum rated mains current of meter. The result is watt seconds or var seconds.

The active and reactive power measured on one channel by the SA9904B is calculated as follows:

$$Power = \frac{V_{NOM} \times I_{MAX} \times N}{320000 \times T_{INT}}$$

where

 ${\it N}$ is the difference in register values between successive register reads and

 T_{INT} is the time difference between successive register reads.



Voltage Registers

The three voltage registers contain the RMS voltage measured on each channel of the device. This measurement is a true RMS measurement which is accurate to 1% for a range of 50% to 115% of the rated mains voltage. The RMS mains voltage measured by the SA9904B is calculated as follows:

 $RMS Mains Voltage = \frac{V_{NOM} \times VREG}{700}$

where

VREG is the voltage register value.

The value of the voltage register will default to zero when the RMS measurement produces a register value of less than 64. This occurs at a mains voltage of just below 10% V_{NOM} . The settling time of the RMS measurement algorithm is in the order of 200 mains cycles.

Frequency register

The single frequency register contains the measured mains frequency information for a valid phase. Internal logic ensures that the frequency information is generated from the same phase being used for the F50 output. Only bits D0 to D9 are used for the mains frequency calculation result, however the remaining bits must still be clocked out as additional information can be derived from these data bits as indicated in Table 3.

Table 3: Frequency register bits allocation

Bits	Description							
D9D0	These bits represent a value that is used in the frequency calculation							
D17D10	Unused	Unused, default value is zero						
		Missing phase. These bits indicate which phase is missing during a lost phase condition.						
D20, D19,	D20	D19	D18	Status				
D18	Х	Х	1	Phase 1 is missing				
	Х	1	Х	Phase 2 is missing				
	1	Х	Х	Phase 3 is missing				
	The pl from th			atus can be ascertained				
	D22	D21	Statu	JS				
D22, D21	0	0	No phase error					
	1	0	Phase sequence error					
	Х	1	Missing Phase					
D23	Voltage zero crossover bit. This bit changes state with each rising edge of the mains voltage.							

The mains frequency measured by the SA9904B is calculated as follows:

 $Mains \ Frequency \ = \ \frac{F_{CRYSTAL} \times FREG}{256}$

where

FREG is the frequency register value in bits D9 to D0 and $F_{CRYSTAL}$ is the frequency of the external crystal.

OSCILLATOR

The SA9904B contains a crystal oscillator driver circuit requiring only an external crystal to be connected between OSC1 and OSC2. All other components are integrated on the device. The recommended crystal is a TV colour burst crystal (3.5795MHz).

TYPICAL APPLICATION

The following description outlines the basic process required to design a typical three phase energy meter using the SA9904B. The meter is a 3-phase 4-wire meter capable of measuring 3x220V/60A/50Hz with a precision better than Class 1 on active energy and Class 2 on reactive energy.

The most important external circuits required for the SA9904B are the current input networks, the voltage input networks as well as the bias resistor. All resistors should be 1% metal film resistors of the same type to minimize temperature effects. Calibration of a microcontroller based meter is typically done in software so the external circuits do not require calibration mechanisms.

Bias Resistor

A bias resistor of R34 = $47k\Omega$ sets optimum bias and reference currents on chip.

Current Input Networks

Three current transformers are used to measure the three line currents. The output of each current transformer is terminated with a low impedance resistor split into two equal parts to obtain purely differential current input signals. The voltage across the termination resistors is converted to the required differential input currents through the current input resistors. Anti-alias filters are incorporated on these input resistors to filter any high frequency signal components that could affect the performance of the SA9904B.

The voltage drop across the current transformer termination resistors at maximum rated current should be in the order of $100mV_{RMS}$. The current transformers have a low phase shift and a turns ratio of 1:2500. The value of the termination resistors R1, R2 is therefore

$$R1 = R2 = 100mV \times \frac{N_{CT}}{I_{MAX}} \times \frac{1}{2} \approx 2\Omega = R_B$$

where N_{CT} is the current transformer ratio (2500) and I_{MAX} is the maximum input current (60A).

The four current input resistors (R3, R4, R5, R6) should be of equal size to optimize the input networks low pass filtering characteristics, so the values can be calculated as follows:

$$R3 = R4 = R5 = R6 = \frac{I_{MAX}}{N_{CT}} \times \frac{R_B}{2 \times 16\mu A} = 1.5k\Omega = R_C$$

For optimum performance the cut-off frequency of the antialias filter should be between 10kHz and 20kHz. The equivalent resistance associated with each capacitor is $R_C/2$ so the capacitor values should be in the order of

$$C1 = C2 = \frac{1}{\pi f_{CI}R_c} = \frac{1}{\pi \times 10kHz \times 1.5k\Omega} \approx 22nF = C_c$$

where f_{CI} is the cut-off frequency of the anti-alias filter of the current input network.

The current input networks for channel 2 and channel 3 are identical.

Voltage Input Networks

The voltage sense inputs require an input current of $14\mu A_{RMS}$ at V_{NOM} . The mains voltage is divided by means of a voltage divider to a lower voltage that is converted to the required input current by means of the input resistor. Once again an anti-alias filter is required to remove any high frequency signals that could affect the performance of the SA9904B. The phase shift of the current transformers is compensated by means of this anti-alias filter as well, by purposefully increasing the cut-off frequency.

The input resistor R22 sets the current input into the device. This resistor should not be too large else the capacitor for the anti-alias filter will be quite small which could cause inaccurate phase shift due to parasitic capacitances. Therefore R22 = $100k\Omega$ is chosen. R23 should be significantly smaller than R22, but not too small in order to limit the power dissipation of the voltage input network. Hence R23 = $4.3k\Omega$ is chosen. Now let R_A = R19 + R20 + R21 and

$$R_A = R23 \times \left(\frac{220V}{1.4V} - 1\right) \approx 671k\Omega$$

so choose R19 = R20 = R21 = $220k\Omega$.

The cut-off frequency of the anti-alias filter is adjusted so that the phase shift of the voltage input network is identical to the sum of the phase shifts of the current transformer and the current input network. The phase shift of the current input network is

 $\phi_{II} = -\tan^{-1}(\pi R_C C_C \times 50 Hz) \approx -0.297^{\circ}$

The phase shift required on the voltage input network is therefore

 $\phi_{IV} = \phi_{II} - \phi_{CT} = -0.297^{\circ} + 0.09^{\circ} = -0.207^{\circ}$

where ϕ_{CT} is the phase shift of the current transformer which is typically about 0.09 degrees for a good quality current transformer. Neglecting R19, R20, R21 and R22 because all these resistors are significantly larger than R23 the capacitance required to achieve the -0.207 degree phase shift is

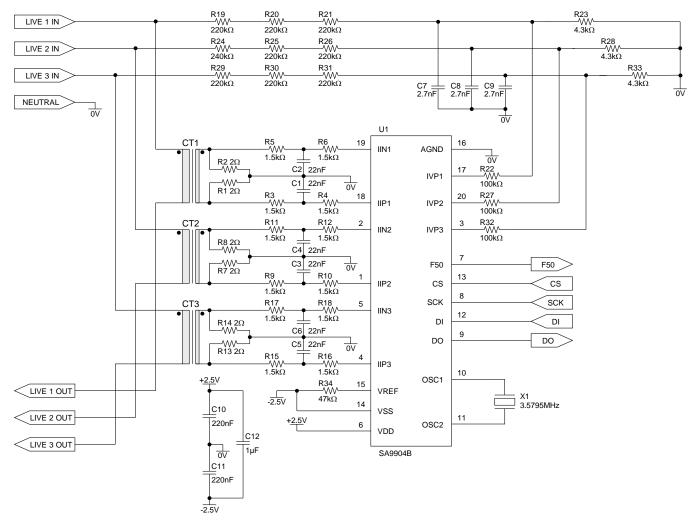
$$C7 = \frac{|\tan \phi_{IV}|}{2\pi \times R23 \times 50 Hz} \approx 2.7 nF$$

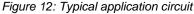
resulting in a cut-off frequency of

$$f_{CV} = \frac{1}{2\pi \times R23 \times C7} = 13.7 kHz$$

The value of the cut-off frequency of the voltage input network is less critical than that of the current input network because the dynamic range of the voltage input is small. A cut-off frequency between 10kHz and 25kHz is acceptable.

The voltage input networks for channel 2 and channel 3 are identical







T 1 1 0		<i></i>
Table 4: Component	list for typical	application

Symbol	Description
U1	Energy metering device, SA9904BSAR
R1, R2	Resistor, 2 Ω , 1%, metal film
R3, R4 ¹ , R5, R6 ¹	Resistor, 1.5k Ω , 1%, metal film
R7, R8	Resistor, 2 Ω , 1%, metal film
R9, R10 ¹ , R11, R12 ¹	Resistor, 1.5k Ω , 1%, metal film
R13, R14	Resistor, 2 Ω , 1%, metal film
R15, R16 ¹ , R17, R18 ¹	Resistor, 1.5k Ω , 1%, metal film
R19, R24, R29	Resistor, 220k Ω , 1%, metal film
R20, R25, R30	Resistor, 220k Ω , 1%, metal film
R21, R26, R31	Resistor, 220k Ω , 1%, metal film
R22 ¹ , R27 ¹ , R32 ¹	Resistor, 100k Ω , 1%, metal film
R23, R28, R33	Resistor, 4.3k Ω , 1%, metal film
R34 ¹	Resistor, $47k\Omega$, 1%, metal film
C1, C2	Capacitor, 22nF, ceramic
C3, C4	Capacitor, 22nF, ceramic
C5, C6	Capacitor, 22nF, ceramic
C7, C8, C9	Capacitor, 2.7nF, ceramic
C10 ² , C11 ²	Capacitor, 220nF, ceramic
C12 ²	Capacitor, 1µF, ceramic
X1	Crystal, 3.5795MHz

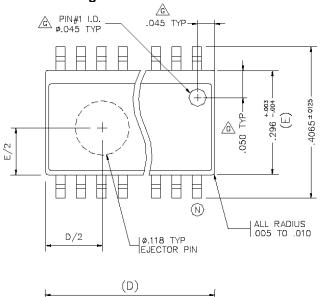
Note 1: Resistors R4, R6, R10, R12, R16, R18, R22, R27, R32 and R34 must be positioned as close as possible to the respective device pins

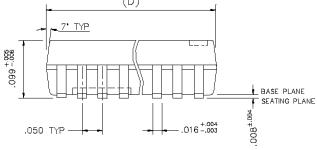
Note 2: Capacitors C10, C11 and C12 must be positioned as close as possible to the V_{DD} and V_{SS} power supply pins



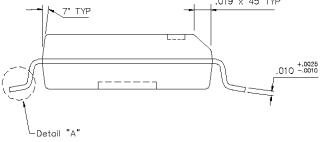
PACKAGE DIMENSIONS

SOIC20 Package





D VARIATIONS Ν MIN NOM MAX 0"-_ 8 .405 16 .398 .412 \land 18 .449 .456 .463 20 .503 .510 .496 .033 ±.017 24 .599 .606 .613 28 .697 .704 .711 Detail "A" .019 x 45 TYP



Dimensions are shown in inches



NOTES



DISCLAIMER

The information contained in this document is confidential and proprietary to Integrated Circuit Design Centre (Pty) Ltd ("ICDC"), a division of South African Micro-Electronic Systems (Pty) Ltd ("SAMES"), and may not be copied or disclosed to a third party, in whole or in part, without the express written consent of ICDC. The information contained herein is current as of the date of publication; however, delivery of this document shall not under any circumstances create any implication that the information contained herein is correct as of any time subsequent to such date. ICDC does not undertake to inform any recipient of this document of any changes in the information contained herein, and ICDC expressly reserves the right to make changes in such information, without notification, even if such changes would render information contained herein inaccurate or incomplete. ICDC makes no representation or warranty that any circuit designed by reference to the information contained herein, will function without errors and as intended by the designer.

Any sales or technical questions may be sent to our support e-mail address: support@sames.co.za

For the latest updates on datasheets, please visit our web site: http://www.sames.co.za.

INTEGRATED CIRCUIT DESIGN CENTRE (PTY) LTD a division of SOUTH AFRICAN MICRO-ELECTRONIC SYSTEMS (PTY) LTD

Tel: 012 333 6021 Tel Int: 00 27 12 333 6021 Fax: 012 333 6393 Fax Int: 00 27 12 333 6393

PO BOX 15888 LYNN EAST 0039 REPUBLIC OF SOUTH AFRICA UNIT 4, PERSEQUOR CLOSE 49 DE HAVILLAND CRESCENT PERSEQUOR TECHNOPARK LYNNWOOD, PRETORIA REPUBLIC OF SOUTH AFRICA