1Gbit - 64M x 16 GL-S MirrorBit© Eclipse™ Flash Memory

Features

- Tin-lead ball metallurgy

- 65 nm MirrorBit Eclipse technology

- Single supply (V_{CC}) for read / program / erase (2.7V to 3.6V)

- Versatile I/O Feature

  - Wide I/O voltage range (V_{IO}): 1.65V to V_{CC}

- Asynchronous 32-byte page read

- 512-byte programming buffer

  - Programming in page multiples, up to a maximum of 512 bytes

- Single word and multiple program on same

- word options

- Sector Erase

  - Uniform 128-kbyte sectors

- Suspend and resume commands for program and erase operations

- Status register, data polling, and ready/busy pin methods to determine device status

- Advanced Sector Protection (ASP)

  - Volatile and non-volatile protection methods for each sector

- Separate 1024-byte One Time Program (OTP) array with two lockable regions

- Common Flash Interface (CFI) parameter table

- 100,000 erase cycles for any sector typical

- 20-year data retention typical

Options	Marking
• Configuration	
▪ 64M x 16	
• FBGA package (Sn63 Pb37 solder)	BG
▪ 64-ball FBGA (9mm x 9mm)	D
• Operating temperature	
▪ Industrial (-40°C ≤ T_C ≤ +85°C)	IT

Table 1: Performance Summary

Density	Voltage Range	Random Access Time (t_{ACC})	Page Access Time (t_{PACC})	CE# Access Time (t_{CE})	OE# Access Time (t_{OE})
1 Gb	Full $V_{CC} = V_{IO}$	100	15	100	25
	VersatileIO V_{IO}	110	25	110	35
Typical Program and Erase Rates					
Buffer Programming (512 bytes)		1.5 MB/s			
Sector Erase (128 kbytes)		477 kB/s			
Maximum Current Consumption					
Active Read at 5 MHz, 30 pF		60 mA			
Program		100 mA			
Erase		100 mA			
Standby		100 µA			

Contents

Advanced information. Subject to change without notice.

1   Product Overview

The MYX29GL01GS11DPIV2 has a 16-bit (word) wide data bus and uses only word boundary addresses. All read accesses provide 16 bits of data on each bus transfer cycle. All writes take 16 bits of data from each bus transfer cycle.

Figure 1: Block Diagram
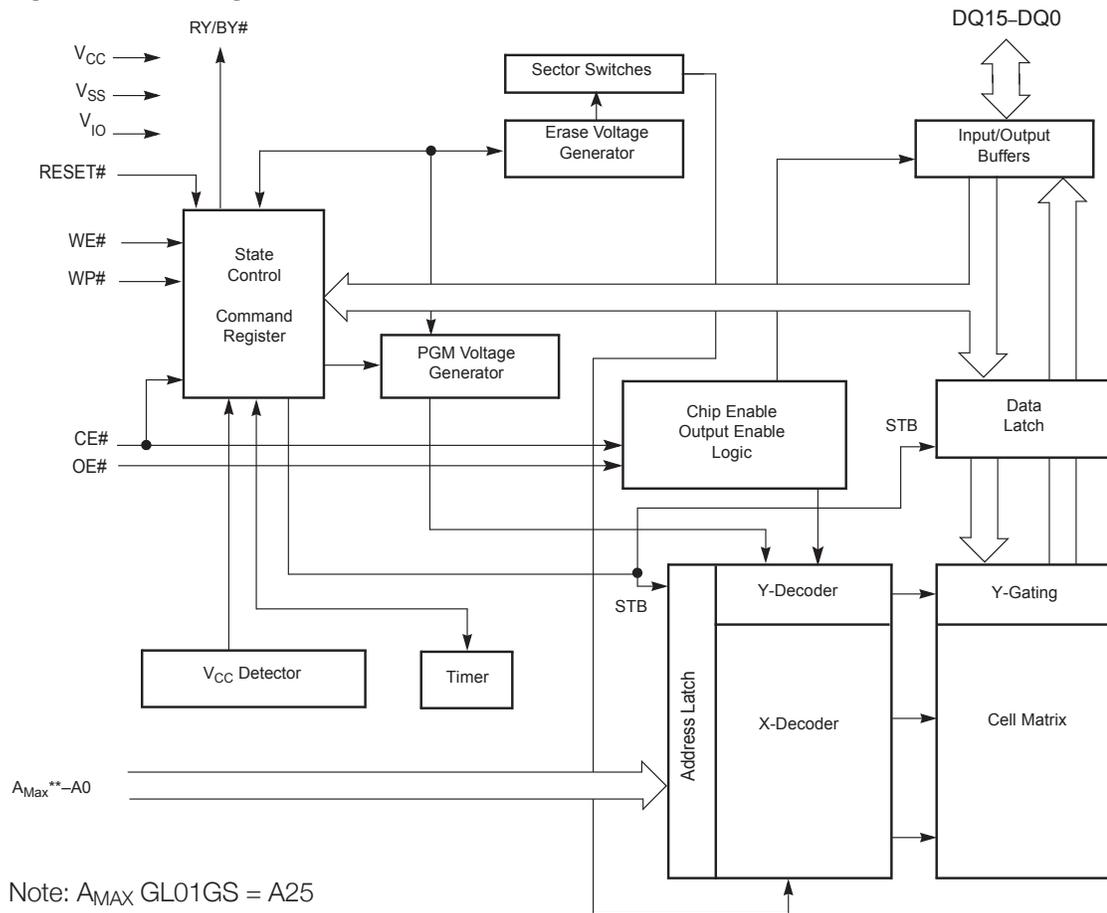
Note: A_{MAX} GL01GS = A25

The MYX29GL01GS11DPIV2 combines the best features of eXecute In Place (XIP) and Data Storage flash memories. This MYX29GL01GS11DPIV2 has the fast random access of XIP flash along with the high density and fast program speed of Data Storage flash.

Read access to any random location takes 90 ns to 120 ns depending on device density and I/O power supply voltage. Each random (initial) access reads an entire 32-byte aligned group of data called a Page. Other words within the same Page may be read by changing only the low order 4 bits of word address. Each access within the same Page takes 15 ns to 30 ns. This is called Page Mode read. Changing any of the higher word address bits will select a different Page and begin a new initial access. All read accesses are asynchronous.

Software Interface

2   Address Space Maps

There are several separate address spaces that may appear within the address range of the flash memory device. One address space is visible (entered) at any given time.

- Flash Memory Array: the main non-volatile memory array used for storage of data that may be randomly accessed by asynchronous read operations.

- ID/CFI: a memory array used for factory programmed device characteristics information. This area contains the Device Identification (ID) and Common Flash Interface (CFI) information tables.

- Secure Silicon Region (SSR): a One Time Programmable (OTP) non-volatile memory array used for factory programmed permanent data, and customer programmable permanent data.

- Lock Register: an OTP non-volatile word used to configure the ASP features and lock the SSR.

- Persistent Protection Bits (PPB): a non-volatile flash memory array with one bit for each Sector. When programmed, each bit protects the related Sector from erasure and programming.

- PPB Lock: a volatile register bit used to enable or disable programming and erasure of the PPB bits.

- Password: an OTP non-volatile array used to store a 64-bit password used to enable changing the state of the PPB Lock Bit when using Password Mode sector protection.

- Dynamic Protection Bits (DYB): a volatile array with one bit for each Sector. When set, each bit protects the related Sector from erasure and programming.

- Status Register: a volatile register used to display Embedded Algorithm status.

- Data Polling Status: a volatile register used as an alternate, legacy software compatible, way to display Embedded Algorithm status.

The main Flash Memory Array is the primary and default address space but, it may be overlaid by one other address space, at any one time. Each alternate address space is called an Address Space Overlay (ASO).

Each ASO replaces (overlays) the entire flash device address range. Any address range not defined by a particular ASO address map, is reserved for future use. All read accesses outside of an ASO address map returns non-valid (undefined) data. The locations will display actively driven data but the meaning of whatever 1's or 0's appear are not defined.

There are four device operating modes that determine what appears in the flash device address space at any given time:

- Read Mode
- Data Polling Mode
- Status Register (SR) Mode
- Address Space Overlay (ASO) Mode

In Read Mode the entire Flash Memory Array may be directly read by the host system memory controller. The memory device Embedded Algorithm Controller (EAC), puts the device in Read mode during Power-on, after a Hardware Reset, after a Command Reset, or after an Embedded Algorithm (EA) is suspended. Read accesses and command writes are accepted in read mode. A subset of commands are accepted in read mode when an EA is suspended.

While in any mode, the Status Register read command may be issued to cause the Status Register ASO to appear at every word address in the device address space. In this Status Register ASO Mode, the device interface waits for a read access and, any write access is ignored. The next read access to the device accesses the content of the status register, exits the Status Register ASO, and returns to the previous (calling) mode in which the Status Register read command was received.

In EA mode the EAC is performing an Embedded Algorithm, such as programming or erasing a non-volatile memory array. While in EA mode, none of the main Flash Memory Array is readable because the entire flash device address space is replaced by the Data Polling Status ASO. Data Polling Status will appear at every word location in the device address space.

While in EA mode, only a Program / Erase suspend command or the Status Register Read command will be accepted. All other commands are ignored. Thus, no other ASO may be entered from the EA mode.

When an Embedded Algorithm is suspended, the Data Polling ASO is visible until the device has suspended the EA. When the EA is suspended the Data Polling ASO is exited and Flash Array data is available. The Data Polling ASO is reentered when the suspended EA is resumed, until the EA is again suspended or finished. When an Embedded Algorithm is completed, the Data Polling ASO is exited and the device goes to the previous (calling) mode (from which the Embedded Algorithm was started).

In ASO mode, one of the remaining overlay address spaces is entered (overlaid on the main Flash Array address map). Only one ASO may be entered at any one time. Commands to the device affect the currently entered ASO. Only certain commands are valid for each ASO. These are listed in Table 7: Command Definitions (page 28), in each ASO related section of the table.

The following ASOs have non-volatile data that may be programmed to change 1's to 0's:

- Secure Silicon Region
- Lock Register
- Persistent Protection Bits (PPB)
- Password
- Only the PPB ASO has non-volatile data that may be erased to change 0's to 1's

When a program or erase command is issued while one of the non-volatile ASOs is entered, the EA operates on the ASO. The ASO is not readable while the EA is active. When the EA is completed the ASO remains entered and is again readable. Suspend and Resume commands are ignored during an EA operating on any of these ASOs.

2.1 Flash Memory Array

The MYX29GL01GS11DPIV2 family has an uniform sector architecture with a sector size of 128 kB.

Table 3: MYX29GL01GS11DPIV2 Sector and Memory Address Map

Sector Size (kbyte)	Sector Count	Sector Range	Address Range (16-Bit)	Notes
128	1024	SA00	0000000h-000FFFFh	Sector Starting Address
		:	:	–
		SA1023	3FF0000h-3FFFFFFh	Sector Ending Address

Note: This table has been condensed to show sector related information for an entire device on a single page Sectors and their address ranges that are not explicitly listed (such as SA001-SA510) have sectors starting and ending addresses that form the same pattern as all other sectors of that size. For example, all 128 kB sectors have the pattern XXX0000h-XXXFFFFh.

2.2 Device ID and CFI (ID-CFI) ASO

There are two traditional methods for systems to identify the type of flash memory installed in the system. One has traditionally been called Autoselect and is now referred to as Device Identification (ID). The other method is called Common Flash Interface (CFI).

For ID, a command is used to enable an address space overlay where up to 16 word locations can be read to get JEDEC manufacturer identification (ID), device ID, and some configuration and protection status information from the flash memory. The system can use the manufacturer and device IDs to select the appropriate driver software to use with the flash device.

CFI also uses a command to enable an address space overlay where an extendable table of standard information about how the flash memory is organized and operates can be read. With this method the driver software does not have to be written with the specifics of each possible memory device in mind. Instead the driver software is written in a more general way to handle many different devices but adjusts the driver behavior based on the information in the CFI table.

Traditionally these two address spaces have used separate commands and were separate overlays. However, the mapping of these two address spaces are non-overlapping and so can be combined in to a single address space and appear together in a single overlay. Either of the traditional commands used to access (enter) the Autoselect (ID) or CFI overlay will cause the now combined ID-CFI address map to appear.

2.2.1 Device ID

The Joint Electron Device Engineering Council (JEDEC) standard JEP106T defines the manufacturer ID for a compliant memory. Common industry usage defined a method and format for reading the manufacturer ID and a device specific ID from a memory device. The manufacturer and device ID information is primarily intended for programming equipment to automatically match a device with the corresponding programming algorithm. Spansion has added additional fields within this 32-byte address space.

2.2.2 Common Flash Memory Interface

The JEDEC Common Flash Interface (CFI) specification (JESD68.01) defines a standardized data structure that may be read from a flash memory device, which allows vendor-specified software algorithms to be used for entire families of devices. The data structure contains information for system configuration such as various electrical and timing parameters, and special functions supported by the device. Software support can then be device-independent, Device ID-independent, and forward-and-backward-compatible for entire Flash device families.

2.3 Status Register ASO

The Status Register ASO contains a single word of registered volatile status for Embedded Algorithms. When the Status Register read command is issued, the current status is captured (by the rising edge of WE#) into the register and the ASO is entered. The Status Register content appears on all word locations. The first read access exits the Status Register ASO (with the rising edge of CE# or OE#) and returns to the address space map in use when the Status Register read command was issued. Write commands will not exit the Status Register ASO state.

2.4 Data Polling Status ASO

The Data Polling Status ASO contains a single word of volatile memory indicating the progress of an EA. The Data Polling Status ASO is entered immediately following the last write cycle of any command sequence that initiates an EA. Commands that initiate an EA are:

- Word Program
- Program Buffer to Flash
- Chip Erase
- Sector Erase
- Erase Resume / Program Resume
- Program Resume Enhanced Method
- Blank Check
- Lock Register Program
- Password Program
- PPB Program
- All PPB Erase

The Data Polling Status word appears at all word locations in the device address space. When an EA is completed the Data Polling Status ASO is exited and the device address space returns to the address map mode where the EA was started.

2.5 Secure Silicon Region ASO

The Secure Silicon Region (SSR) provides an extra flash memory area that can be programmed once and permanently protected from further changes i. e. it is a One Time Program (OTP) area. The SSR is 1024 bytes in length. It consists of 512 bytes for Factory Locked Secure Silicon Region and 512 bytes for Customer Locked Secure Silicon Region.

2.6 Sector Protection Control

2.6.1 Lock Register ASO

The Lock register ASO contains a single word of OTP memory. When the ASO is entered the Lock Register appears at all word locations in the device address space. However, it is recommended to read or program the Lock Register only at location 0 of the device address space for future compatibility.

2.6.2 Persistent Protection Bits (PPB) ASO

The PPB ASO contains one bit of a Flash Memory Array for each Sector in the device. When the PPB ASO is entered, the PPB bit for a sector appears in the Least Significant Bit (LSB) of each address in the sector. Reading any address in a sector displays data where the LSB indicates the non-volatile protection status for that sector. However, it is recommended to read or program the PPB only at address 0 of the sector for future

compatibility. If the bit is 0 the sector is protected against programming and erase operations. If the bit is 1 the sector is not protected by the PPB. The sector may be protected by other features of ASP.

2.6.3 PPB LOCK ASO

The PPB Lock ASO contains a single bit of volatile memory. The bit controls whether the bits in the PPB ASO may be programmed or erased. If the bit is 0 the PPB ASO is protected against programming and erase operations. If the bit is 1 the PPB ASO is not protected. When the PPB Lock ASO is entered the PPB Lock bit appears in the Least Significant Bit (LSB) of each address in the device address space. However, it is recommended to read or program the PPB Lock only at address 0 of the device for future compatibility.

2.6.4 Password ASO

The Password ASO contains four words of OTP memory. When the ASO is entered the Password appears starting at address 0 in the device address space. All locations above the forth word are undefined.

2.6.5 Dynamic Protection Bits (DYB) ASO

The DYB ASO contains one bit of a volatile memory array for each Sector in the device. When the DYB ASO is entered, the DYB bit for a sector appears in the Least Significant Bit (LSB) of each address in the sector. Reading any address in a sector displays data where the LSB indicates the non-volatile protection status for that sector. However, it is recommended to read, set, or clear the DYB only at address 0 of the sector for future compatibility. If the bit is 0 the sector is protected against programming and erase operations. If the bit is 1 the sector is not protected by the DYB. The sector may be protected by other features of ASP.

3 Data Protection

The device offers several features to prevent malicious or accidental modification of any sector via hardware means.

3.1 Device Protection Methods

3.1.1 Power-Up Write Inhibit

RESET#, CE#, WE#, and, OE# are ignored during Power-On Reset (POR). During POR, the device can not be selected, will not accept commands on the rising edge of WE#, and does not drive outputs. The Host Interface Controller (HIC) and Embedded Algorithm Controller (EAC) are reset to their standby states, ready for reading array data, during POR. CE# or OE# must go to V_{IH} before the end of POR (t_{VCS}).

At the end of POR the device conditions are:

- all internal configuration information is loaded,

- the device is in read mode,

- the Status Register is at default value,

- all bits in the DYB ASO are set to un-protect all sectors,

- the Write Buffer is loaded with all 1's,

- the EAC is in the standby state.

3.1.2 Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the HIC does not accept any write cycles and the EAC resets. This protects data during V_{CC} power-up and power-down. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

3.2 Command Protection

Embedded Algorithms are initiated by writing command sequences into the EAC command memory. The command memory array is not readable by the host system and has no ASO. Each host interface write is a command or part of a command sequence to the device. The EAC examines the address and data in each write transfer to determine if the write is part of a legal command sequence. When a legal command sequence is complete the EAC will initiate the appropriate EA.

Writing incorrect address or data values, or writing them in an improper sequence, will generally result in the EAC returning to its Standby state. However, such an improper command sequence may place the device in an unknown state, in which case the system must write the reset command, or possibly provide a hardware reset by driving the RESET# signal Low, to return the EAC to its Standby state, ready for random read.

The address provided in each write may contain a bit pattern used to help identify the write as a command to the device. The upper portion of the address may also select the sector address on which the command operation is to be performed. The Sector Address (SA) includes AMAX through A16 flash address bits (system byte address signals amax through a17). A command bit pattern is located in A10 to A0 flash address bits (system byte address signals a11 through a1).

The data in each write may be: a bit pattern used to help identify the write as a command, a code that identifies the command operation to be performed, or supply information needed to perform the operation. See Table 7: Command Definitions (page 28) for a listing of all commands accepted by the device.

3.3 Secure Silicon Region (OTP)

The Secure Silicon Region (SSR) provides an extra flash memory area that can be programmed once and permanently protected from further changes i.e. it is a One Time Program (OTP) area. The SSR is 1024 bytes in length. It consists of 512 bytes for Factory Locked Secure Silicon Region and 512 bytes for Customer Locked Secure Silicon Region.

3.4 Sector Protection Methods

3.4.1 Write Protect Signal

If WP# = V_{IL}, the lowest or highest address sector is protected from program or erase operations independent of any other ASP configuration. Whether it is the lowest or highest sector depends on the device ordering option (model) selected. If WP# = V_{IH}, the lowest or highest address sector is not protected by the WP# signal but it may be protected by other aspects of ASP configuration. WP# has an internal pull-up; when unconnected, WP# is at V_{IH}.

3.4.2 ASP

Advanced Sector Protection (ASP) is a set of independent hardware and software methods used to disable or enable programming or erase operations, individually, in any or all sectors. This section describes the various methods of protecting data stored in the memory array. An overview of these methods is shown in Figure 2: Advanced Sector Protection Overview (page 13).

*Advanced information. Subject to change without notice.

Figure 2: Advanced Sector Protection Overview

1. Bit is volatile, and defaults to "1" on reset (to "0" if in Password Mode).
2. Programming to "0" locks all PPBs to their current state.
3. Once programmed to "0", requires hardware reset to unlock or application of the password.

4. N = Highest Address Sector.

5. 0 = Sector Protected,
   1 = Sector Unprotected.
6. PPBs programmed individually, but cleared collectively

7. 0 = Sector Protected,
   1 = Sector Unprotected.
8. Protect effective only if corresponding PPB is "1" (unprotected).
9. Volatile Bits: defaults to user choice upon power-up (see ordering options).

Every main flash array sector has a non-volatile (PPB) and a volatile (DYB) protection bit associated with it. When either bit is 0, the sector is protected from program and erase operations.

he PPB bits are protected from program and erase when the PPB Lock bit is 0. There are two methods for managing the state of the PPB Lock bit, Persistent Protection and Password Protection.

3.4.3   Sector Protection States Summary

Each sector can be in one of the following protection states:

- Unlocked – The sector is unprotected and protection can be changed by a simple command. The protection state defaults to unprotected after a power cycle or hardware reset.
- Dynamically Locked – A sector is protected and protection can be changed by a simple command. The protection state is not saved across a power cycle or hardware reset.
- Persistently Locked – A sector is protected and protection can only be changed if the PPB Lock Bit is set to
    1. The protection state is non-volatile and saved across a power cycle or hardware reset. Changing the protection state requires programming or erase of the PPB bits.

Table 4: Sector Protection States

Protection Bit Values			Sector State
PPB Lock	PPB	DYB	
1	1	1	Unprotected - PPB and DYB are changeable
1	1	0	Protected - PPB and DYB are changeable
1	0	1	Protected - PPB and DYB are changeable
1	0	0	Protected - PPB and DYB are changeable
0	1	1	Unprotected - PPB not changeable, DYB is changeable
0	1	0	Protected - PPB not changeable, DYB is changeable
0	0	1	Protected - PPB not changeable, DYB is changeable
0	0	0	Protected - PPB not changeable, DYB is changeable

3.4.4 Lock Register

The Lock Register holds the non-volatile OTP bits for controlling protection of the SSR, and determining the PPB Lock bit management method (protection mode).

Table 5: Lock Register

Bit	Default Value	Name
15-9	1	Reserved
8	0	Reserved
7	X	Reserved
6	1	SSR Region 1 (Customer) Lock Bit
5	1	Reserved
4	1	Reserved
3	1	Reserved
2	1	Password Protection Mode Lock Bit
1	1	Persistent Protection Mode Lock Bit
0	0	SSR Region 0 (Factory) Lock Bit

The Secure Silicon Region (SSR) protection bits must be used with caution, as once locked, there is no procedure available for unlocking the protected portion of the Secure Silicon Region and none of the bits in the protected Secure Silicon Region memory space can be modified in any way. Once the Secure Silicon Region area is protected, any further attempts to program in the area will fail with status indicating the area being programmed is protected. The Region 0 Indicator Bit is located in the Lock Register at bit location 0 and Region 1 in bit location 6.

As shipped from the factory, all devices default to the Persistent Protection method, with all sectors unprotected, when power is applied. The device programmer or host system can then choose which sector protection method to use. Programming either of the following two, one-time programmable, non-volatile bits, locks the part permanently in that mode:

- Persistent Protection Mode Lock Bit (DQ1)
- Password Protection Mode Lock Bit (DQ2)

If both lock bits are selected to be programmed at the same time, the operation will abort. Once the Password Mode Lock Bit is programmed, the Persistent Mode Lock Bit is permanently disabled and no changes to the protection scheme are allowed. Similarly, if the Persistent Mode Lock Bit is programmed, the Password Mode is permanently disabled.

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If the password mode is to be chosen, the password must be programmed prior to setting the corresponding lock register bit. Setting the Password Protection Mode Lock Bit is programmed, a power cycle, hardware reset, or PPB Lock Bit Set command is required to set the PPB Lock bit to 0 to protect the PPB array.

The programming time of the Lock Register is the same as the typical word programming time. During a Lock Register programming EA, Data polling Status DQ6 Toggle Bit I will toggle until the programming has completed. The system can also determine the status of the lock register programming by reading the Status Register. See Section 5.4.1: Status Register (page 25) for information on these status bits.

The user is not required to program DQ2 or DQ1, and DQ6 or DQ0 bits at the same time. This allows the user to lock the SSR before or after choosing the device protection scheme. When programming the Lock Bits, the Reserved Bits must be 1 (masked).

3.4.5 Persistent Protection Mode

The Persistent Protection method sets the PPB Lock to 1 during POR or Hardware Reset so that the PPB bits are unprotected by a device reset. There is a command to clear the PPB Lock bit to 0 to protect the PPB. There is no command in the Persistent Protection method to set the PPB Lock bit to 1 therefore the PPB Lock bit will remain at 0 until the next power-off or hardware reset.

3.4.6 Password Protection Mode

3.4.6.1 PPB Password Protection Mode

PPB Password Protection Mode allows an even higher level of security than the Persistent Sector Protection Mode, by requiring a 64-bit password for setting the PPB Lock. In addition to this password requirement, after power up and reset, the PPB Lock is cleared to 0 to ensure protection at power-up. Successful execution of the Password Unlock command by entering the entire password sets the PPB Lock to 1, allowing for sector PPB modifications.

Password Protection Notes:

- The Password Program Command is only capable of programming 0's.

- The password is all 1's when shipped from the OEM. It is located in its own memory space and is accessible through the use of the Password Program and Password Read commands.

- All 64-bit password combinations are valid as a password.

- Once the Password is programmed and verified, the Password Mode Locking Bit must be set in order to prevent reading or modification of the password.

- The Password Mode Lock Bit, once programmed, prevents reading the 64-bit password on the data bus and further password programming. All further program and read commands to the password region are disabled (data is read as 1's) and these commands are ignored. There is no means to verify what the

Advanced information. Subject to change without notice.

password is after the Password Protection Mode Lock Bit is programmed. Password verification is only allowed before selecting the Password Protection mode.

- The Password Mode Lock Bit is not erasable.

- The exact password must be entered in order for the unlocking function to occur.

- The addresses can be loaded in any order but all 4 words are required for a successful match to occur.

- The Sector Addresses and Word Line Addresses are compared while the password address/data are loaded. If the Sector Adddress don't match than the error will be reported at the end of that write cycle. The status register will return to the ready state with the Program Status Bit set to 1, Program Status Register Bit set to 1, and Write Buffer Abort Status Bit set to 1 indicating a failed programming operation. It is a failure to change the state of the PPB Lock bit because it is still protected by the lack of a valid password. The data polling status will remain active, with DQ7 set to the complement of the DQ7 bit in the last word of the password unlock command, and DQ6 toggling. RY/BY# will remain low.

- The specific address and data are compared after the Program Buffer To Flash command has been given. If they don't match to the internal set value than the status register will return to the ready state with the Program Status Bit set to 1 and Program Status Register Bit set to 1 indicating a failed programming operation. It is a failure to change the state of the PPB Lock bit because it is still protected by the lack of a valid password. The data polling status will remain active, with DQ7 set to the complement of the DQ7 bit in the last word of the password unlock command, and DQ6 toggling. RY/BY# will remain low.

- The device requires approximately 100 μs for setting the PPB Lock after the valid 64-bit password is given to the device.

- The Password Unlock command cannot be accepted any faster than once every 100 μs ± 20 μs. This makes it take an unreasonably long time (58 million years) for a hacker to run through all the 64-bit combinations in an attempt to correctly match a password. The EA status checking methods may be used to determine when the EAC is ready to accept a new password command.

- If the password is lost after setting the Password Mode Lock Bit, there is no way to clear the PPB Lock.

4 Read Operations

4.1 Asynchronous Read

Each read access may be made to any location in the memory (random access). Each random access is selftimed with the same latency from CE# or address to valid data (t_{ACC} or t_{CE}).

4.2 Page Mode Read

Each random read accesses an entire 32-byte Page in parallel. Subsequent reads within the same Page have faster read access speed. The Page is selected by the higher address bits (A_{MAX}-A4), while the specific word of that page is selected by the least significant address bits A3-A0. The higher address bits are kept constant and only A3-A0 changed to select a different word in the same Page. This is an asynchronous access with data appearing on DQ15-DQ0 when CE# remains Low, OE# remains Low, and the asynchronous Page access time (t_{PACC}) is satisfied. If CE# goes High and returns Low for a subsequent access, a random read access is performed and time is required (t_{ACC} or tCE).

5 Embedded Operations

5.1 Embedded Algorithm Controller (EAC)

The EAC takes commands from the host system for programming and erasing the flash memory array and performs all the complex operations needed to change the non-volatile memory state. This frees the host system from any need to manage the program and erase processes.

There are four EAC operation categories:

- Standby (Read Mode)
- Address Space Switching
- Embedded Algorithms (EA)
- Advanced Sector Protection (ASP) Management

5.1.1 EAC Standby

In the standby mode current consumption is greatly reduced. The EAC enters its standby mode when no command is being processed and no Embedded Algorithm is in progress. If the device is deselected (CE# = High) during an Embedded Algorithm, the device still draws active current until the operation is completed (I_{CC3}). I_{CC4} in Section 9.4: DC Characteristics (page 48) represents the standby current specification when both the Host Interface and EAC are in their Standby state.

5.1.2 Address Space Switching

Writing specific address and data sequences (command sequences) switch the memory device address space from the main flash array to one of the Address Space Overlays (ASO).

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Embedded Algorithms operate on the information visible in the currently active (entered) ASO. The system continues to have access to the ASO until the system issues an ASO Exit command, performs a Hardware RESET, or until power is removed from the device. An ASO Exit Command switches from an ASO back to the main flash array address space. The commands accepted when a particular ASO is entered are listed between the ASO enter and exit commands in the command definitions table. See Table 7: Command Definitions (page 28) for address and data requirements for all command sequences.

5.1.3 Embedded Algorithms (EA)

Changing the non-volatile data in the memory array requires a complex sequence of operations that are called Embedded Algorithms (EA). The algorithms are managed entirely by the device internal Embedded Algorithm Controller (EAC). The main algorithms perform programming and erasing of the main array data and the ASO's. The host system writes command codes to the flash device address space. The EAC receives the commands, performs all the necessary steps to complete the command, and provides status information during the progress of an EA.

5.2 Program and Erase Summary

Flash data bits are erased in parallel in a large group called a sector. The Erase operation places each data bit in the sector in the logical 1 state (High). Flash data bits may be individually programmed from the erased 1 state to the programmed logical 0 (low) state. A data bit of 0 cannot be programmed back to a 1. A succeeding read shows that the data is still 0. Only erase operations can convert a 0 to a 1. Programming the same word location more than once with different 0 bits will result in the logical AND of the previous data and the new data being programmed.

5.2.1 Program Granularity

The MYX29GL01GS11DPIV2 supports two methods of programming, Word or Write Buffer Programming. Each Page can be programmed by either method. Pages programmed by different methods may be mixed within a Line for the Industrial Temperature version (-40°C to +85°C).

5.2.2 Incremental Programming

The same word location may be programmed more than once, by either the Word or Write Buffer Programming methods, to incrementally change 1's to 0's.

5.3 Command Set

5.3.1 Program Methods

5.3.1.1 Word Programming

Word programming is used to program a single word anywhere in the main Flash Memory Array.

The Word Programming command is a four-write-cycle sequence. The program command sequence is initiated by writing two unlock write cycles, followed by the program set up command. The program address and data are written next, which in turn initiate the Embedded Word Program algorithm. The system is not required to provide further controls or timing. The device automatically generates the program pulses and verifies the programmed cell margin internally. When the Embedded Word Program algorithm is complete, the EAC then returns to its standby mode.

5.3.1.2 Write Buffer Programming

A write buffer is used to program data within a 512-byte address range aligned on a 512-byte boundary (Line). Thus, a full Write Buffer Programming operation must be aligned on a Line boundary. Programming operations of less than a full 512 bytes may start on any word boundary but may not cross a Line boundary. At the start of a Write Buffer programming operation all bit locations in the buffer are all 1's (FFFFh words) thus any locations not loaded will retain the existing data.

Write Buffer Programming allows up to 512 bytes to be programmed in one operation. It is possible to program from 1 bit up to 512 bytes in each Write Buffer Programming operation. It is recommended that a multiple of Pages be written and each Page written only once. For the very best performance, programming should be done in full Lines of 512 bytes aligned on 512-byte boundaries.

Write Buffer Programming is supported only in the main flash array or the SSR ASO.

The Write Buffer Programming Sequence can be stopped by the following: Hardware Reset or Power cycle. However, using either of these methods may leave the area being programmed in an intermediate state with invalid or unstable data values. In this case the same area will need to be reprogrammed with the same data or erased to ensure data values are properly programmed or erased.

5.3.2 Program Suspend / Program Resume Commands

The Program Suspend command allows the system to interrupt an embedded programming operation so that data can read from any non-suspended Line. When the Program Suspend command is written during a programming process, the device halts the programming operation within t_{PSL} (program suspend latency) and updates the status bits. Addresses are don't-cares when writing the Program Suspend command.

There are two commands available for program suspend. The legacy combined Erase / Program suspend command (B0h command code) and the separate Program Suspend command (51h command code). There are also two commands for Program resume. The legacy combined Erase / Program resume command (30h command code) and the separate Program Resume command (50h command code). It is recommended to use the separate program suspend and resume commands for programming and use the legacy combined command only for erase suspend and resume.

5.3.3 Blank Check

The Blank Check command will confirm if the selected main flash array sector is erased. The Blank Check command does not allow for reads to the array during the Blank Check. Reads to the array while this command is executing will return unknown data.

5.3.4 Erase Methods

5.3.4.1 Chip Erase

The chip erase function erases the entire main Flash Memory Array. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all 0 data pattern prior to electrical erase. After a successful chip erase, all locations within the device contain FFFFh. The system is not required to provide any controls or timings during these operations. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. When WE# goes high, at the end of the 6th cycle, the RY/BY# goes low.

5.3.4.2 Sector Erase

The sector erase function erases one sector in the memory array. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire sector for an all 0 data pattern prior to electrical erase. After a successful sector erase, all locations within the erased sector contain FFFFh. The system is not required to provide any controls or timings during these operations. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. When WE# goes high, at the end of the 6th cycle, the RY/BY# goes low.

5.3.5 Erase Suspend / Erase Resume

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, the main flash array. This command is valid only during sector erase or program operation. The Erase Suspend command is ignored if written during the chip erase operation.

5.3.6 ASO Entry and Exit

5.3.6.1 ID-CFI ASO

The system can access the ID-CFI ASO by issuing the ID-CFI Entry command sequence during Read Mode. This entry command uses the Sector Address (SA) in the command to determine which sector will be overlaid and which sector's protection state is reported in word location 2h. See Table 8: ID (Autoselect) Address Map (page 33).

5.3.6.2 Status Register ASO

The Status Register ASO contains a single word of registered volatile status for Embedded Algorithms. When the Status Register read command is issued, the current status is captured (by the rising edge of WE#) into the register and the ASO is entered. The Status Register content appears on all word locations. The first read access exits the Status Register ASO (with the rising edge of CE# or OE#) and returns to the address space map in use when the Status Register read command was issued. Write commands will not exit the Status Register ASO state.

5.3.6.3 Secure Silicon Region ASO

The system can access the Secure Silicon Region by issuing the Secure Silicon Region Entry command sequence during Read Mode. This entry command uses the Sector Address (SA) in the command to determine which sector will be overlaid.

The Secure Silicon Region ASO allows the following activities:

- Read Secure Silicon Regions.
- Programming the customer Secure Silicon Region is allowed using the Word or Write Buffer Programming commands.
- ASO Exit using legacy Secure Silicon Exit command for backward software compatibility.
- ASO Exit using the common exit command for all ASO - alternative for a consistent exit method.

5.3.6.4 Lock Register ASO

The system can access the Lock Register by issuing the Lock Register entry command sequence during Read Mode. This entry command does not use a sector address from the entry command. The Lock Register appears at word location 0 in the device address space. All other locations in the device address space are undefined.

The Lock Register ASO allows the following activities:

- Read Lock Register, using device address location 0.
- Program the customer Lock Register using a modified Word Programming command.
- ASO Exit using legacy Command Set Exit command for backward software compatibility.
- ASO Exit using the common exit command for all ASO - alternative for a consistent exit method.

5.3.6.5 Password ASO

The system can access the Password ASO by issuing the Password entry command sequence during Read Mode. This entry command does not use a sector address from the entry command. The Password appears at word locations 0 to 3 in the device address space. All other locations in the device address space are undefined.

The Password ASO allows the following activities:

- Read Password, using device address location 0 to 3.
- Program the Password using a modified Word Programming command.
- Unlock the PPB Lock bit with the Password Unlock command.
- ASO Exit using legacy Command Set Exit command for backward software compatibility.
- ASO Exit using the common exit command for all ASO - alternative for a consistent exit method.

5.3.6.6 PPB ASO

The system can access the PPB ASO by issuing the PPB entry command sequence during Read Mode. This entry command does not use a sector address from the entry command. The PPB bit for a sector appears in bit 0 of all word locations in the sector.

The PPB ASO allows the following activities:

- Read PPB protection status of a sector in bit 0 of any word in the sector.
- Program the PPB bit using a modified Word Programming command.

- Erase all PPB bits with the PPB erase command.
- ASO Exit using legacy Command Set Exit command for backward software compatibility.
- ASO Exit using the common exit command for all ASO - alternative for a consistent exit method.

5.3.6.7 PPB Lock ASO

The system can access the PPB Lock ASO by issuing the PPB Lock entry command sequence during Read Mode. This entry command does not use a sector address from the entry command. The global PPB Lock bit appears in bit 0 of all word locations in the device.

The PPB Lock ASO allows the following activities:

- Read PPB Lock protection status in bit 0 of any word in the device address space.
- Set the PPB Lock bit using a modified Word Programming command.
- ASO Exit using legacy Command Set Exit command for backward software compatibility.
- ASO Exit using the common exit command for all ASO - alternative for a consistent exit method.

5.3.6.8 DYB ASO

The system can access the DYB ASO by issuing the DYB entry command sequence during Read Mode. This entry command does not use a sector address from the entry command. The DYB bit for a sector appears in bit 0 of all word locations in the sector.

The DYB ASO allows the following activities:

- Read DYB protection status of a sector in bit 0 of any word in the sector.
- Set the DYB bit using a modified Word Programming command.
- Clear the DYB bit using a modified Word Programming command.
- ASO Exit using legacy Command Set Exit command for backward software compatibility.
- ASO Exit using the common exit command for all ASO - alternative for a consistent exit method.

5.3.6.9 Software (Command) Reset / ASO exit

Software reset is part of the command set (aee Table 7: Command Definitions (page 28)) that also returns the EAC to standby state and must be used for the following conditions:

- Exit ID/CFI mode
- Clear timeout bit (DQ5) for data polling when timeout occurs

*Advanced information. Subject to change without notice.

Software Reset does not affect EA mode. Reset commands are ignored once programming or erasure has begun, until the operation is complete. Software Reset does not affect outputs; it serves primarily to return to Read Mode from an ASO mode or from a failed program or erase operation.

Software Reset may cause a return to Read Mode from undefined states that might result from invalid command sequences. However, a Hardware Reset may be required to return to normal operation from some undefined states. There is no software reset latency requirement.

The reset command is executed during the t_{WPH} period.

5.4 Status Monitoring

There are three methods for monitoring EA status. Previous generations of the MYX29GL01GS11DPIV2 used the methods called Data Polling and Ready/Busy# (RY/BY#) Signal. These methods are still supported by the MYX29GL01GS11DPIV2. One additional method is reading the Status Register.

5.4.1 Status Register

The status of program and erase operations is provided by a single 16-bit status register. The status is receiver by writing the Status Register Read command followed by a read access. When the Status Register read command is issued, the current status is captured (by the rising edge of WE#) into the register and the ASO is entered. The contents of the status register is aliased (overlaid) on the full memory address space. Any valid read (CE# and OE# low) access while in the Status Register ASO will exit the ASO (with the rising edge of CE# or OE# for t_{CEPH}/t_{OEPH} time) and return to the address space map in use when the Status Register Read command was issued.

The status register contains bits related to the results - success or failure - of the most recently completed Embedded Algorithms (EA):

- Erase Status (bit 5),
- Program Status (bit 4),
- Write Buffer Abort (bit 3),
- Sector Locked Status (bit 1),
- RFU (bit 0).

and, bits related to the current state of any in process EA:

- Device Busy (bit 7),
- Erase Suspended (bit 6),
- Program Suspended (bit 2),

The current state bits indicate whether an EA is in process, suspended, or completed.

Advanced information. Subject to change without notice.

5.4.2   Data Polling Status

During an active Embedded Algorithm the EAC switches to the Data Polling ASO to display EA status to any read access. A single word of status information is aliased in all locations of the device address space. In the status word there are several bits to determine the status of an EA. These are referred to as DQ bits as they appear on the data bus during a read access while an EA is in progress. DQ bits 15 to 8, DQ4, and DQ0 are reserved and provide undefined data. Status monitoring software must mask the reserved bits and treat them as don't care.

5.5   Error Types and Clearing Procedures

There are three types of errors reported by the embedded operation status methods. Depending on the error type, the status reported and procedure for clearing the error status is different. Following is the clearing of error status:

- If an ASO was entered before the error the device remains entered in the ASO awaiting ASO read or a command write.
- If an erase was suspended before the error the device returns to the erase suspended state awaiting flash array read or a command write.
- Otherwise, the device will be in standby state awaiting flash array read or a command write.

5.5.1   Embedded Operation Error

If an error occurs during an embedded operation (program, erase, blank check, or password unlock) the device (EAC) remains busy. The RY/BY# output remains Low, data polling status continues to be overlaid on all address locations, and the status register shows ready with valid status bits. The device remains busy until the error status is detected by the host system status monitoring and the error status is cleared.

5.5.2   Protection Error

If an embedded algorithm attempts to change data within a protected area (program, or erase of a protected sector or OTP area) the device (EAC) goes busy for a period of 20 to 100 µs then returns to normal operation. During the busy period the RY/BY# output remains Low, data polling status continues to be overlaid on all address locations, and the status register shows not ready with invalid status bits (SR[7] = 0).

5.5.3   Write Buffer Abort

If an error occurs during a Write to Buffer command the device (EAC) remains busy. The RY/BY# output remains Low, data polling status continues to be overlaid on all address locations, and the status register shows ready with valid status bits. The device remains busy until the error status is detected by the host system status monitoring and the error status is cleared.

5.6 Embedded Algorithm Performance Table

Table 6: Embedded Algorithm Characteristics (-40°C to +85°C)

Parameter		Typ[2]	Max[3]	Unit	Comments
Sector Erase Time 128 kbyte		275	1100	ms	Includes pre-programming prior to erasure[5]
Single Word Programming Time[1]		125	400	µs	
Buffer Programming Time	2-byte[1]	125	750	µs	
	32-byte[1]	160	750		
	64-byte[1]	175	750		
	128-byte[1]	198	750		
	256-byte[1]	239	750		
	512-byte	340	750		
Effective Write Buffer Program Operation per Word	512-byte	1.33		µs	
Sector Programming Time 128 kB (full Buffer Programming)		108	192	ms	Note 6
Erase Suspend/Erase Resume (t$_{ESL}$)			40	µs	
Program Suspend/Program Resume (t$_{PSL}$)			40	µs	
Erase Resume to next Erase Suspend (t$_{ERS}$)		100		µs	Minimum of 60 ns but ≥ typical periods are needed for Erase to progress to completion.
Program Resume to next Program Suspend (t$_{PRS}$)		100		µs	Minimum of 60 ns but ≥ typical periods are needed for Program to progress to completion.
Blank Check		6.2	8.5	ms	
NOP (Number of Program-operations, per Line)			256		

Notes:

1. Not 100% tested.

2. Typical program and erase times assume the following conditions: 25°C, 3.0V V$_{CC}$, 10,000 cycle, and a random data pattern.

3. Under worst case conditions of 90°C, V$_{CC}$ = 2.70V, 100,000 cycles, and a random data pattern.

4. Effective write buffer specification is based upon a 512-byte write buffer operation.

5. In the pre-programming step of the Embedded Erase algorithm, all words are programmed to 0000h before Sector and Chip erasure.

6. System-level overhead is the time required to execute the bus-cycle sequence for the program command.

6 Software Interface Reference

6.1 Command Summary

Table 7: Command Definitions

Command Sequence[1]	Cycles	Bus Cycles[2-5]												
		First		Second		Third		Fourth		Fifth		Sixth		Seventh	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read[6]	1	RA	RD												
Reset/ASO Exit[7,16]	1	XXX	F0												
Status Register Read	2	555	70	XXX	RD										
Status Register Clear	1	555	71												
Word Program	4	555	AA	2AA	55	555	A0	PA	PD						
Write to Buffer	6	555	AA	2AA	55	SA	25	SA	WC	WBL	PD	WBL	PD		
Program Buffer to Flash (confirm)	1	SA	29												
Write-to-Buffer-Abort Reset[11]	3	555	AA	2AA	55	555	F0								
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10		
Sector Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30		
Erase Suspend/Program Suspend Legacy Method[9]	1	XXX	B0												
Erase Suspend Enhanced Method															
Erase Resume/Program Resume Legacy Method[10]	1	XXX	30												
Erase Resume Enhanced Method															
Program Suspend Enhanced Method	1	XXX	51												
Program Resume Enhanced Method	1	XXX	50												
Blank Check	1	(SA) 555	33												

*Advanced information. Subject to change without notice.

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Table 7: Command Definitions (continued)

Command Sequence[1]		Cycles	Bus Cycles[2-5]												
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
ID-CFI (Autoselect) ASO	ID (Autoselect) Entry	3	555	AA	2AA	55	(SA) 555	90								
	CFI Enter (Note 8)	1	(SA) 55	98												
	ID-CFI Read	1	RA	RD												
	Reset/ASO Exit (Notes 7, 16)	1	XXX	F0												
Secure Silicon Region Command Definitions																
Secure Silicon Region (SSR) ASO	SSR Entry	3	555	AA	2AA	55	(SA) 555	88								
	Read[6]	1	RA	RD												
	Word Program	4	555	AA	2AA	55	555	A0	PA	PD						
	Write to Buffer	6	555	AA	2AA	55	SA	25	SA	WC	WBL	PD	WBL	PD		
	Program Buffer to Flash (confirm)	1	SA	29												
	Write-to-Buffer-Abort Reset[11]	3	555	AA	2AA	55	555	F0								
	SSR Exit[11]	4	555	AA	2AA	55	555	90	XX	0						
	Reset/ASO Exit[7, 16]	1	XXX	F0												
Lock Register Command Set Definitions																
Lock Register ASO	Lock Register Entry	3	555	AA	2AA	55	555	40								
	Program[15]	2	XXX	A0	XXX	PD										
	Read[15]	1	0	RD												
	Command Set Exit[12, 16]	2	XXX	90	XXX	0										
	Reset/ASO Exit[7, 16]	1	XXX	F0												

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Table 7: Command Definitions (continued)

Command Sequence[1]		Cycles	Bus Cycles[2-5]												
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Password Protection Command Set Definitions																
Password ASO	Password ASO Entry	3	555	AA	2AA	55	555	60								
	Program[14]	2	XXX	A0	PWAx	PWDx										
	Read[13]	4	0	PWD0	1	PWD1	2	PWD2	3	PWD 3						
	Unlock	7	0	25	0	3	0	PWD0	1	PWD 1	2	PWD2	3	PWD 3	0	29
	Command Set Exit[12, 16]	2	XXX	90	XXX	0										
	Reset/ASO Exit[7, 16]	1	XXX	F0												
Non-Volatile Sector Protection Command Set Definitions																
PPB (Non-Volatile Sector Protection)	PPB Entry	3	555	AA	2AA	55	555	C0								
	PPB Program[17]	2	XXX	A0	SA	0										
	All PPB Erase[17]	2	XXX	80	0	30										
	PPB Read[17]	1	SA	RD (0)												
	Command Set Exit[12, 16]	2	XXX	90	XXX	0										
	Reset/ASO Exit[7, 16]	1	XXX	F0												
Global Non-Volatile Sector Protection Freeze Command Set Definitions																
PPB Lock Bit	PPB Lock Entry	3	555	AA	2AA	55	555	50								
	PPB Lock Bit Cleared	2	XXX	A0	XXX	0										
	PPB Lock Status Read[17]	1	XXX	RD (0)												
	Command Set Exit[12, 16]	2	XXX	90	XXX	0										
	Reset/ASO Exit[7, 16]	1	XXX	F0												
Volatile Sector Protection Command Set Definitions																
DYB (Volatile Sector Protection) ASO	DYB ASO Entry	3	555	AA	2AA	55	555	E0								
	DYB Set[17]	2	XXX	A0	SA	0										
	DYB Clear[17]	2	XXX	A0	SA	1										
	DYB Status Read[17]	1	SA	RD (0)												
	Command Set Exit[12, 16]	2	XXX	90	XXX	0										
	Reset/ASO Exit[16]	1	XXX	F0												

Table 7: Command Definitions (continued)

Legend:

- X = Don't care.
- RA = Address of the memory to be read.
- RD = Data read from location RA during read operation.
- PA = Address of the memory location to be programmed.
- PD = Data to be programmed at location PA.
- SA = Address of the sector selected. Address bits A_{MAX}-A16 uniquely select any sector.
- WBL = Write Buffer Location. The address must be within the same Line.
- WC = Word Count is the number of write buffer locations to load minus 1.
- PWAx = Password address for word0 = 00h, word1 = 01h, word2 = 02h, and word3 = 03h.
- PWDx = Password data word0, word1, word2, and word3.

Notes:

1. See Table 15: Interface States (page 41) for description of bus operations.
2. All values are in hexadecimal.
3. Except for the following, all bus cycles are write cycle: read cycle during Read, ID/CFI Read (Manufacturing ID / Device ID), Indicator Bits, Secure Silicon Region Read, SSR Lock Read, and 2nd cycle of Status Register Read .
4. Data bits DQ15-DQ8 are don't care in command sequences, except for RD, PD, WC and PWD.
5. Address bits A_{MAX}-A11 are don't cares for unlock and command cycles, unless SA or PA required. (A_{MAX} is the Highest Address pin.).
6. No unlock or command cycles required when reading array data.
7. The Reset command is required to return to reading array data when device is in the ID-CFI (autoselect) mode, or if DQ5 goes High (while the device is providing status data).
8. Command is valid when device is ready to read array data or when device is in ID-CFI (autoselect) mode.
9. The system can read and program/program suspend in non-erasing sectors, or enter the ID-CFI ASO, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
10. The Erase Resume/Program Resume command is valid only during the Erase Suspend/Program Suspend modes.
11. Issue this command sequence to return to READ mode after detecting device is in a Write-to-Buffer-Abort state. IMPORTANT: the full command sequence is required if resetting out of ABORT.
12. The Exit command returns the device to reading the array.
13. The password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.

14. For PWDx, only one portion of the password can be programmed per each A0 command. Portions of the password must be programmed in sequential order (PWD0 - PWD3).

15. All Lock Register bits are one-time programmable. The program state = 0 and the erase state = 1. Also, both the Persistent Protection Mode Lock Bit and the Password Protection Mode Lock Bit cannot be programmed at the same time or the Lock Register Bits Program operation aborts and returns the device to read mode. Lock Register bits that are reserved for future use are undefined and may be 0's or 1's.

16. If any of the Entry commands was issued, an Exit command must be issued to reset the device into read mode.

17. Protected State = 00h, Unprotected State = 01h. The sector address for DYB set, DYB clear, or PPB Program command may be any location within the sector - the lower order bits of the sector address are don't care.

6.2 Device ID and Common Flash Interface (ID-CFI) ASO Map

The Device ID portion of the ASO (word locations 0h to 0Fh) provides manufacturer ID, device ID, Sector Protection State, and basic feature set information for the device.

ID-CFI Location 02h displays sector protection status for the sector selected by the sector address (SA) used in the ID-CFI enter command. To read the protection status of more than one sector it is necessary to exit the ID ASO and enter the ID ASO using the new SA. The access time to read location 02h is always t_{ACC} and a read of this location requires CE# to go High before the read and return Low to initiate the read (asynchronous read access). Page mode read between location 02h and other ID locations is not supported. Page mode read between ID locations other than 02h is supported.

Table 8: ID (Autoselect) Address Map

Description	Address	Read Data
Manufacture ID	(SA) + 0000h	0001h
Device ID	(SA) + 0001h	227Eh
Protection Verification	(SA) + 0002h	Sector Protection State (1= Sector protected, 0= Sector unprotected). This protection state is shown only for the SA selected when entering ID-CFI ASO. Reading other SA provides undefined data. To read a different SA protection state ASO exit command must be used and then enter ID-CFI ASO again with the new SA.

Indicator Bits	(SA) + 0003h	DQ15-DQ08 = 1 (Reserved)
		DQ7 - Factory Locked Secure Silicon Region
		    1 = Locked,
		    0 = Not Locked
		DQ6 - Customer Locked Secure Silicon Region
		    1 = Locked
		    0 = Not Locked DQ5 = 1 (Reserved) DQ4 - WP# Protects
		    0 = lowest address Sector
		    1 = highest address Sector
		DQ3 - DQ0 = 1 (Reserved)

RFU	(SA) + 0004h	Reserved
	(SA) + 0005h	Reserved
	(SA) + 0006h	Reserved
	(SA) + 0007h	Reserved
	(SA) + 0008h	Reserved
	(SA) + 0009h	Reserved
	(SA) + 000Ah	Reserved
	(SA) + 000Bh	Reserved

Lower Software Bits	(SA) + 000Ch	Bit 0 - Status Register Support
		    1 = Status Register Supported
		    0 = Status Register not supported
		Bit 1 - DQ polling Support
		    1 = DQ bits polling supported
		    0 = DQ bits polling not supported
		Bit 3-2 - Command Set Support
		    11 = reserved
		    10 = reserved
		    01 = Reduced Command Set
		    00 = Classic Command set
		Bits 4-15 - Reserved = 0

Upper Software Bits	(SA) + 000Dh	Reserved
Device ID	(SA) + 000Eh	2228h = 1 Gb 2223h = 512 Mb 2222h = 256 Mb 2221h = 128 Mb
Device ID	(SA) + 000Fh	2201h

Table 9: CFI Query Identification String

Word Address	Data	Description
(SA) + 0010h (SA) + 0011h (SA) + 0012h	0051h 0052h 0059h	Query Unique ASCII string "QRY"
(SA) + 0013h (SA) + 0014h	0002h 0000h	Primary OEM Command Set
(SA) + 0015h (SA) + 0016h	0040h 0000h	Address for Primary Extended Table
(SA) + 0017h (SA) + 0018h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
(SA) + 0019h (SA) + 001Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 10: CFI System Interface String

Word Address	Data	Description
(SA) + 001Bh	0027h	V_{CC} Min. (erase/program) (D7-D4: volts, D3-D0: 100 mV)
(SA) + 001Ch	0036h	V_{CC} Max. (erase/program) (D7-D4: volts, D3-D0: 100 mV)
(SA) + 001Dh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
(SA) + 001Eh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
(SA) + 001Fh	0008h	Typical timeout per single word write 2N µs
(SA) + 0020h	0009h	Typical timeout for max multi-byte program, 2N µs (00h = not supported)
(SA) + 0021h	0008h	Typical timeout per individual block erase 2N ms
(SA) + 0022h	0012h (1 Gb) 0011h (512 Mb) 0010h (256 Mb) 000Fh (128 Mb)	Typical timeout for full chip erase 2N ms (00h = not supported)
(SA) + 0023h	0001h	Max. timeout for single word write 2N times typical
(SA) + 0024h	0002h	Max. timeout for buffer write 2N times typical
(SA) + 0025h	0003h	Max. timeout per individual block erase 2N times typical
(SA) + 0026h	0003h	Max. timeout for full chip erase 2N times typical (00h = not supported)

Table 11: CFI Device Geometry Definition

Word Address	Data	Description
(SA) + 0027h	001Bh (1 Gb) 001Ah (512 Mb) 0019h (256 Mb) 0018h (128 Mb)	Device Size = 2^N byte;
(SA) + 0028h	0001h	Flash Device Interface Description 0 = x8-only, 1 = x16-only, 2 = x8/x16 capable
(SA) + 0029h	0000h	
(SA) + 002Ah	0009h	Max. number of byte in multi-byte write = 2^N (00 = not supported)
(SA) + 002Bh	0000h	
(SA) + 002Ch	0001h	Number of Erase Block Regions within device; 1 = Uniform Device, 2 = Boot Device
(SA) + 002Dh	00XXh	Erase Block Region 1 Information (refer to JEDEC JESD68-01 or JEP137 specifications) 00FFh, 0003h, 0000h, 0002h =1 Gb 00FFh, 0001h, 0000h, 0002h = 512 Mb 00FFh, 0000h, 0000h, 0002h = 256 Mb 007Fh, 0000h, 0000h, 0002h = 128 Mb
(SA) + 002Eh	000Xh	
(SA) + 002Fh	0000h	
(SA) + 0030h	000Xh	
(SA) + 0031h	0000h	Erase Block Region 2 Information (refer to CFI publication 100)
(SA) + 0032h	0000h	
(SA) + 0033h	0000h	
(SA) + 0034h	0000h	
(SA) + 0035h	0000h	Erase Block Region 3 Information (refer to CFI publication 100)
(SA) + 0036h	0000h	
(SA) + 0037h	0000h	
(SA) + 0038h	0000h	
(SA) + 0039h	0000h	Erase Block Region 4 Information (refer to CFI publication 100)
(SA) + 003Ah	0000h	
(SA) + 003Bh	0000h	
(SA) + 003Ch	0000h	
(SA) + 003Dh	FFFFh	Reserved
(SA) + 003Eh	FFFFh	Reserved
(SA) + 003Fh	FFFFh	Reserved

Table 12: CFI Primary Vendor-Specific Extended Query

Word Address	Data	Description
(SA) + 0040h	0050h	Query-unique ASCII string "PRI"
(SA) + 0041h	0052h	
(SA) + 0042h	0049h	
(SA) + 0043h	0031h	Major version number, ASCII
(SA) + 0044h	0035h	Minor version number, ASCII

(SA) + 0045h	001Ch	Address Sensitive Unlock (Bits 1-0)
		    00b = Required
		    01b = Not Required
		Process Technology (Bits 5-2)
		    0000b = 0.23 µm Floating Gate
		    0001b = 0.17 µm Floating Gate
		    0010b = 0.23 µm MirrorBit
		    0011b = 0.13 µm Floating Gate
		    0100b = 0.11 µm MirrorBit
		    0101b = 0.09 µm MirrorBit
		    0110b = 0.09 µm Floating Gate
		    0111b = 0.065 µm MirrorBit Eclipse
		    1000b = 0.065 µm MirrorBit
		    1001b = 0.045 µm MirrorBit

(SA) + 0046h	0002h	Erase Suspend
		    0 = Not Supported
		    1 = Read Only
		    2 = Read and Write

(SA) + 0047h	0001h	Sector Protect
		    00 = Not Supported
		    X = Number of sectors in smallest group

(SA) + 0048h	0000h	Temporary Sector Unprotect
		    00 = Not Supported
		    01 = Supported

(SA) + 0049h	0008h	Sector Protect/Unprotect Scheme
		    04 = High Voltage Method
		    05 = Software Command Locking Method
		    08 = Advanced Sector Protection Method

(SA) + 004Ah	0000h	Simultaneous Operation
		    00 = Not Supported
		    X = Number of banks

(SA) + 004Bh	0000h	Burst Mode Type
		    00 = Not Supported
		    01 = Supported

Table 12: CFI Primary Vendor-Specific Extended Query (continued)

Word Address	Data	Description
(SA) + 004Ch	0003h	Page Mode Type 00 = Not Supported 01 = 4 Word Page 02 = 8 Word Page 03=16 Word Page
(SA) + 004Dh	0000h	ACC (Acceleration) Supply Minimum 00 = Not Supported D7-D4: Volt D3-D0: 100 mV
(SA) + 004Eh	0000h	ACC (Acceleration) Supply Maximum 00 = Not Supported D7-D4: Volt D3-D0: 100 mV
(SA) + 004Fh	0004h (Bottom) 0005h (Top)	WP# Protection 00h = Flash device without WP Protect (No Boot) 01h = Eight 8 kB Sectors at TOP and Bottom with WP (Dual Boot) 02h = Bottom Boot Device with WP Protect (Bottom Boot) 03h = Top Boot Device with WP Protect (Top Boot) 04h = Uniform, Bottom WP Protect (Uniform Bottom Boot) 05h = Uniform, Top WP Protect (Uniform Top Boot) 06h = WP Protect for all sectors 07h = Uniform, Top and Bottom WP Protect
(SA) + 0050h	0001h	Program Suspend 00 = Not Supported 01 = Supported
(SA) +0051h	0000h	Unlock Bypass 00 = Not Supported 01 = Supported
(SA) + 0052h	0009h	Secured Silicon Sector (Customer OTP Area) Size 2N (bytes)
(SA) + 0053h	008Fh	Software Features bit 0: status register polling (1 = supported, 0 = not supported) bit 1: DQ polling (1 = supported, 0 = not supported) bit 2: new program suspend/resume commands (1 = supported, 0 = not supported) bit 3: word programming (1 = supported, 0 = not supported) bit 4: bit-field programming (1 = supported, 0 = not supported) bit 5: autodetect programming (1 = supported, 0 = not supported) bit 6: RFU bit 7: multiple writes per Line (1 = supported, 0 = not supported)

Advanced information. Subject to change without notice.

Table 12: CFI Primary Vendor-Specific Extended Query (continued)

Word Address	Data	Description
(SA) + 0054h	0005h	Page Size = 2^N bytes
(SA) + 0055h	0006h	Erase Suspend Timeout Maximum < 2^N (µs)
(SA) + 0056h	0006h	Program Suspend Timeout Maximum < 2^N (µs)
(SA) + 0057h to (SA) + 0077h	FFFFh	Reserved
(SA) + 0078h	0006h	Embedded Hardware Reset Timeout Maximum < 2^N (µs) Reset with Reset Pin
(SA) + 0079h	0009h	Non-Embedded Hardware Reset Timeout Maximum < 2N (µs) Power on Reset

7 Signal Descriptions

7.1 Address and Data Configuration

Address and data are connected in parallel (ADP) via separate signal inputs and I/Os.

7.2 Input/Output Summary

Table 13: I/O Summary

Symbol	Type	Description
RESET#	Input	Hardware Reset. At V_{IL}, causes the device to reset control logic to its standby state, ready for reading array data.
CE#	Input	Chip Enable. At V_{IL}, selects the device for data transfer with the host memory controller.
OE#	Input	Output Enable. At V_{IL}, causes outputs to be actively driven. At V_{IH}, causes outputs to be high impedance (High-Z).
WE#	Input	Write Enable. At V_{IL}, indicates data transfer from host to device. At V_{IH}, indicates data transfer is from device to host.
A_{MAX}-A0	Input	Address input. A25-A0
DQ15-DQ0	Input/Output	Data inputs and outputs.
WP#	Input	Write Protect. At V_{IL}, disables program and erase functions in the lowest or highest address 64-kword (128-kB) sector of the device. At V_{IH}, the sector is not protected. WP# has an internal pull up; When unconnected WP# is at V_{IH}.

Table 13: I/O Summary (continued)

Symbol	Type	Description
RY/BY#	Output - open drain	Ready/Busy. Indicates whether an Embedded Algorithm is in progress or complete. At V_{IL}, the device is actively engaged in an Embedded Algorithm such as erasing or programming. At High-Z, the device is ready for read or a new command write - requires external pull-up resistor to detect the High-Z state. Multiple devices may have their RY/BY# outputs tied together to detect when all devices are ready.
V_{CC}	Power Supply	Core power supply
V_{IO}	Power Supply	Versatile IO power supply.
V_{SS}	Power Supply	Power supplies ground
NC	No Connect	Not Connected internally. The pin/ball location may be used in Printed Circuit Board (PCB) as part of a routing channel.
RFU	No Connect	Reserved for Future Use. Not currently connected internally but the pin/ball location should be left unconnected and unused by PCB routing channel for future compatibility. The pin/ball may be used by a signal in the future.
DNU	Reserved	Do Not Use. Reserved for use by the OCM. The pin/all is connected internally. The input has an internal pull down resistance to V_{SS}. The pin/ball can be left open or tied to V_{SS} on the PCB.

7.3 Versatile I/O Feature

The maximum output voltage level driven by, and input levels acceptable to, the device are determined by the V_{IO} power supply. This supply allows the device to drive and receive signals to and from other devices on the same bus having interface signal levels different from the device core voltage.

7.4 Ready/Busy# (RY/BY#)

RY/BY# is a dedicated, open drain output pin that indicates whether an Embedded Algorithm, Power-On Reset (POR), or Hardware Reset is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in a command sequence, when V_{CC} is above V_{CC} minimum during POR, or after the falling edge of RESET#. Since RY/BY# is an open drain output, several RY/BY# pins can be tied together in parallel with a pull up resistor to V_{IO}.

If the output is Low (Busy), the device is actively erasing, programming, or resetting. (This includes programming in the Erase Suspend mode). If the output is High (Ready), the device is ready to read data (including during the Erase Suspend mode), or is in the standby mode.

If an Embedded algorithm has failed (Program / Erase failure as result of max pulses or Sector is locked), RY/BY# will stay Low (busy) until status register bits 4 and 5 are cleared and the reset command is issued. This includes Erase or Programming on a locked sector.

7.5 Hardware Reset

The RESET# input provides a hardware method of resetting the device to standby state. When RESET# is driven Low for at least a period of t_{RP}, the device immediately:

- terminates any operation in progress,
- exits any ASO,
- tristates all outputs,
- resets the Status Register,
- resets the EAC to standby state.
- CE# is ignored for the duration of the reset operation (t_{RPH}).
- To meet the Reset current specification (I_{CC5}) CE# must be held High.

To ensure data integrity any operation that was interrupted should be reinitiated once the device is ready to accept another command sequence.

8 Signal Protocols

The following sections describe the host system interface signal behavior and timing for the MYX29GL01GS11DPIV2.

8.1 Interface States

Table 15 describes the required value of each interface signal for each interface state.

Table 15: Interface States

Interface State	V_{CC}	V_{IO}	RESET#	CE#	OE#	WE#	A_{MAX}-A0	DQ15-DQ0
Power-Off with Hardware Data Protection	$< V_{LKO}$	$\leq V_{CC}$	X	X	X	X	X	High-Z
Power-On (Cold) Reset	$\geq V_{CC}$ min	$\geq V_{IO}$ min; $\leq V_{CC}$	X	X	X	X	X	High-Z
Hardware (Warm) Reset	$\geq V_{CC}$ min	$\geq V_{IO}$ min; $\leq V_{CC}$	L	X	X	X	X	High-Z
Interface Standby	$\geq V_{CC}$ min	$\geq V_{IO}$ min; $\leq V_{CC}$	H	H	X	X	X	High-Z
Automatic Sleep[1, 3]	$\geq V_{CC}$ min	$\geq V_{IO}$ min; $\leq V_{CC}$	H	L	X	X	Valid	Output Available
Read with Output Disable[2]	$\geq V_{CC}$ min	$\geq V_{IO}$ min; $\leq V_{CC}$	H	L	H	H	Valid	High-Z
Random Read	$\geq V_{CC}$ min	$\geq V_{IO}$ min	H	L	L	H	Valid	Output Valid
Page Read	$\geq V_{CC}$ min	$\geq V_{IO}$ min; $\leq V_{CC}$	H	L	L	H	A_{MAX}-A4 Valid A3-A0 Modified	Output Valid
Write	$\geq V_{CC}$ min	$\geq V_{IO}$ min; $\leq V_{CC}$	H	L	H	L	Valid	Input Valid

Legend:

1. L = V_{IL}
2. H = V_{IH}
3. X = either V_{IL} or V_{IH}
4. L/H = rising edge
5. H/L = falling edge
6. Valid = all bus signals have stable L or H level
7. Modified = valid state different from a previous valid state
8. Available = read data is internally stored with output driver controlled by OE#

Notes:

1. WE# and OE# can not be at V_{IL} at the same time.
2. Read with Output Disable is a read initiated with OE# High.
3. Automatic Sleep is a read/write operation where data has been driven on the bus for an extended period, without CE# going High and the device internal logic has gone into standby mode to conserve power.

8.2 Power-Off with Hardware Data Protection

The memory is considered to be powered off when the core power supply (V_{CC}) drops below the lock-out voltage (V_{LKO}). When V_{CC} is below V_{LKO}, the entire memory array is protected against a program or erase operation. This ensures that no spurious alteration of the memory content can occur during power transition. During a power supply transition down to Power-Off, V_{IO} should remain less than or equal to V_{CC}.

If V_{CC} goes below V_{RST} (Min) then returns above V_{RST} (Min) to V_{CC} minimum, the Power-On Reset interface state is entered and the EAC starts the Cold Reset Embedded Algorithm.

8.3 Power Conservation Modes

8.3.1 Interface Standby

Standby is the default, low power, state for the interface while the device is not selected by the host for data transfer (CE# = High). All inputs are ignored in this state and all outputs except RY/BY# are high impedance. RY/BY# is a direct output of the EAC, not controlled by the Host Interface.

8.3.2 Automatic Sleep

The automatic sleep mode reduces device interface energy consumption to the sleep level (I_{CC6}) following the completion of a random read access time. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. While in sleep mode, output data is latched and always available to the system. Output of the data depends on the level of the OE# signal but, the automatic sleep mode current is independent of the OE# signal level. Standard address access timings (t_{ACC} or t_{PACC}) provide new data when addresses are changed. I_{CC6} in Section 9.4: DC Characteristics (page 48) represents the automatic sleep mode current specification.

Automatic sleep helps reduce current consumption especially when the host system clock is slowed for power reduction. During slow system clock periods, read and write cycles may extend many times their length versus when the system is operating at high speed. Even though CE# may be Low throughout these extended data transfer cycles, the memory device host interface will go to the Automatic Sleep current at t_{ACC} + 30 ns. The device will remain at the Automatic Sleep current for t_{ASSB}. Then the device will transition to the standby current level. This keeps the memory at the Automatic Sleep or standby power level for most of the long duration data transfer cycles, rather than consuming full read power all the time that the memory device is selected by the host system.

However, the EAC operates independent of the automatic sleep mode of the host interface and will continue to draw current during an active Embedded Algorithm. Only when both the host interface and EAC are in their standby states is the standby level current achieved.

8.4 Read

8.4.1 Read With Output Disable

When the CE# signal is asserted Low, the host system memory controller begins a read or write data transfer. Often there is a period at the beginning of a data transfer when CE# is Low, Address is valid, OE# is High, and WE# is High. During this state a read access is assumed and the Random Read process is started while the data outputs remain at high impedance. If the OE# signal goes Low, the interface transitions to the Random Read state, with data outputs actively driven. If the WE# signal is asserted Low, the interface transitions to the Write state. Note, OE# and WE# should never be Low at the same time to ensure no data bus contention between the host system and memory.

8.4.2 Random (Asynchronous) Read

When the host system interface selects the memory device by driving CE# Low, the device interface leaves the Standby state. If WE# is High when CE# goes Low, a random read access is started. The data output depends on the address map mode and the address provided at the time the read access is started.

The data appears on DQ15-DQ0 when CE# is Low, OE# is Low, WE# remains High, address remains stable, and the asynchronous access times are satisfied. Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable CE# to valid data at the outputs. In order for the read data to be driven on to the data outputs the OE# signal must be Low at least the output enable time (t_{OE}) before valid data is available.

At the completion of the random access time from CE# active (t_{CE}), address stable (t_{ACC}), or OE# active (t_{OE}), whichever occurs latest, the data outputs will provide valid read data from the currently active address map mode. If CE# remains Low and any of the A_{MAX} to A4 address signals change to a new value, a new random read access begins. If CE# remains Low and OE# goes High the interface transitions to the Read with Output Disable state. If CE# remains Low, OE# goes High, and WE# goes Low, the interface transitions to the Write state. If CE# returns High, the interface goes to the Standby state. Back to Back accesses, in which CE# remains Low between accesses, requires an address change to initiate the second access.

See .

8.4.3 Page Read

After a Random Read access is completed, if CE# remains Low, OE# remains Low, the A_{MAX} to A4 address signals remain stable, and any of the A3 to A0 address signals change, a new access within the same Page begins. The Page Read completes much faster (t_{PACC}) than a Random Read access.

*Advanced information. Subject to change without notice.

8.4.4 Asynchronous Write

When WE# goes Low after CE is Low, there is a transition from one of the read states to the Write state. If WE# is Low before CE# goes Low, there is a transition from the Standby state directly to the Write state without beginning a read access.

When CE# is Low, OE# is High, and WE# goes Low, a write data transfer begins. Note, OE# and WE# should never be Low at the same time to ensure no data bus contention between the host system and memory. When the asynchronous write cycle timing requirements are met the WE# can go High to capture the address and data values in to EAC command memory.

Address is captured by the falling edge of WE# or CE#, whichever occurs later. Data is captured by the rising edge of WE# or CE#, whichever occurs earlier.

When CE# is Low before WE# goes Low and stays Low after WE# goes High, the access is called a WE# controlled Write. When WE# is High and CE# goes High, there is a transition to the Standby state. If CE# remains Low and WE# goes High, there is a transition to the Read with Output Disable state.

When WE# is Low before CE# goes Low and remains Low after CE# goes High, the access is called a CE# controlled Write. A CE# controlled Write transitions to the Standby state.

If WE# is Low before CE# goes Low, the write transfer is started by CE# going Low. If WE# is Low after CE# goes High, the address and data are captured by the rising edge of CE#. These cases are referred to as CE# controlled write state transitions.

Write followed by Read accesses, in which CE# remains Low between accesses, requires an address change to initiate the following read access.

Back to Back accesses, in which CE# remains Low between accesses, requires an address change to initiate the second access.

The EAC command memory array is not readable by the host system and has no ASO. The EAC examines the address and data in each write transfer to determine if the write is part of a legal command sequence. When a legal command sequence is complete the EAC will initiate the appropriate EA.

8.4.5 Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on WE# will not initiate a write cycle.

8.4.6 Logical Inhibit

Write cycles are inhibited by holding OE# at V_{IL}, or CE# at V_{IH}, or WE# at V_{IH}. To initiate a write cycle, CE# and WE# must be Low (V_{IL}) while OE# is High (V_{IH}).

*Advanced information. Subject to change without notice.

9 Electrical Specifications

9.1 Absolute Maximum Ratings

Table 16: Absolute Maximum Ratings

Storage Temperature Plastic Packages	-65°C to +150°C
Ambient Temperature with Power Applied	-65°C to +125°C
Voltage with Respect to Ground	
All pins other than RESET#[1]	-0.5V to (V_{IO} + 0.5V)
RESET#[1]	-0.5V to (V_{CC} + 0.5V)
Output Short Circuit Current[2]	100 mA
V_{CC}	-0.5V to +4.0V
V_{IO}	

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, input or I/O pins may undershoot V_{SS} to -2.0V for periods of up to 20 ns. See Figure 5 (page 48). Maximum DC voltage on input or I/O pins is V_{CC} +0.5V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0V for periods up to 20 ns. See Figure 6 (page 48).
2. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
3. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

9.2 Latchup Characteristics

This product complies with JEDEC standard JESD78C latchup testing requirements.

9.3 Operating Ranges

9.3.1 Temperature Ranges

Industrial (I) Devices

Ambient Temperature (T_A) -40°C to +85°C

9.3.2 Power Supply Voltages

V_{CC} 2.7V to 3.6V

V_{IO} 1.65V to V_{CC} + 200 mV

Operating ranges define those limits between which the functionality of the device is guaranteed.

9.3.3 Power-Up and Power-Down

During power-up or power-down V_{CC} must always be greater than or equal to V_{IO} ($V_{CC} \geq V_{IO}$).

The device ignores all inputs until a time delay of t_{VCS} has elapsed after the moment that V_{CC} and V_{IO} both rise above, and stay above, the minimum V_{CC} and V_{IO} thresholds. During t_{VCS} the device is performing power on reset operations.

During power-down or voltage drops below V_{CC} Lockout maximum (V_{LKO}), the V_{CC} and V_{IO} voltages must drop below V_{CC} Reset (V_{RST}) minimum for a period of t_{PD} for the part to initialize correctly when V_{CC} and V_{IO} again rise to their operating ranges. See . If during a voltage drop the V_{CC} stays above V_{LKO} maximum the part will stay initialized and will work correctly when V_{CC} is again above V_{CC} minimum. If the part locks up from improper initialization, a hardware reset can be used to initialize the part correctly.

Normal precautions must be taken for supply decoupling to stabilize the V_{CC} and V_{IO} power supplies. Each device in a system should have the V_{CC} and V_{IO} power supplies decoupled by a suitable capacitor close to the package connections (this capacitor is generally on the order of 0.1 μF). At no time should V_{IO} be greater then 200 mV above V_{CC} ($V_{CC} \geq V_{IO}$ - 200 mV).

Table 17: Power-Up/Power-Down Voltage and Timing

Symbol	Parameter	Min	Max	Unit
V_{CC}	V_{CC} Power Supply	2.7	3.6	V
V_{LKO}	V_{CC} level below which re-initialization is required[1]	2.25	2.5	V
V_{RST}	V_{CC} and V_{IO} Low voltage needed to ensure initialization will occur[1]	1.0		V
t_{VCS}	V_{CC} and $V_{IO} \geq$ minimum to first access[1]	300		µs
t_{PD}	Duration of $V_{CC} \leq V_{RST}$(min)[1]	15		µs

Note: 1. Not 100% tested.

Figure 3: Power-up
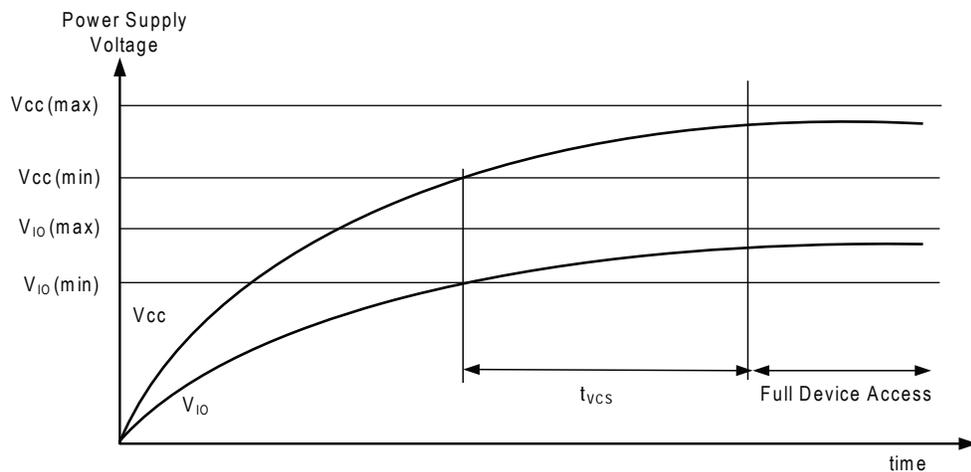
Figure 4: Power-down and Voltage Drop
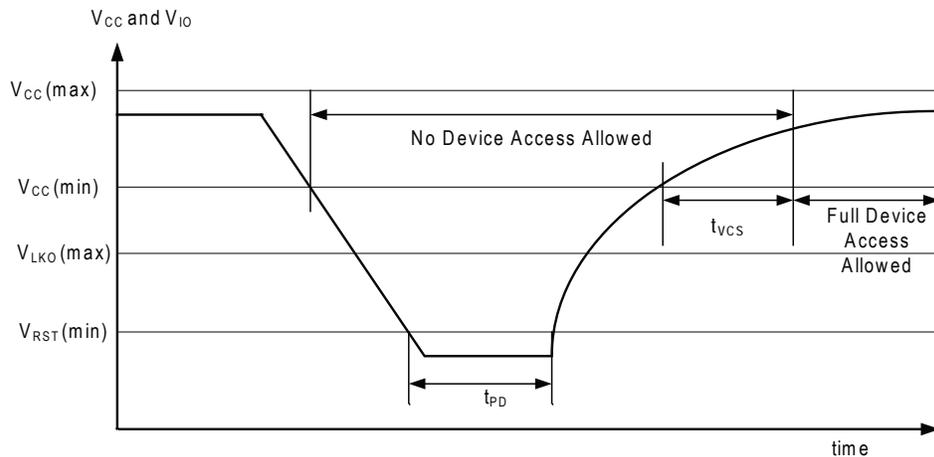
9.3.4   Input Signal Overshoot

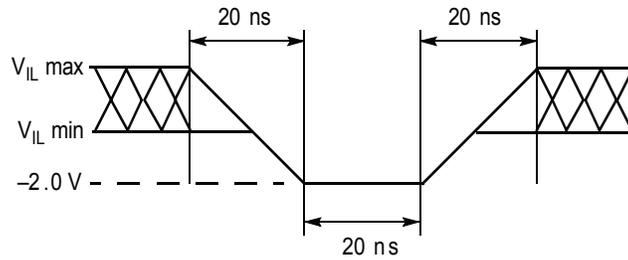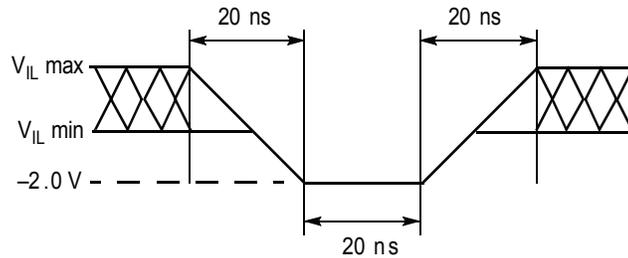Figure 5: Maximum Negative Overshoot Waveform

Figure 6: Maximum Positive Overshoot Waveform

9.4   DC Characteristics

Table 18: DC Characteristics (-40°C to +85°C)

Parameter	Description	Test Conditions	Min	Typ[2]	Max	Unit
V_{SS}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max		+0.02	±1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max		+0.02	±1.0	µA
I_{CC1}	V_{CC} Active Read Current	CE# = V_{IL}, OE# = V_{IH}, Address switching@ 5 MHz, $V_{CC} = V_{CC}$ max		55	60	mA
I_{CC2}	V_{CC} Intra-Page Read Current	CE# = V_{IL}, OE# = V_{IH}, Address switching@ 33 MHz, $V_{CC} = V_{CC}$ max		9	25	mA
I_{CC3}	V_{CC} Active Erase/Program Current[1,2]	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC}$ max		45	100	mA
I_{CC4}	V_{CC} Standby Current	CE#, RESET#, OE# = V_{IH}, $V_{IH} = V_{IO}$ $V_{IL} = V_{SS}$, $V_{CC} = V_{CC}$ max		70	100	µA

Table 18: DC Characteristics (-40°C to +85°C) (continued)

Parameter	Description	Test Conditions	Min	Typ[2]	Max	Unit
I_{CC5}	V_{CC} Reset Current[2,7]	CE# = V_{IH}, RESET# = V_{IL}, V_{CC} = V_{CC} max		10	20	mA
I_{CC6}	Automatic Sleep Mode[3]	V_{IH} = V_{IO}, V_{IL} = V_{SS} , V_{CC} = V_{CC} max, t_{ACC} + 30 ns		3	6	mA
		V_{IH} = V_{IO}, V_{IL} = V_{SS}, V_{CC} = V_{CC} max, t_{ASSB}		100	150	µA
I_{CC7}	V_{CC} Current during power up[2,6]	RESET# = V_{IO}, CE# = V_{IO}, OE# = V_{IO}, V_{CC} = V_{CC} max,		53	80	mA
V_{IL}	Input Low Voltage[4]		-0.5		0.3 x V_{IO}	V
V_{IH}	Input High Voltage[4]		0.7 x V_{IO}		V_{IO} + 0.4	V
V_{OL}	Output Low Voltage[4,8]	I_{OL} = 100 µA for DQ15-DQ0; IOL = 2 mA for RY/BY#			0.15 x V_{IO}	V
V_{OH}	Output High Voltage[4]	I_{OH} = 100 µA	0.85 x V_{IO}			V
V_{LKO}	Low V_{CC} Lock-Out Voltage[2]		2.25		2.5	V
V_{RST}	Low V_{CC} Power on Reset Voltage[2]			1.0		V

Notes:

1. I_{CC} active while Embedded Algorithm is in progress.
2. Not 100% tested.
3. Automatic sleep mode enables the lower power mode when addresses remain stable for the specified designated time.
4. V_{IO} = 1.65V to V_{CC} or 2.7V to V_{CC} depending on the model.
5. V_{CC} = 3V and V_{IO} = 3V or 1.8V. When V_{IO} is at 1.8V, I/O pins cannot operate at >1.8V.
6. During power-up there are spikes of current demand, the system needs to be able to supply this current to insure the part initializes correctly.
7. If an embedded operation is in progress at the start of reset, the current consumption will remain at the embedded operation specification until the embedded operation is stopped by the reset. If no embedded operation is in progress when reset is started, or following the stopping of an embedded operation, I_{CC5} will be drawn during the remainder of t_{RPH}. After the end of t_{RPH} the device will go to standby mode until the next read or write.
8. The recommended pull-up resistor for RY/BY# output is 5k to 10k Ohms.

9.5 Capacitance Characteristics

Table 19: Connector Capacitance for FBGA (LAE) Package

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	7	8	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	5	6	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	3	7	pF
RY/BY#	Output Capacitance	$V_{OUT} = 0$	3	4	pF

Notes:

1. Sampled, not 100% tested.

2. Test conditions $T_A = 25°C$, f = 1.0 MHz.

10 Timing Specifications

10.1 AC Test Conditions

Figure 7: Test Setup
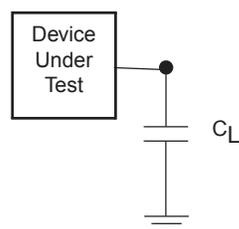
Table 20: Test Specification

Parameter	All Speeds	Units
Output Load Capacitance, CL	30	pF
Input Rise and Fall Times[1]	1.5	ns
Input Pulse Levels	0.0-V_{IO}	V
Input timing measurement reference levels	$V_{IO}/2$	V
Output timing measurement reference levels	$V_{IO}/2$	V

Note: 1. Measured between V_{IL} max and V_{IH} min.

Figure 8: Input Waveforms and Measurement Levels

10.2 Power-On Reset (POR) and Warm Reset

Normal precautions must be taken for supply decoupling to stabilize the V_{CC} and V_{IO} power supplies. Each device in a system should have the V_{CC} and V_{IO} power supplies decoupled by a suitable capacitor close to the package connections (this capacitor is generally on the order of 0.1 µF).

Table 21: Power ON and Reset Parameters

Parameter	Description	Limit	Value	Unit
t_{VCS}	V_{CC} Setup Time to first access[1,2]	Min	300	µs
t_{VIOS}	V_{IO} Setup Time to first access[1,2]	Min	300	µs
t_{RPH}	RESET# Low to CE# Low	Min	35	µs
t_{RP}	RESET# Pulse Width	Min	200	ns
t_{RH}	Time between RESET# (High) and CE# (low)	Min	50	ns
t_{CEH}	CE# Pulse Width High	Min	20	ns

Table 21: Power ON and Reset Parameters (continued)

Notes:

1. Not 100% tested.
2. Timing measured from V_{CC} reaching V_{CC} minimum and V_{IO} reaching V_{IO} minimum to V_{IH} on Reset and V_{IL} on CE#.
3. RESET# Low is optional during POR. If RESET is asserted during POR, the later of t_{RPH}, t_{VIOS}, or t_{VCS} will determine when CE# may go Low. If RESET# remains Low after t_{VIOS}, or t_{VCS} is satisfied, t_{RPH} is measured from the end of t_{VIOS}, or t_{VCS}. RESET must also be High t_{RH} before CE# goes Low.
4. $V_{CC} \geq V_{IO}$ - 200 mV during power-up.
5. V_{CC} and V_{IO} ramp rate can be non-linear.
6. Sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.

10.2.1   Power-On (Cold) Reset (POR)

During the rise of power supplies the V_{IO} supply voltage must remain less than or equal to the V_{CC} supply voltage. V_{IH} also must remain less than or equal to the V_{IO} supply.

The Cold Reset Embedded Algorithm requires a relatively long, hundreds of µs, period (t_{VCS}) to load all of the EAC algorithms and default state from non-volatile memory. During the Cold Reset period all control signals including CE# and RESET# are ignored. If CE# is Low during t_{VCS} the device may draw higher than normal POR current during t_{VCS} but the level of CE# will not affect the Cold Reset EA. CE# or OE# must transition from High to Low after t_{VCS} for a valid read or write operation. RESET# may be High or Low during t_{VCS}. If RESET# is Low during t_{VCS} it may remain Low at the end of t_{VCS} to hold the device in the Hardware Reset state. If RESET# is High at the end of t_{VCS} the device will go to the Standby state.

When power is first applied, with supply voltage below V_{RST} then rising to reach operating range minimum, internal device configuration and warm reset activities are initiated. CE# is ignored for the duration of the POR operation (t_{VCS} or t_{VIOS}). RESET# Low during this POR period is optional. If RESET# is driven Low during POR it must satisfy the Hardware Reset parameters t_{RP} and t_{RPH}. In which case the Reset operations will be completed at the later of t_{VCS} or t_{VIOS} or t_{RPH}.

During Cold Reset the device will draw I_{CC7} current.

Figure 9: Power-Up Diagram
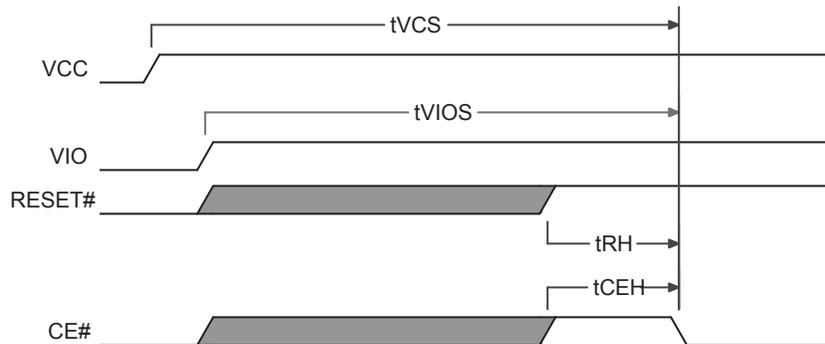
10.2.2   Hardware (Warm) Reset

During Hardware Reset (t_{RPH}) the device will draw ICC5 current.

When RESET# continues to be held at V_{SS}, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL}, but not at V_{SS}, the standby current is greater.

If a Cold Reset has not been completed by the device when RESET# is asserted Low after t_{VCS}, the Cold Reset# EA will be performed instead of the Warm RESET#, requiring t_{VCS} time to complete.

See Figure 10: Hardware Reset (page 54).

After the device has completed POR and entered the Standby state, any later transition to the Hardware Reset state will initiate the Warm Reset Embedded Algorithm. A Warm Reset is much shorter than a Cold Reset, taking tens of µs (t_{RPH}) to complete. During the Warm Reset EA, any in progress Embedded Algorithm is stopped and the EAC is returned to its POR state without reloading EAC algorithms from non-volatile memory. After the Warm Reset EA completes, the interface will remain in the Hardware Reset state if RESET# remains Low. When RESET# returns High the interface will transit to the Standby state. If RESET# is High at the end of the Warm Reset EA, the interface will directly transit to the Standby state.

If POR has not been properly completed by the end of t_{VCS}, a later transition to the Hardware Reset state will cause a transition to the Power-on Reset interface state and initiate the Cold Reset Embedded Algorithm. This ensures the device can complete a Cold Reset even if some aspect of the system Power-On voltage ramp-up causes the POR to not initiate or complete correctly. The RY/BY# pin is Low during cold or warm reset as an indication that the device is busy performing reset operations. Hardware Reset is initiated by the RESET# signal going to V_{IL}.

*Advanced information. Subject to change without notice.

Figure 10: Hardware Reset
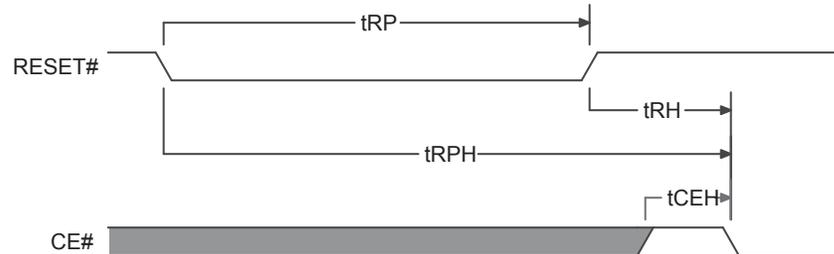
10.3 AC Characteristics

10.3.1 Asynchronous Read Operations

Table 22: Read Operation $V_{IO} = V_{CC} = 2.7V$ to $3.6V$ ($-40°C$ to $+85°C$)

Parameter		Description		Test Setup		Speed Option			Unit
JEDEC	Std					90	100	110	
t_{AVAV}	t_{RC}	Read Cycle Time[1]		128 Mb, 256 Mb	Min	90	100		ns
				512 Mb, 1 Gb			100	110	
t_{AVQV}	t_{ACC}	Address to Output Delay	CE# = V_{IL} OE# = V	128 Mb, 256 Mb	Max	90	100		ns
				512 Mb, 1 Gb			100	110	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	OE# = V_{IL}	128 Mb, 256 Mb	Max	90	100		ns
				512 Mb, 1 Gb			100	110	
	t_{PACC}	Page Access Time		128 Mb, 256 Mb	Max	15	20		ns
				512 Mb, 1 Gb			15	20	
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	25			ns
t_{AXQX}	t_{OH}	Output Hold time from addresses, CE# or OE#, Whichever Occurs First			Min	0			ns
t_{EHQZ}	t_{DF}	Chip Enable or Output Enable to Output High-Z[1]			Max	15			ns
	t_{OEH}	Output Enable Hold Time[1]	Read		Min	0			ns
			Toggle and Data# Polling		Min	10			ns
	t_{ASSB}	Automatic Sleep to Standby time[1]		CE# = V_{IL}, Address stable	Typ	5			µs
					Max	8			µs

Note: 1. Not 100% tested.

Table 23: Read Operation V_{IO} = 1.65V to V_{CC}, V_{CC} = 2.7V to 3.6V (-40°C to +85°C)

| Parameter | | Description | | Test Setup | | Speed Option | | | Unit |
JEDEC	Std					90	100	110	
t_{AVAV}	t_{RC}	Read Cycle Time[1]		128 Mb, 256 Mb	Min	100	110		ns
				512 Mb, 1 Gb			110	120	
t_{AVQV}	t_{ACC}	Address to Output Delay	CE# = V_{IL} OE# = V_{IL}	128 Mb, 256 Mb	Max	100	110		ns
				512 Mb, 1 Gb			110	120	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	OE# = V_{IL}	128 Mb, 256 Mb	Max	100	110		ns
				512 Mb, 1 Gb			110	120	
	t_{PACC}	Page Access Time		128 Mb, 256 Mb	Max	25	30		ns
				512 Mb, 1 Gb			25	30	
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	35			ns
t_{AXQX}	t_{OH}	Output Hold time from addresses, CE# or OE#, Whichever Occurs First			Min	0			ns
t_{EHQZ}	t_{DF}	Chip Enable or Output Enable to Output High-Z[1]			Max	20			ns
	t_{OEH}	Output Enable Hold Time[1]	Read		Min	0			ns
			Toggle and Data# Polling		Min	10			ns
	t_{ASSB}	Automatic Sleep to Standby time[1]		CE# = V_{IL}, Address stable	Typ	5			µs
					Max	8			µs

Note: 1. Not 100% tested.

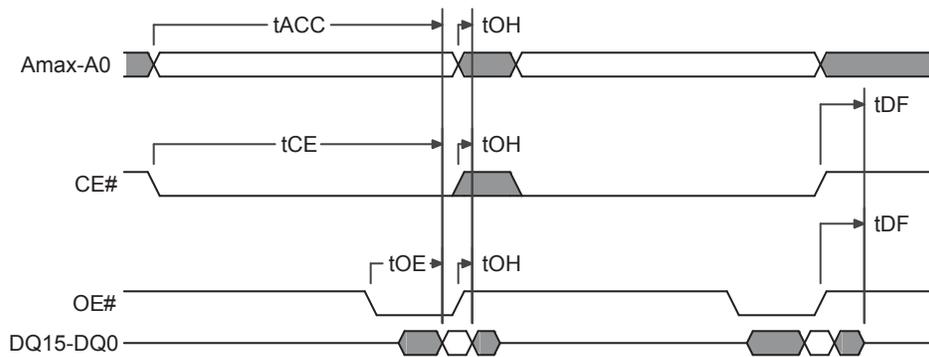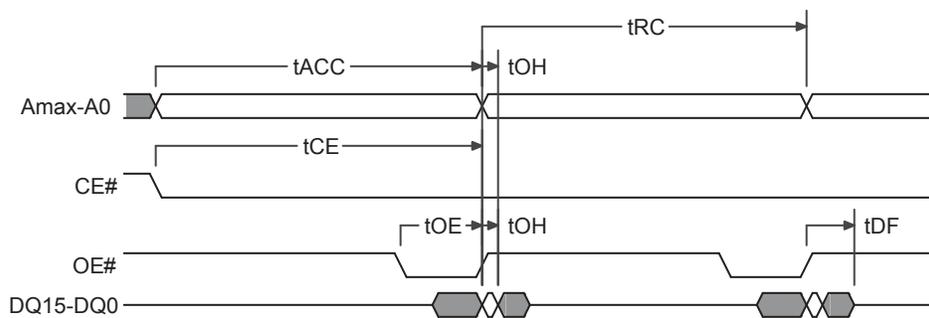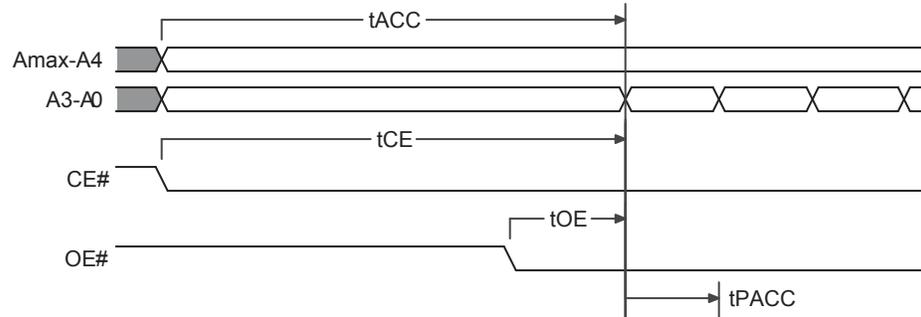Figure 11: Back to Back Read (t_{ACC}) Operation Timing Diagram

Figure 12: Back to Back Read Operation (t_{RC})Timing Diagram

Note: Back to Back operations, in which CE# remains Low between accesses, requires an address change to initiate the second access.

Figure 13: Page Read Timing Diagram

Note: Word Configuration: Toggle A0, A1, A2, and A3.

10.3.2   Asynchronous Write Operations

Parameter		Description		$V_{IO} = 2.7V$ to V_{CC}	$V_{IO} = 1.65V$ to V_{CC}	Unit
JEDEC	Std					
t_{AVAV}	t_{WC}	Write Cycle Time[1]	Min	60		ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0		ns
	t_{ASO}	Address Setup Time to OE# Low during toggle bit polling	Min	15		ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45		ns
	t_{AHT}	Address Hold Time From CE# or OE# High during toggle bit polling	Min	0		ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	30		ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0		ns
	t_{OEPH}	Output Enable High during toggle bit polling or following status register read.	Min	20		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0		ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0		ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0		ns
t_{WLWH}	t_{WP}	WE# Pulse Width	Min	25		ns
t_{WHWL}	t_{WPH}	WE# Pulse Width High	Min	20		ns

Note: 1. Not 100% tested.

*Advanced information. Subject to change without notice.
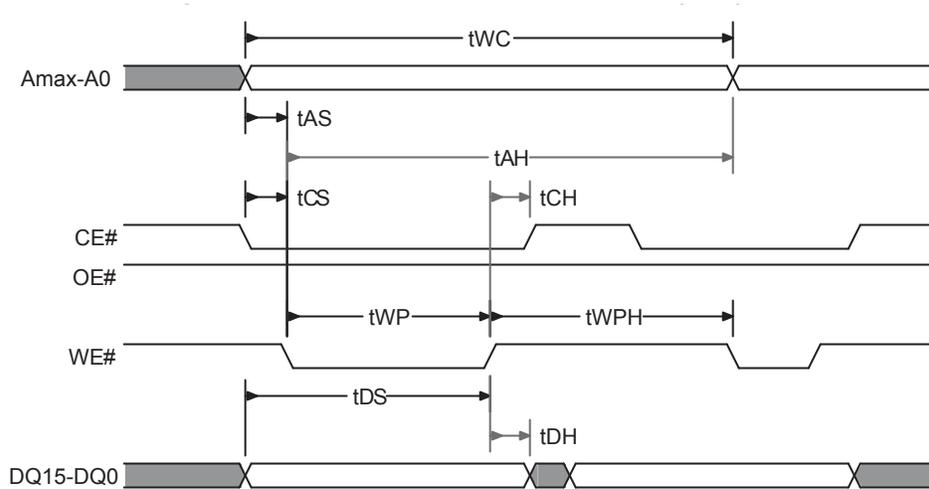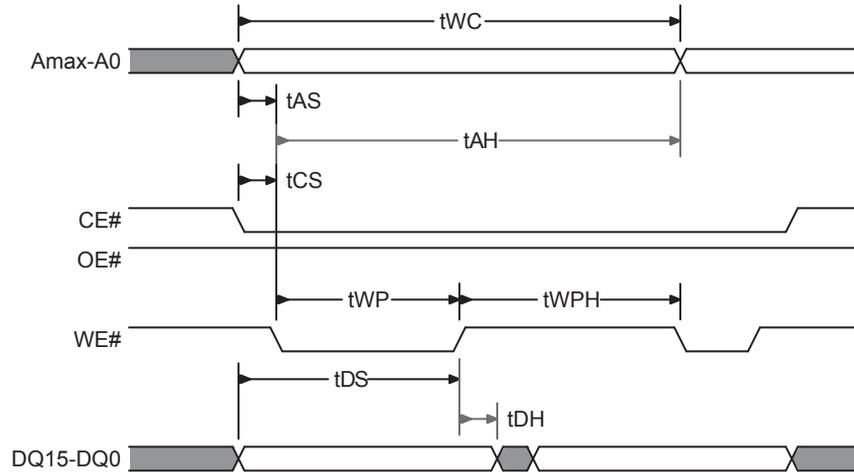
Table 24: Back to Back Write Operation Timing Diagram

Figure 14: Back to Back (CE#V$_{IL}$) Write Operation Timing Diagram

Figure 15: Write to Read (t_{ACC}) Operation Timing Diagram
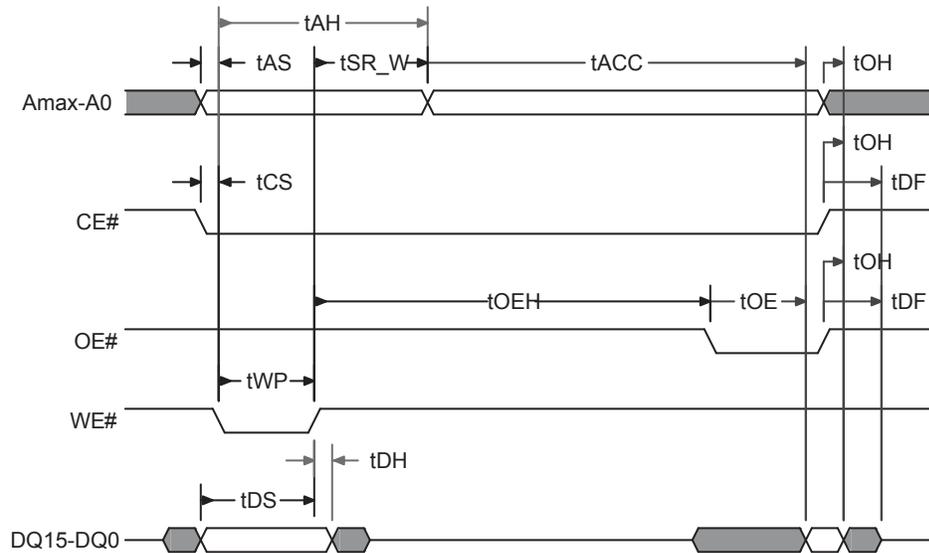
Figure 16: Write to Read (t_{CE}) Operation Timing Diagram
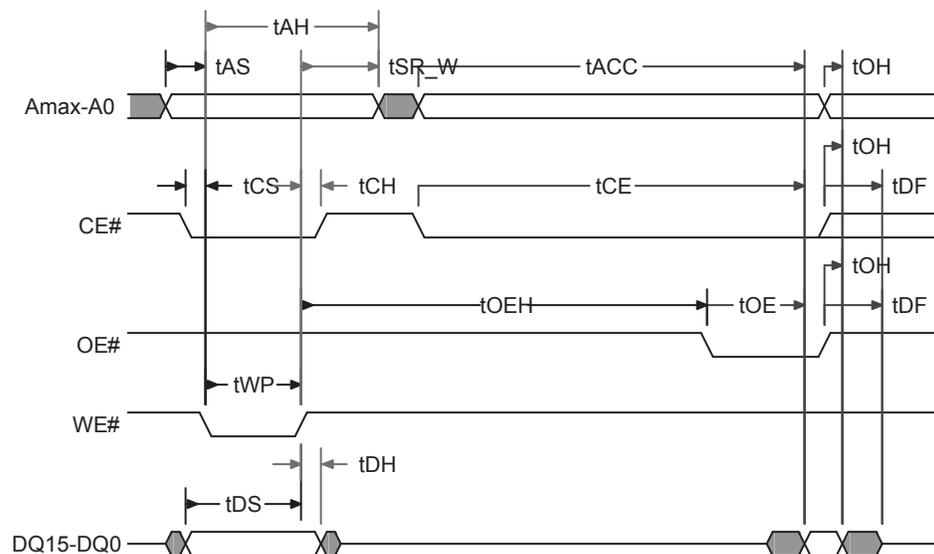
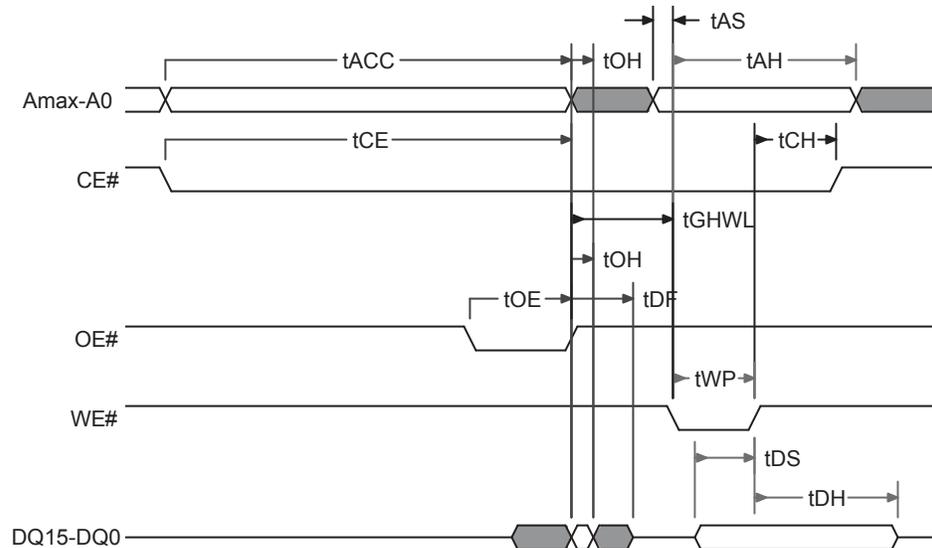Figure 17: Read to Write (CE# V_IL) Operation Timing Diagram

Figure 18: Read to Write (CE# Toggle) Operation Timing Diagram

Table 25: Erase/Program Operations
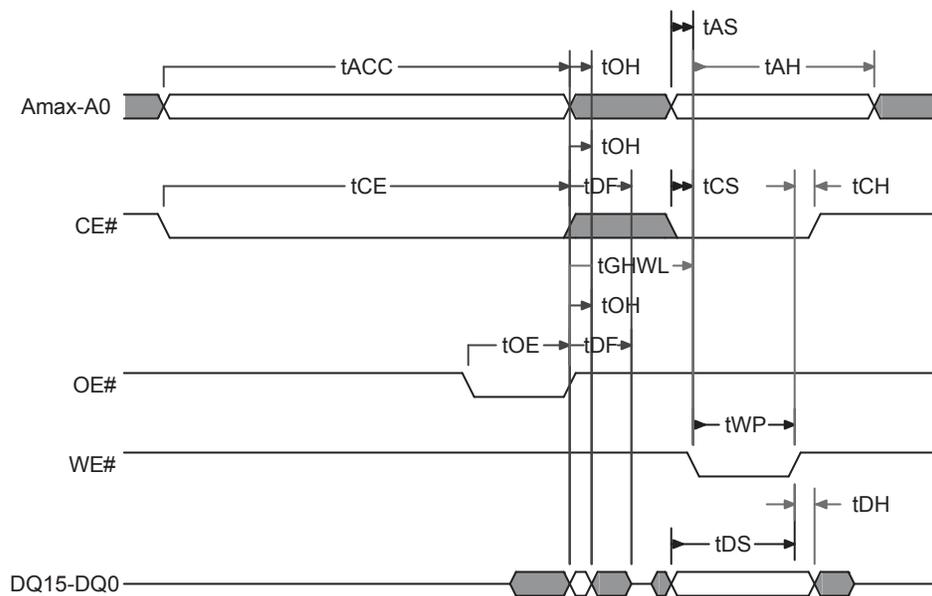
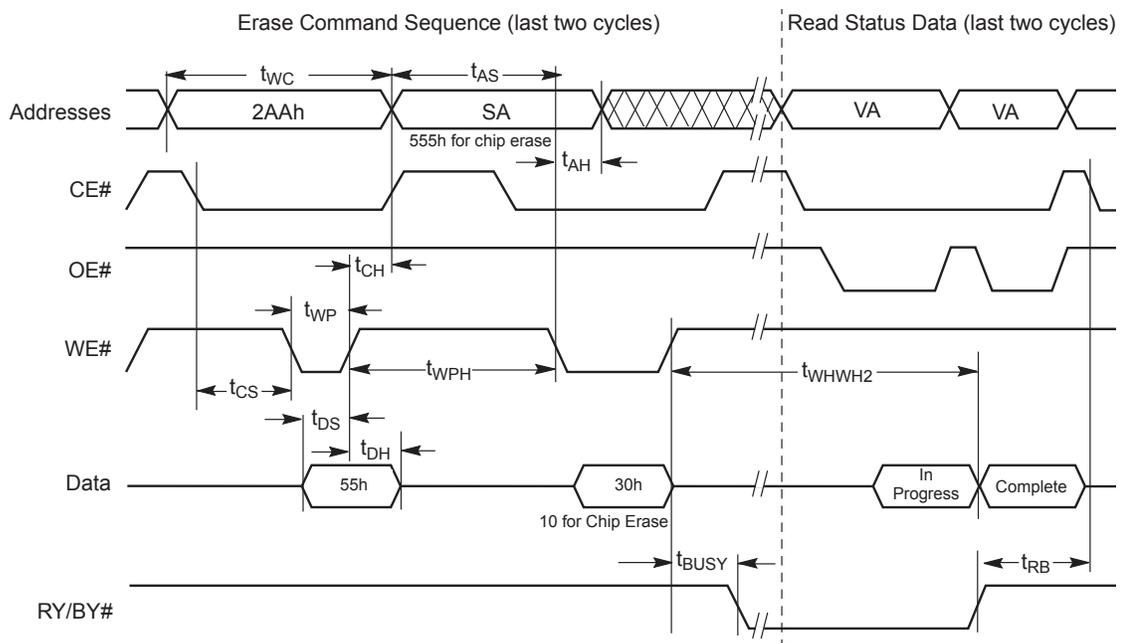| Parameter		Description		V_{IO} = 2.7V to V_{CC}	V_{IO} = 1.65V to V_{CC}	Unit
JEDEC	Std					
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation	Typ	Note 3		µs
		Effective Write Buffer Program Operation per Word	Typ	Note 3		µs
		Program Operation per Word or Page	Typ	Note 3		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation[1]	Typ	Note 3		ms
	t_{BUSY}	Erase/Program Valid to RY/BY# Delay	Max	80		ns
	$t_{SR/W}$	Latency between Read and Write operations[2]	Min	10		ns
	t_{ESL}	Erase Suspend Latency	Max	Note 3		µs
	t_{PSL}	Program Suspend Latency	Max	Note 3		µs
	t_{RB}	RY/BY# Recovery Time	Min	0		µs

Notes:

1. Not 100% tested.

2. Upon the rising edge of WE#, must wait $t_{SR/W}$ before switching to another address.

3. See Table 6: Embedded Algorithm Characteristics (-40°C to +85°C) (page 27) for specific values.

Figure 19: Program Operation Timing Diagram
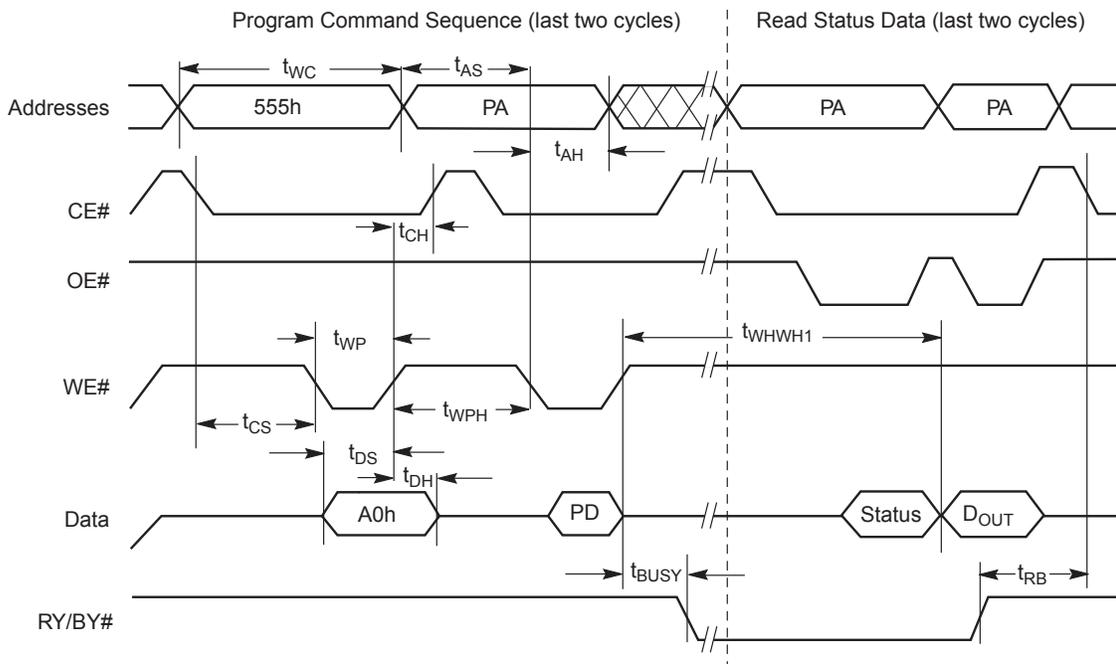
Note: 1. PA = program address, PD = program data, D$_{OUT}$ is the true data at the program address.

Figure 20: Chip/Sector Erase Operation Timing Diagram

Note: 1. SA = sector address (for sector erase), VA = valid address for reading status data.

10.3.3 Alternate CE# Controlled Write Operations

Table 26: Alternate CE# Controlled Write Operations

Parameter		Description		V_{IO} = 2.7V to V_{CC}	V_{IO} = 1.65V to V_{CC}	Unit
JEDEC	Std					
t_{AVAV}	t_{WC}	Write Cycle Time[1]	Min	60		ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0		ns
	t_{ASO}	Address Setup Time to OE# Low during toggle bit polling	Min	15		ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45		ns
	t_{AHT}	Address Hold Time From CE# or OE# High during toggle bit polling	Min	0		ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	30		ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0		ns
	t_{CEPH}	CE# High during toggle bit polling	Min	20		ns
	t_{OEPH}	OE# High during toggle bit polling	Min	20		ns
t_{GHEK}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0		ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0		ns
t_{ELWH}	t_{WH}	WE# Hold Time	Min	0		ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	25		ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	20		ns

Note: 1. Not 100% tested.

Figure 21: Back to Back (CE#) Write Operation Timing Diagram
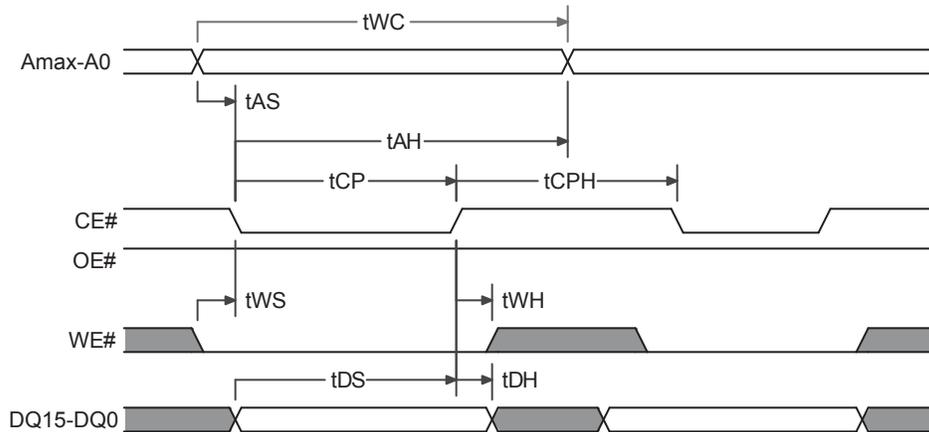
Figure 22: (CE#) Write to Read Operation Timing Diagram

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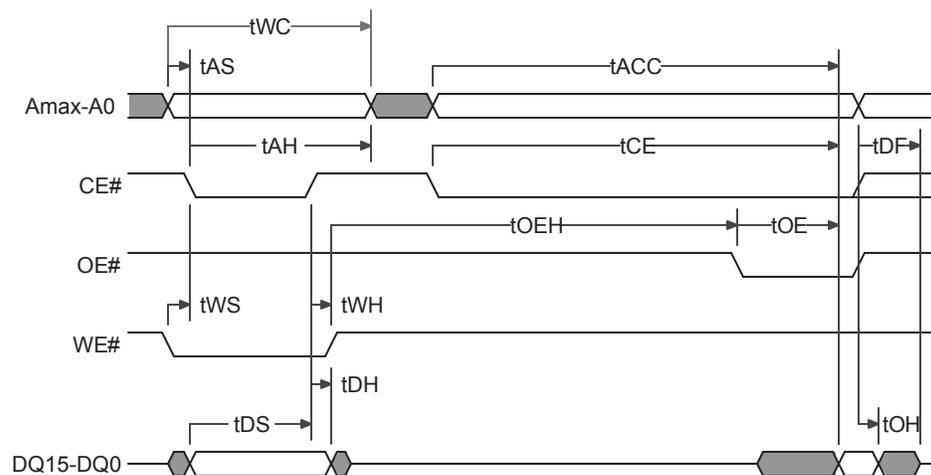
11   Physical Interface

11.1   Connection Diagram

Figure 23: 64-ball Fortified Ball Grid Array - Product Pinout (Top View)
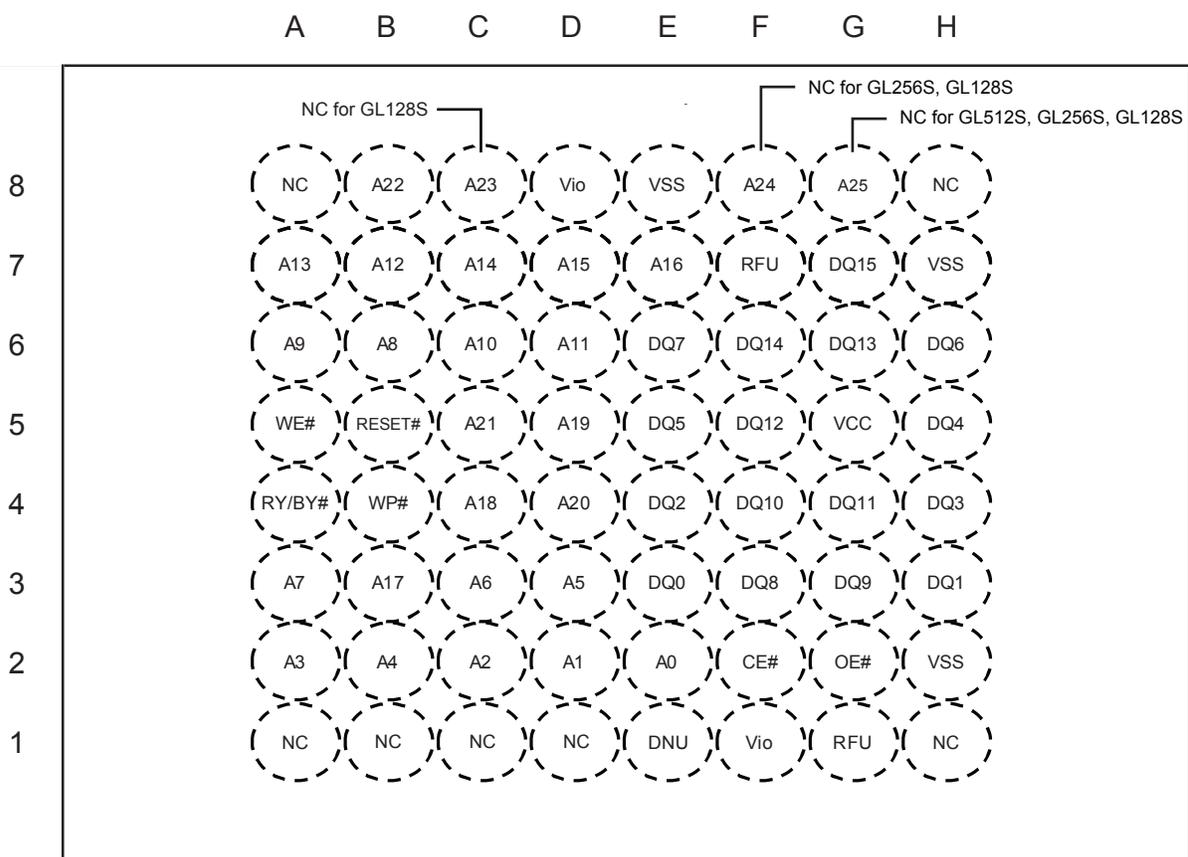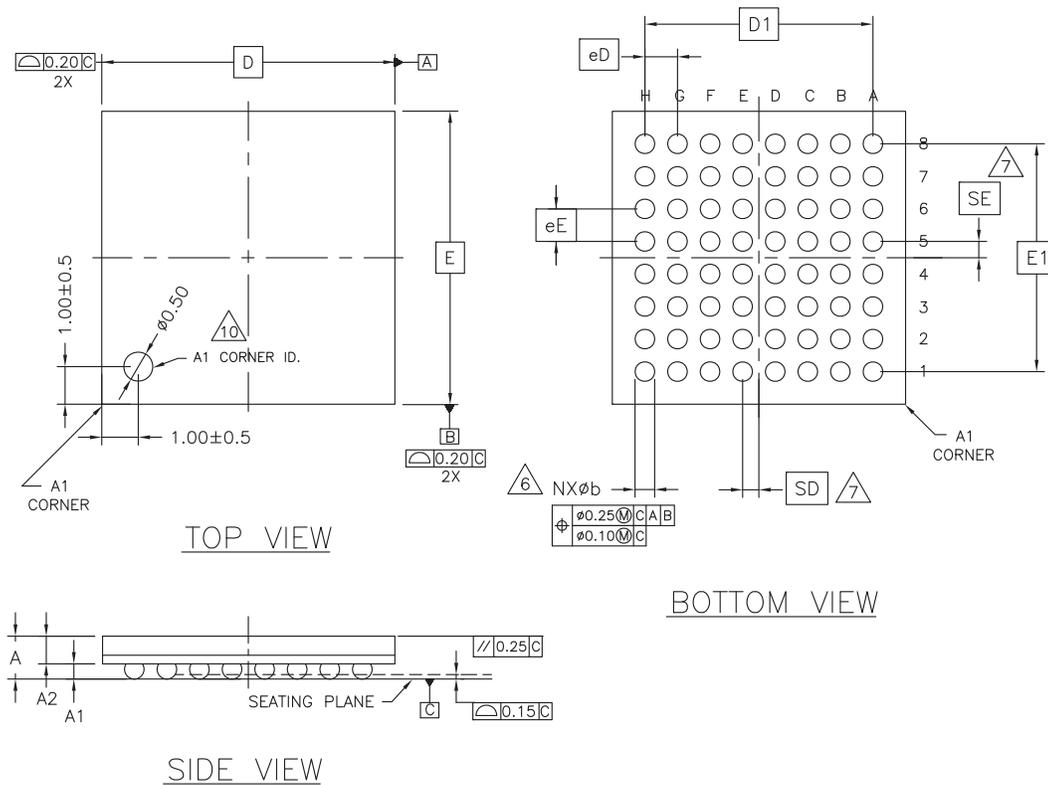

Notes:

1. Ball E1, Do Not Use (DNU), a device internal signal is connected to the package connector. The connector may be used by the OCM for test or other purposes and is not intended for connection to any host system signal. Do not use these connections for PCB Signal routing channels. Though not recommended, the ball can be connected to V_{CC} or V_{SS} through a series resistor.

2. Balls F7 and G1, Reserved for Future Use (RFU).

3. Balls A1, A8, C1, D1, H1, and H8, No Connect (NC).

Advanced information. Subject to change without notice.

11.2 Physical Diagram – LAE064

Figure 24: LAE064 - 64-ball Fortified Ball Grid Array (FBGA), 9 x 9 mm

TOP VIEW

BOTTOM VIEW

SIDE VIEW

PACKAGE	LAE 064			
JEDEC	N/A			
	9.00 mm x 9.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.40	PROFILE HEIGHT
A1	0.40	---	---	STANDOFF
A2	0.60	---	---	BODY THICKNESS
D	9.00 BSC.			BODY SIZE
E	9.00 BSC.			BODY SIZE
D1	7.00 BSC.			MATRIX FOOTPRINT
E1	7.00 BSC.			MATRIX FOOTPRINT
MD	8			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
N	64			BALL COUNT
b	0.50	0.60	0.70	BALL DIAMETER
eD	1.00 BSC.			BALL PITCH - D DIRECTION
eE	1.00 BSC.			BALL PITCH - E DIRECTION
SD / SE	0.50 BSC.			SOLDER BALL PLACEMENT
?	NONE			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010? EXCEPT AS NOTED).

4. $\boxed{e}$ REPRESENTS THE SOLDER BALL GRID PITCH.

5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.

   N IS THE TOTAL NUMBER OF SOLDER BALLS.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN ? THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = $\boxed{e/2}$

8. NOT USED.

9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

3623 \ 16-038.12 \ 1.16.07

Form #: CSI-D-685 Document 001

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12   Ordering Information

Table 27: Ordering Information

Part Number	Device Grade
MYX29GL01GS11DPIV2BG-ITRL	Industrial

For more information, contact a Micross sales representative at sales@micross.com.

*Advanced information. Subject to change without notice.

Document Title

1Gbit - 64M x 16 GL-S MirrorBit© Eclipse™ Flash Memory

Revision History

Revision #	History	Release Date	Status
1.0	Initial Release	January 23, 2015	Preliminary