DEVELOPMENT KIT
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DR8000

916.50 MHz Transceiver Module

- ***4.8Designed for Short-Range Wireless Data Communications***
- ***Supports RF Data Transmission Rates Up to 115.2 kbps***
- ***3 V, Low Current Operation plus Sleep Mode***
- ***Up to 10 mW Transmitter Power***

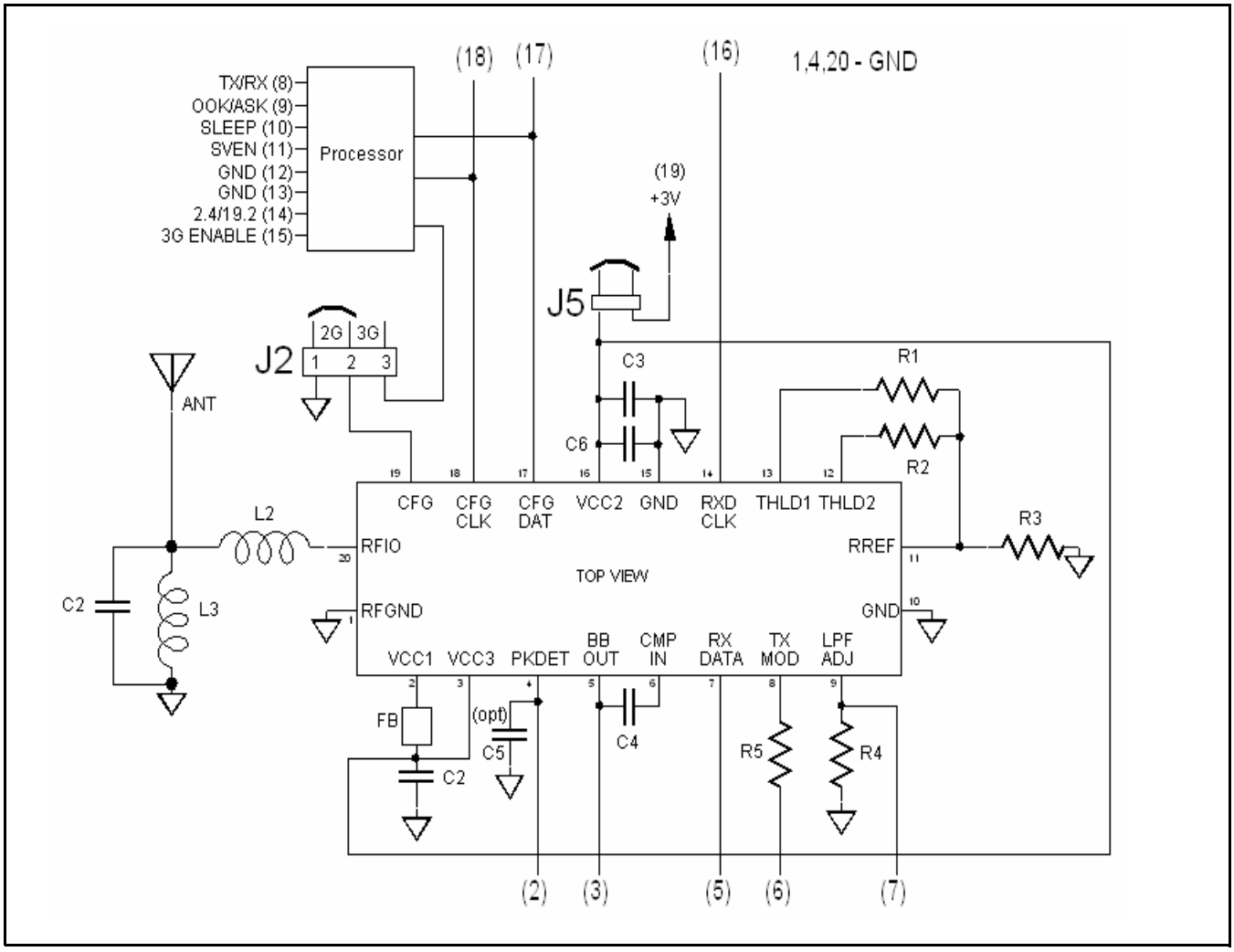
The DR8000 hybrid transceiver module is ideal for short-range wireless data applications where robust operation, small size, low power consumption and low cost are required. The DR8000 utilizes RFM's TR8000 amplifier-sequenced hybrid (ASH) architecture to achieve this unique blend of characteristics. All critical RF functions are contained in the hybrid, simplifying and speeding design-in. The receiver section of the DR8000 is sensitive and stable. A wide dynamic range log detector, in combination with digital AGC and a compound data slicer, provide robust performance in the presence of on-channel interference or noise. Two stages of SAW filtering provide excellent receiver out-of-band rejection. The transmitter includes provisions for both on-off keyed (OOK) and amplitude-shift keyed (ASK) modulation. The transmitter employs SAW filtering to suppress output harmonics, facilitating compliance with FCC and similar regulations.

Absolute Maximum Ratings

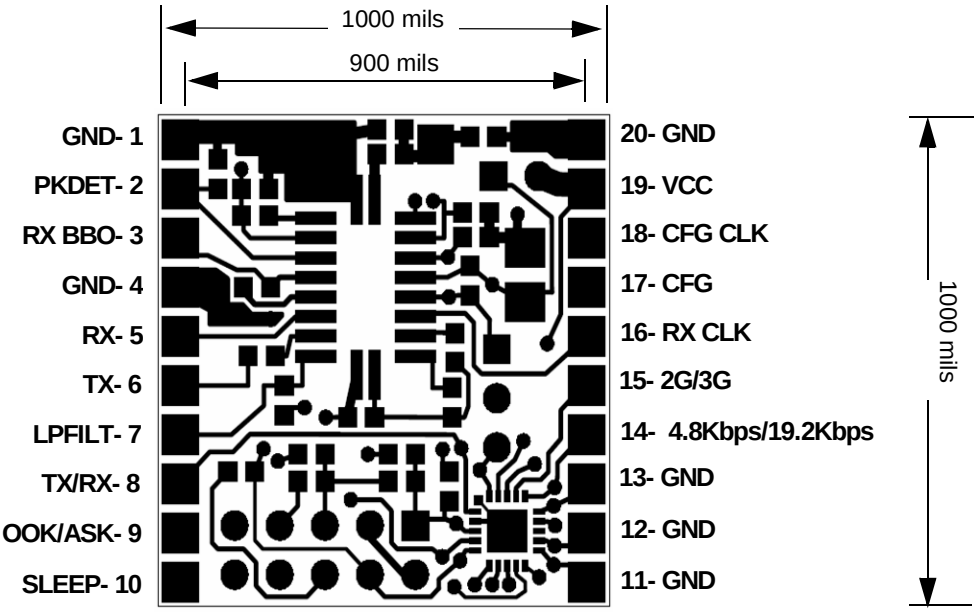
Rating	Value	Units
Power Supply and All Input/Output Pins	**-0.3 to +4.0**	**V**
Non-Operating Case Temperature	**-50 to +100**	**°C**
Soldering Temperature (10 seconds, 5 cycles maximum)	**260**	**°C**

Electrical Characteristics

Characteristic	Sym	Notes	Minimum	Typical	Maximum	Units
Operating Frequency	f_o		916.30		916.70	MHz
Data Modulation Type				OOK/ASK		
OOK Data Rate					30	kb/s
ASK Data Rate					115.2	kb/s
Receiver Performance (OOK @ 4.8kbps)						
Sensitivity, 4.8 kbps, 10-3 BER, AM Test Method				-108		dBm
Input Current, 4.8 kbps, 3.0V Supply				4.2		mA
Sensitivity, 19.2 kbps, 10-3 BER, AM Test Method				-104		dBm
Input Current, 19.2 kbps, 3.0V Supply				4.25		mA
Transmitter Performance (OOK @ 4.8kbps)						
Peak RF Output Power, 315 µA TXMOD Current	P_{OL}			10		dBm
Peak Current, 315 µA TXMOD Current	I_{TPL}			32		mA
OOK Turn On/Turn Off Times	t_{ON}/t_{OFF}				12/6	µs
ASK Output Rise/Fall Times	t_{TR}/t_{TF}				1.1/1.1	µs
Power Supply Voltage Range (including I/O)	Vcc		2.2		3.7	Vdc
Operating Ambient Temperature	T_A		-40		+85	°C
Power Supply Voltage Ripple					10	mVp-p



DR8000 Pinout and Dimensions



Pin Descriptions

Pin	Name	In/Out	Description
1,4,20	GND	-	GND is the ground pin.
19	VCC	-	VCC is a positive supply voltage pin.
2	PKDET	Out	This pin is the peak detector output. A 0.022uF capacitor to ground (C5) sets the peak detector attack and decay times, which have a fixed 1:1000 ratio. For most applications, these time constants should be coordinated with the base-band time constant. For a given base-band capacitor C_{BBO} , the capacitor value C_{PKD} is: $C_{PKD} = 2.0* C_{BBO}$, where C_{BBO} and C_{PKD} are in pF A ±10% ceramic capacitor should be used at this pin. This time constant will vary between t_{PKA} and 1.5* t_{PKA} with variations in supply voltage, temperature, etc. The capacitor is driven from a 200 ohm "attack" source, and decays through a 200 K load. The peak detector is used to drive the "dB-below-peak" data slicer and the AGC release function. The peak detector capacitor is discharged in the receiver power-down (sleep) mode and in the transmit modes. See the description of Pin 3 below for further information. **A 0.022uF capacitor is installed for operation at 4.8kbps.**
3	BBOUT	Out	This pin is connected directly to the transceiver BBOUT pin. This pin drives the CMPIN pin through a coupling capacitor, C_{BBO} = 0.01uF (C4), for internal data slicer operation at 4.8kbps. $C_{BBO} = 11.2*SP_{MAX}$, where SP_{MAX} is the maximum signal pulse width in µs and C_{BBO} is in pF The nominal output impedance of this pin is 1 K.The BBOUT signal changes about 10 mV/dB, with a peak-to-peak signal level of up to 450 mV. The signal at BBOUT is riding on a 1.5 Vdc value that varies somewhat with supply voltage and temperature, so it should be coupled through a capacitor to an external load. When an external data recovery process is used with AGC, BBOUT must be coupled to the external data recovery process and CMPIN by separate series coupling capacitors. The output impedance of this pin becomes very high in sleep mode, preserving the charge on the coupling capacitor. The value of C3 on the circuit board has been chosen to match typical data encoding schemes at 4.8 kbps. If C4 is modified to support higher data rates and/or different data encoding schemes and PK DET is being used, make the value of the peak detector capacitor C5 about 2x the value of C_{BBO}.
5	RXDATA	Out	RXDATA is the receiver data output pin. It is a CMOS output. The signal on this pin can come from one of two sources. The default source is directly from the output of the data slicer circuit. The alternate source is from the radio's internal data and clock recovery circuit. When the internal data and clock recovery circuit is used, the signal on RXDATA is switched from the output of the data slicer to the output of the data and clock recovery circuit when a packet start symbol is detected. Each recovered data bit is then output on the rising edge of a RXDCLK pulse (Pin 16), and is stable for reading on the falling edge of the RXDCLK pulse.
6	TXMOD	In	The transmitter RF output voltage is proportional to the input current to this pin. A resistor in series with the TXMOD input is normally used to adjust the peak transmitter output. Full transmitter power (10 mW) requires about 315 µA of drive current. The transmitter output power P_O for a 3 Vdc supply voltage is approximately: $PO = 101*(I_{TXM})^2$, where PO is in mW and the modulation current I_{TXM} is in mA The practical power control range is 10 to -50 dBm. A ±5% TXMOD resistor value is recommended. Internally, this pin is connected to the base of a bipolar transistor with a small emitter resistor. The voltage at the TXMOD input pin is about 0.87 volt with 315 uA of drive current. This pin accepts analog modulation and can be driven with either logic level data pulses (unshaped) or shaped data pulses. **A series 6.2 kilohm resistor is installed to provide +10dBm average output power with a +3Vdc input.**
7	LPFADJ	In	This pin is the receiver low-pass filter bandwidth adjust. The filter bandwidth is set by a resistor R_{LPF} (R4) between this pin and ground. The resistor value can range from 510 K to 3 K, providing a filter 3 dB bandwidth f_{LPF} from 5 to 600 kHz. The resistor value is determined by: $R_{LPF} = (0.0006*f_{LPF})^{-1.069}$ where R_{LPF} is in kilohms, and f_{LPF} is in kHz A ±5% resistor should be used to set the filter bandwidth. This will provide a 3 dB filter bandwidth between f_{LPF} and 1.3* f_{LPF} with variations in supply voltage, temperature, etc. The filter provides a three-pole, 0.05 degree equiripple phase response. **A 470 kilohm resistor to GND is installed to provide a 3dB filter bandwidth of 5.275kHz. Connect an external ±1%, 243kilohm resistor to GND for 19.2kbps operation.**
8	TX/RX	In	Logic Input (CMOS compatible). This pin, in 3G mode, selects the operation of the TR8000 . Pull this pin 'High' for Transmit Mode. Pull this pin 'Low' for Receive mode. *Do not allow this pin to float.*
9	OOK/ASK	In	Logic Input (CMOS compatible). This pin, in 3G mode, selects the operation of the TR8000. Pull this pin 'High' for OOK Transmit/Receive mode. Pull this pin 'Low' for ASK Transmit/Receive mode. *Do not allow this pin to float.*

Pin	Name	In/Out	Description
10	SLEEP	In	Logic Input (CMOS compatible). This pin, in 3G mode, puts the TR8000 into Sleep mode. Pull this pin 'High' for Sleep Mode. Pull this pin 'Low' for operation mode. *Do not allow this pin to float.*
11	SVEN	In	Logic Input (CMOS compatible). This pin, in 3G mode, enables the Start Vector Recognition circuit. The TR8000 will not output a recovered clock on RXDCLK (pin 16) until the start vector, 0xE2E2, has been recognized. Pull this pin 'High' to enable Start Vector Recognition. Pull this pin 'Low' then 'High' to reset the Start Vector Recognition circuit. *Do not allow this pin to float.*
12	Not Used		Keep this pin pulled 'Low'.
13	Not Used		Keep this pin pulled 'Low'.
14	4.8KBPS/ 19.2KBPS	In	Logic Input (CMOS compatible). This pin, in 3G mode, selects the receive data rate of the DR8000. Pull this pin 'High' to select 4.8kbps. Pull this pin 'Low' to select 19.2kbps. *Do not allow this pin to float.* **NOTE: Operating at 19.2kbps will require the value of C4, C5 and R4 to change to accommodate the higher data rate. See the TR8000 datasheet for recommended component values.**
15	3G SEL	In	Logic Input (CMOS compatible). This pin sets the processor to operate in 3G mode. The power-up operating configuration of the TR8000 device is controlled by the J2 jumper setting. When DC power is applied to the DR8000 with J2 installed across 2-3, this pin should be pulled 'High' immediately after power-up to initiate 3G mode. Failure to pull pin 15 'High' after power-up will cause the processor to remain inactive. Pulling this pin 'High' wakes the processor for 3G mode operation. When DC power is applied to the DR8000 with J2 installed across 1-2, this pin should be held 'Low' to operate in 2G mode. *Do not allow this pin to float.*
16	RXDCLK	Out	RXDCLK is the clock output from the data and clock recovery circuit. RXDCLK is a CMOS output. When the radio's internal data and clock recovery circuit is not used, RXDCLK is a steady low value. When the internal data and clock recovery is used, RXDCLK is low until a packet start symbol is detected at the output of the data slicer. Each bit following the start symbol is output at RXDATA on the rising edge of a RXDCLK pulse, and is stable for reading on the falling edge of the RXDCLK pulse. Once RXDCLK is activated by the detection of a start symbol, it remains active until SVEN (pin 11) is reset. See Pin 11 description.
17	CFGDAT	In/Out	In 3G control mode, CFGDAT is a bi-directional CMOS logic pin. When CFG (Pin 19) is set to a logic 1, configuration data can be clocked into or out of the radio's configuration registers through CFGDAT using CFGCLK (Pin 18). Data clocked into CFGDAT is transferred to a control register each time a group of 8 bits is received. Pulses on CFGCLK are used to clock configuration data into and out of the radio through CFGDAT. When writing through CFGDAT, a data bit is clocked into the radio on the rising edge of a CFGCLK pulse. When reading through CFGDAT, data is output on the rising edge of the CFGCLK pulse and is stable for reading on the falling edge of the CFGCLK. Refer to the TR8000 datasheet for detailed timing. This pin is a high impedance input (CMOS compatible) in 2G mode. This pin must be held at a logic level. *Do not allow this pin to float.*
18	CFGCLK	In/Out	In 3G control mode, pulses on CFGCLK are used to clock configuration data into and out of the radio through CFGDAT (Pin 17). When writing to CFGDAT, a data bit is clocked into the radio on the rising edge of a CFGCLK pulse. When reading through CFGDAT, data is stable for reading on the falling edge of the CFGCLK. Refer to the TR8000 datasheet for detailed timing. This pin is a high impedance input (CMOS compatible) in 2G mode. *Do not allow this pin to float.*

Theory of Operation

The DR8000 evaluation module is centered around the TR8000 ASH Transceiver. The DR8000 may operate in backward compatible 2G mode, or in the enhanced 3G mode. Since 3G mode requires the use of a serial I/O port to configure internal registers, the module includes an on-board Silicon Labs C8051F330 microcontroller to control access to the serial port. When 2G mode is enabled the microcontroller serves no function. When 3G mode is enabled the microcontroller constantly scans pins 8-15 for a change of logic state. When a state change is detected on one or more of these pins, the microcontroller automatically updates the internal configuration registers via the serial port of the TR8000. The microcontroller assumes full control of the CFG pin, CFGCLK pin, and CFGDAT pin in 3G mode to continuously update the internal registers.

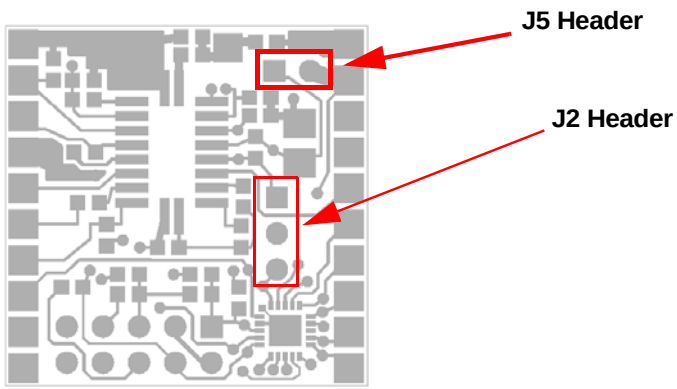
The DR8000 module is designed to demonstrate the performance of the TR8000 ASH Transceiver at 4.8kbps, although other data rates are possible with changes in on-board component values. See pin descriptions and refer to the TR8000 datasheet.

The DR8000 module may be mounted on a prototype assembly using standard 0.1" spacing, 10-pin headers spaced 0.9" apart.

2G Mode Operation

The DR8000 may operate in 2G mode. See pin 15 description and Power-up Mode Select (J2) section for mode select details. In 2G mode, the CFGCLK pin (18) and CFGDAT pin (17) operate as CTRL0 and CTRL1, respectively, just as for second-generation devices. The CFGCLK and CFGDAT pins are a high impedance input allowing external control for 2G configuration. The logic levels on CFGCLK (CTRL0) and CFGDAT (CTRL1) control the default 2G operation as shown below:

CFGCLK (CNTRL0)	CFGDAT (CNTRL1)	MODE
0	0	SLEEP
1	0	TX OOK
0	1	TX ASK
1	1	RX



Current Consumption Monitor (J5)

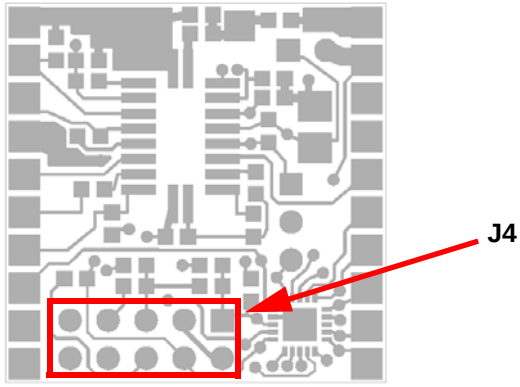
The current consumption of the TR8000 device may be monitored by removing J5 and connecting an ammeter across the terminals. When J5 is removed it isolates the TR8000 from VCC powering the on-board processor to give a true reading of the current consumption of only the TR8000 without the additional current usage of the processor. J5 must be installed to power the TR8000 if not using the header for current measurement.

Power-up Mode Select (J2)

J2 is used to select the operating mode of the TR8000 device **only** at power-up. The state of J2 when VCC is applied will determine whether the board operates in 2G mode or 3G mode. Pin 2 (center pin) of J2 is connected to Pin 19 (CFG) of the TR8000 device and is grounded for 2G mode and functions as the chip select line for the serial interface in 3G mode. Installing the jumper will either connect the CFG pin of the TR8000 to GND or directly to the processor for control in 3G mode. See the table below for power-up jumper settings.

Setting	Power-up Mode	Pin 19
J2(1-2)	2G	Connected to GND
J2(2-3)	3G	Connected to Processor

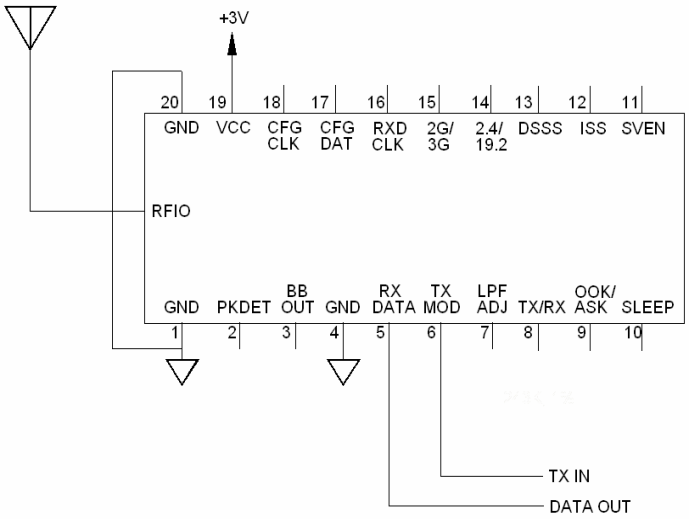
After power-up if 3G mode is selected, pin 15 (3G Sel) must be pulled 'High' to initiate the processor to operate in 3G mode. Failure to pull pin 15 'High' after power-up will cause the processor to remain inactive.



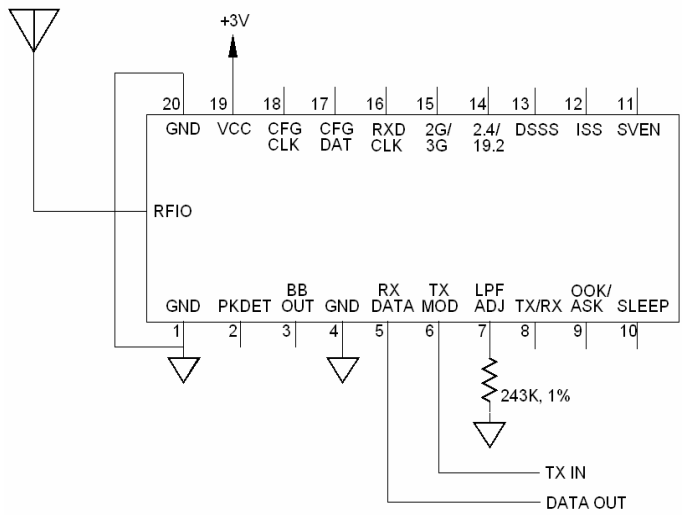
Programming Header (J4)

The programming header allows for custom firmware development for the Silicon Labs C8051F330 if desired. Contact RFM for more information about custom firmware development.

4.8kbps Application Circuit



19.2kbps Application Circuit



Sample Set Ups

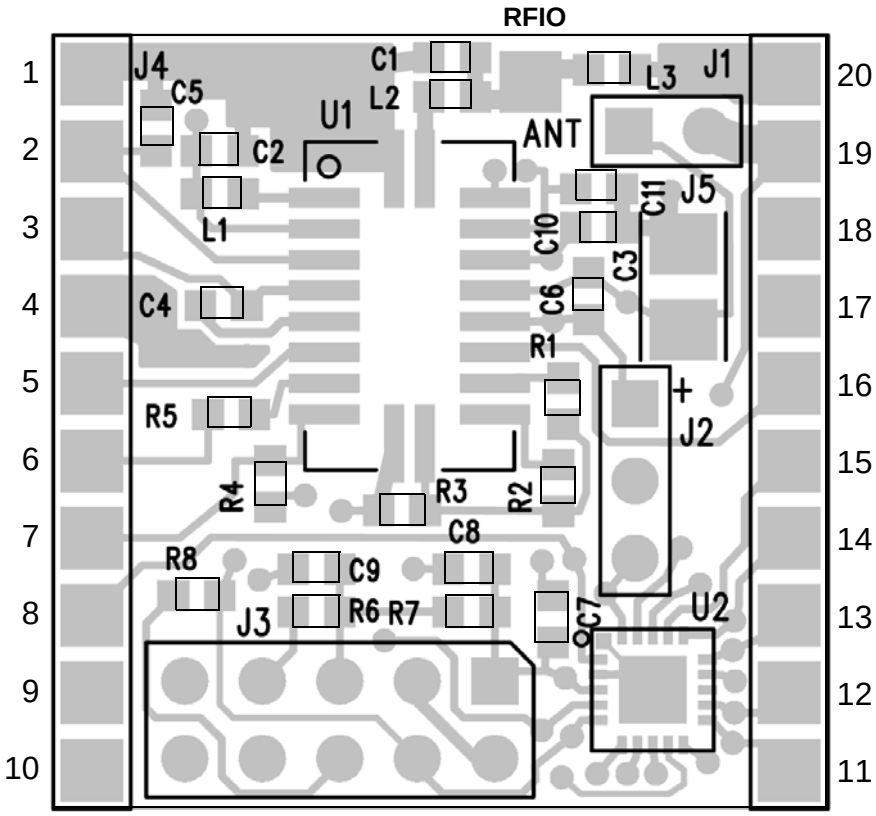
Command	TX/RX (pin 8)	ASK/OOK (pin 9)	SLEEP (pin 10)	SVEN (pin 11)	DSSS (pin 12)	ISS (pin 13)	4.8/19.2 (pin 14)	3G SEL (pin 15)
Receive OOK 4.8kbps	0	0	0	0	0	0	1	1
Receive ASK 4.8kbps	0	1	0	0	0	0	1	1
Receive ASK 19.2kbps (add ext 243K Resistor on pin 7)	0	1	0	0	0	0	0	1
Receive ASK 4.8kbps w/ Start Vector and Clock Recovery	0	1	0	1*	0	0	1	1
TX OOK	1	0	0	0	0	0	0	1
Sleep	0	0	1	0	0	0	0	0

1='Pull High' 0='Pull Low'

*After data is received, reset this pin to '0' then set back to '1' to re-enable Start Vector recognition.

DR8000 Bill of Material (4.8kbps)

Item	Reference	Description	Value	Qty
1	C2	Capacitor SMT 0603	27pF	1
2	C4	Capacitor SMT 0603	.01uF	1
3	C5	Capacitor SMT 0603	.022uF	1
4	C6	Capacitor SMT 0603	100pF	1
5	C7	Capacitor SMT 0603	0.1uF	1
6	C8	Capacitor SMT 0603	0.1uF	1
7	C9	Capacitor SMT 0603	0.1uF	1
8	C3	Capacitor Tantalum EIA-B	4.7uF	1
9	L1	Fair-rite Bead 0603	2506033017YO	1
10	L2	Inductor Chip 0603	15nH	1
11	L3	Inductor Chip 0603	100nH	1
12	R1	Resistor Chip 0603	20K	1
13	R3	Resistor Chip 0603	100K	1
14	R4	Resistor Chip 0603	330K	1
15	R5	Resistor Chip 0603	6.2K	1
16	R6	Resistor Chip 0603	1.0K	1
17	R8	Resistor Chip 0603	1.0K	1
18	R7	Resistor Chip 0603	10K	1
19	U2	C8051F330 SILICON LABS Microcontroller		1
20	U1	IC, TR8000		1



Note: Specifications subject to change without notice.