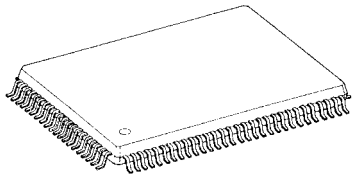
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TMP04CH01FXXX (JTMP04CH01XXXS)

CMOS 4 bit LL Microcontroller

(LL: Low power consumption & Low voltage operation)



QFP100-P-1420-0.65A

Weight: 1.65 g (typ.)

The TMP04CH00FXXX is a high-performance microcontroller designed to be in a variety of low-voltage products.

It is a 4 bit CMOS LL microcontroller with integrated a 4 bit high-performance CPU, memory (static work RAM and program ROM). LCD display LL controller driver, and a multi-function timer into a single chip.

The basic features are as follows.

Features

- Number of instructions: 56
- Minimum instruction execution time: 61 μs (at 32.768 kHz)
  1 μs (2 MHz/3.0 V)
- Oscillating circuit : low speed-crystal oscillator (32.768 kHz)/internal CR (33 kHz at 1.5 V)
  high speed-crystal oscillator (2 MHz at 3.0 V)/external CR (200 kHz at 1.5 V)
- Built-in ROM size : 16 K words (1 word = 16 bits)
- Built-in RAM size :
  Work RAM : 512 × 4 bits
- Input pins : 4 pins (with interrupts)
- I/O pins : 12 pins (with 4 interrupts and mask option)
- Output pins : 1 pin (Buzzer)
- Interruption : 2 external system (input pins, general purpose I/O pin)
  2 internal system (timer/counter, timings)
- Timer : 8 bits × 2 ch or 16 bits × 1 ch (software-selectable)
- LCD display driver controller: 52 seg × 16 com
- Built-in LCD driver power circuit
- Watchdog timer : Timer/Counter can be used as Watch Dog Timer
- Power supply voltage : 1.5/3.0 V (typ.) Mask option

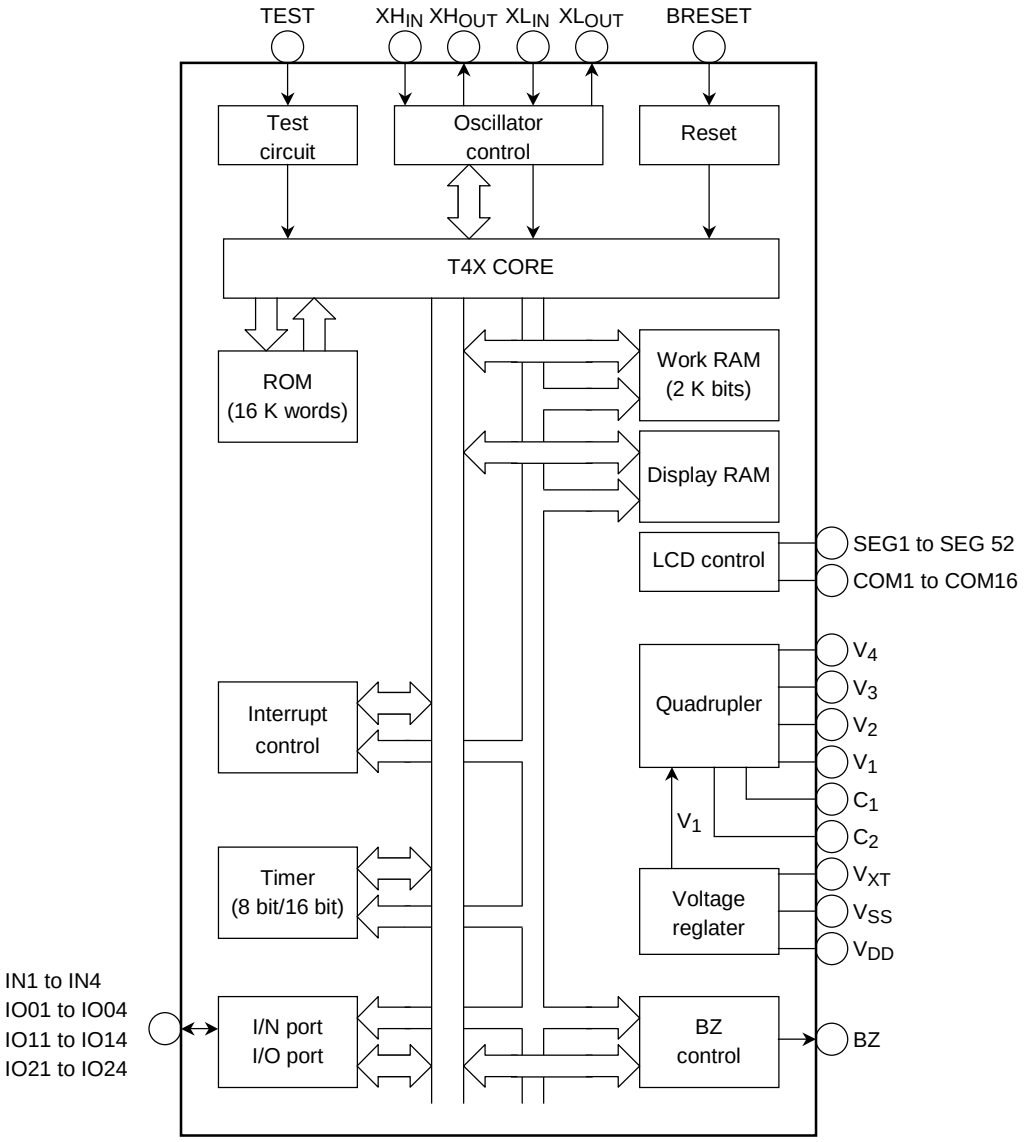
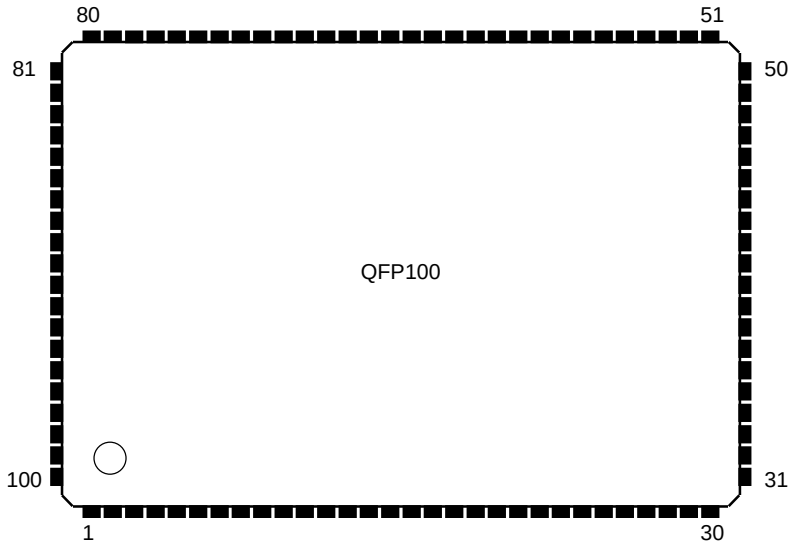


Figure 1 Block diagram

Pin Configuration

1. Pin Assignment



Pin No.	Pin Name
1	V_1
2	C_1
3	C_2
4	V_{SS}
5	V_{XT}
6	BRESET
7	XL_{IN}
8	XL_{OUT}
9	V_{DD}
10	XH_{IN}
11	XH_{OUT}
12	TEST
13	BZ
14	IN1
15	IN2
16	IN3
17	IN4
18	IO01
19	IO02
20	IO03
21	IO04
22	IO11
23	IO12
24	IO13
25	IO14

Pin No.	Pin Name
26	IO21
27	IO22
28	IO23
29	IO24
30	S_1
31	S_2
32	S_3
33	S_4
34	S_5
35	S_6
36	S_7
37	S_8
38	S_9
39	S_{10}
40	S_{11}
41	S_{12}
42	S_{13}
43	S_{14}
44	S_{15}
45	S_{16}
46	S_{17}
47	S_{18}
48	S_{19}
49	S_{20}
50	S_{21}

Pin No.	Pin Name
51	S_{22}
52	S_{23}
53	S_{24}
54	S_{25}
55	S_{26}
56	S_{27}
57	S_{28}
58	S_{29}
59	S_{30}
60	S_{31}
61	S_{32}
62	S_{33}
63	S_{34}
64	S_{35}
65	S_{36}
66	S_{37}
67	S_{38}
68	S_{39}
69	S_{40}
70	S_{41}
71	S_{42}
72	S_{43}
73	S_{44}
74	S_{45}
75	S_{46}

Pin No.	Pin Name
76	S_{47}
77	S_{48}
78	S_{49}
79	S_{50}
80	S_{51}
81	S_{52}
82	COM16
83	COM15
84	COM14
85	COM13
86	COM12
87	COM11
88	COM10
89	COM9
90	COM8
91	COM7
92	COM6
93	COM5
94	COM4
95	COM3
96	COM2
97	COM1
98	V_4
99	V_3
100	V_2

2. Pin Description

Pin Name	Function
V_{DD}	Power supply (+)
V_{SS}	Power supply (−)
V_{XT}	Voltage regulator1 output (output for only the mask option 3.0 V type)
V_1	Voltage regulator2 output
V_2 to V_4	Boosted voltage output
C_1, C_2	Capacitor pin for LCD booster
XH_{IN}, XH_{OUT}	Crystal/resister connection pin for high-speed oscillator
XL_{IN}, XL_{OUT}	Crystal connection pin for low-speed oscillator
IN1 to IN4	Input port (with interruption)
IO01 to IO04	I/O port (with interruption)
IO11 to IO14	I/O port
IO21 to IO24	I/O port
SEG1 to SEG52	LCD segment output
COM1 to COM16	LCD common output
BZ	Buzzer output
BRESET	Reset input (low active)
TEST	Test input

Memory Map

1. Program ROM

Program ROM consists of 16 bits 1 word. Op-code and operand are executed in one word units. Program ROM consists of 4 K words per page. The internal program ROM area is 4 pages (16 K words).
This program ROM area can be used for constant data ROM. In this case, it can be used in byte units (1 byte = 8 bits).

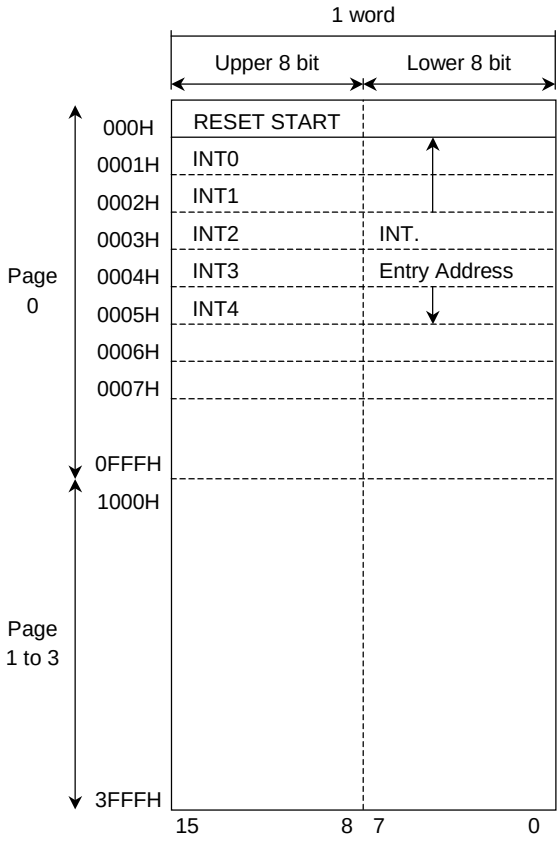


Figure 2 Program memory map

Note: Use the CALL instruction to write the interrupt entry address. Write NOP for unused interrupts.

```
Example:    CALL A    ; INT0
            NOP       ; INT1
            CALL B    ; INT2
            NOP       ; INT3
            NOP       ; INT4
            NOP       ; INT5
            NOP       ; INT6
```

2. Work RAM

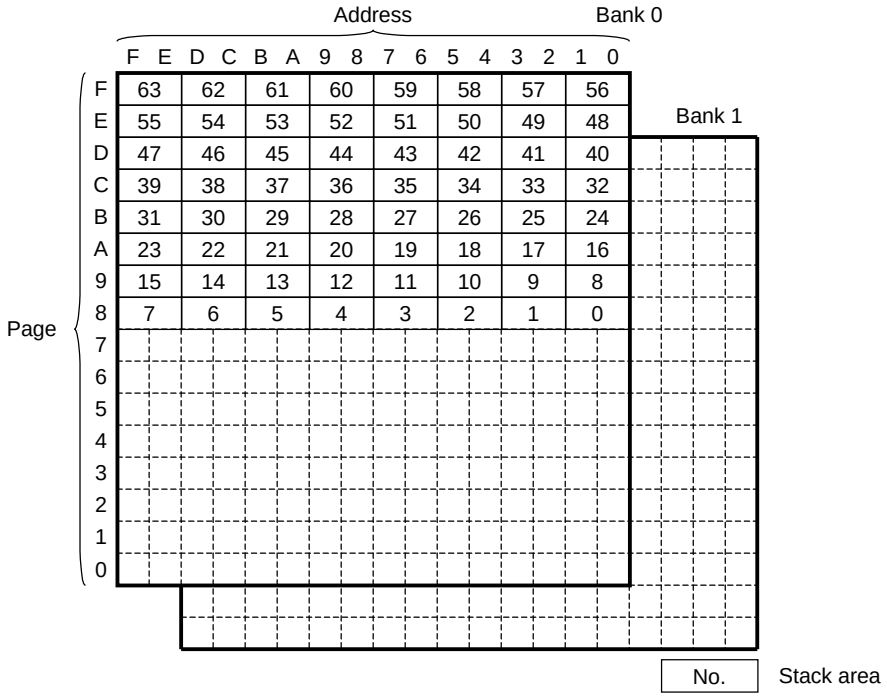
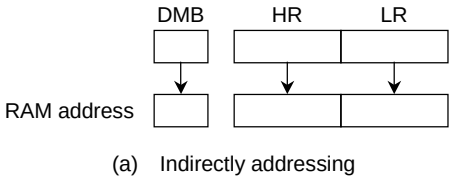


Figure 3 Work RAM

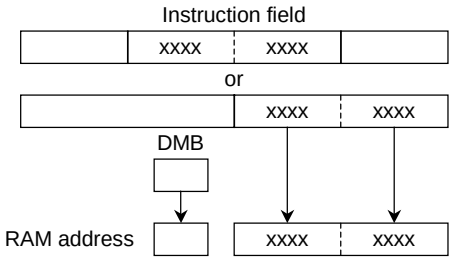
Work RAM consists of 512 × 4 bits.
R/W is performed at the address specified by bellows.

(1) Indirectly addressing mode (Figure 4 (a))
DMB in F-reg, H, L-reg specify the Work RAM address. (DMB: bank, H-reg : page, L-reg: address)
LD A, M: A ← RAM (HL)



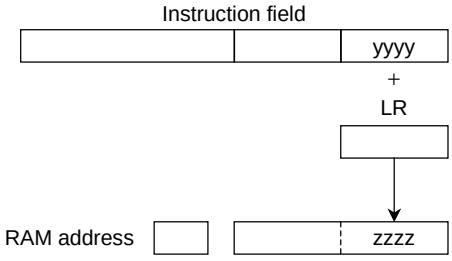
(a) Indirectly addressing

(2) Directly addressing mode (Figure 4 (b))
Immediate data (8 bits) in instruction specify the Work RAM page and address.
Bank is specified by DMB in F-reg.
LDI 2CH, 0AH: RAM (2CH) ← AH



(b) Directly addressing

(3) Index addressing mode (Figure 4 (c))
Address (L-reg) is specified by the immediate data (4 bits) in instruction, and the other immediate data specify page.
LDRI 4H, 3H: RAM (HL + 4H) ← RAM (3H, L)
L ← L + 1, A ← A − 1



(c) Index addressing

Figure 4 Addressing mode

BANK0, PAGE8 to F area can be used as Stack area.
When using the “CALL/CALLS” instruction or start the interruption routine, the data of program counter and Program memory bank are stored in Stack area.
Then, using “RET” instruction, program return according to those data.
And, using “PUSH” instruction, 8 bits data in a pair register can be stored in Stack area.
Then, using “POP” instruction, those data are returned to the register.
Maximum Stack area is 64 (0 to 63), and each Stack area consist of 8 bits.

3. Data RAM

TMP04CH01FXXX has Display RAM, and addressing and data read/write is decided by Register file, as follows. When the data is read from/written into Display RAM. DRCE (PC6-bit2) is needed to be 1.

	MSB 3	2	1	0 LSB
PC6	—	DRCE	DON	CE1

Addressing is decided by DRR1 to DRR4 (PD4) and DRC1 to DRC3 (PD5) (LSB is DRR1, and MSB is DRC3)

	MSB 3	2	1	0 LSB
PD5	—	DRC3	DRC2	DRC1
PD4	DRR4	DRR3	DRR2	DRR1

Data is read/written by 8 bits which is set in DRD1 to DRD8 (PD6, PD7).
To read from/written into DISPLAY, only 8 bits transference instruction can be used.

	MSB 3	2	1	0 LSB
PD7	DRD8	DRD7	DRD6	DRD5
PD6	DRD4	DRD3	DRD2	DRD1

CAUTION:

1. When “HALT” instruction is executed for the next instruction of the transference the data to Display RAM, the data of Display RAM is broken.
2. When “HALT” instruction is executed during DRCE is 1, the data of Display RAM is broken. Therefore, be sure to set DRCE to 0 before executing the HALT instruction.
   DRD1 to 8 (PD6, PD7) are valid for only 8-bit transfer instructions.

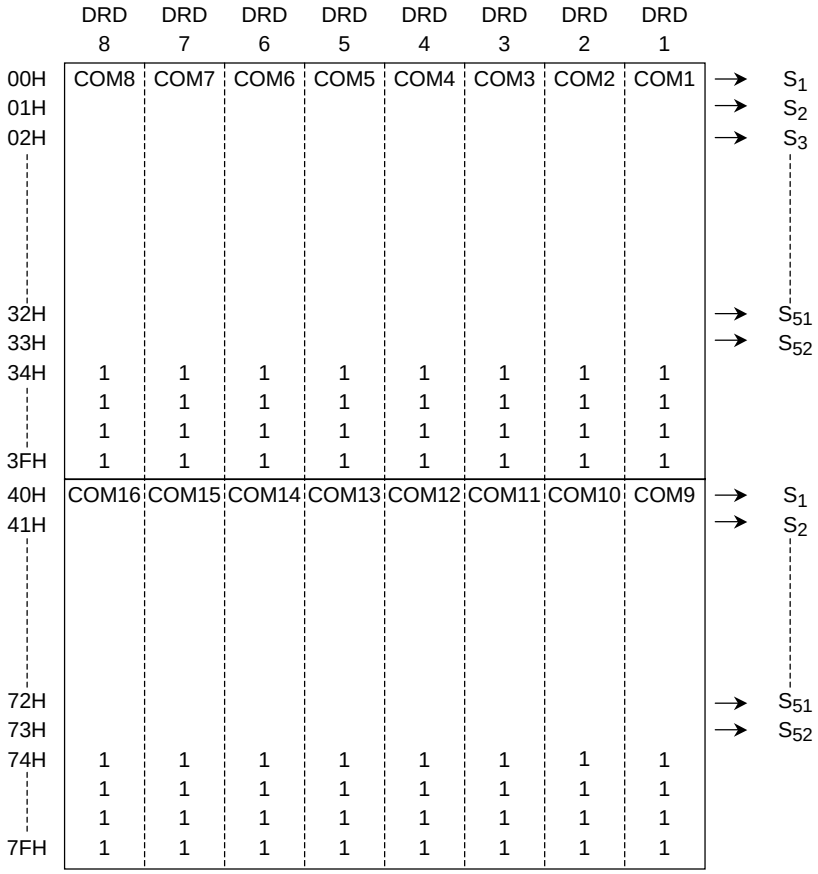


Figure 5 Display RAM

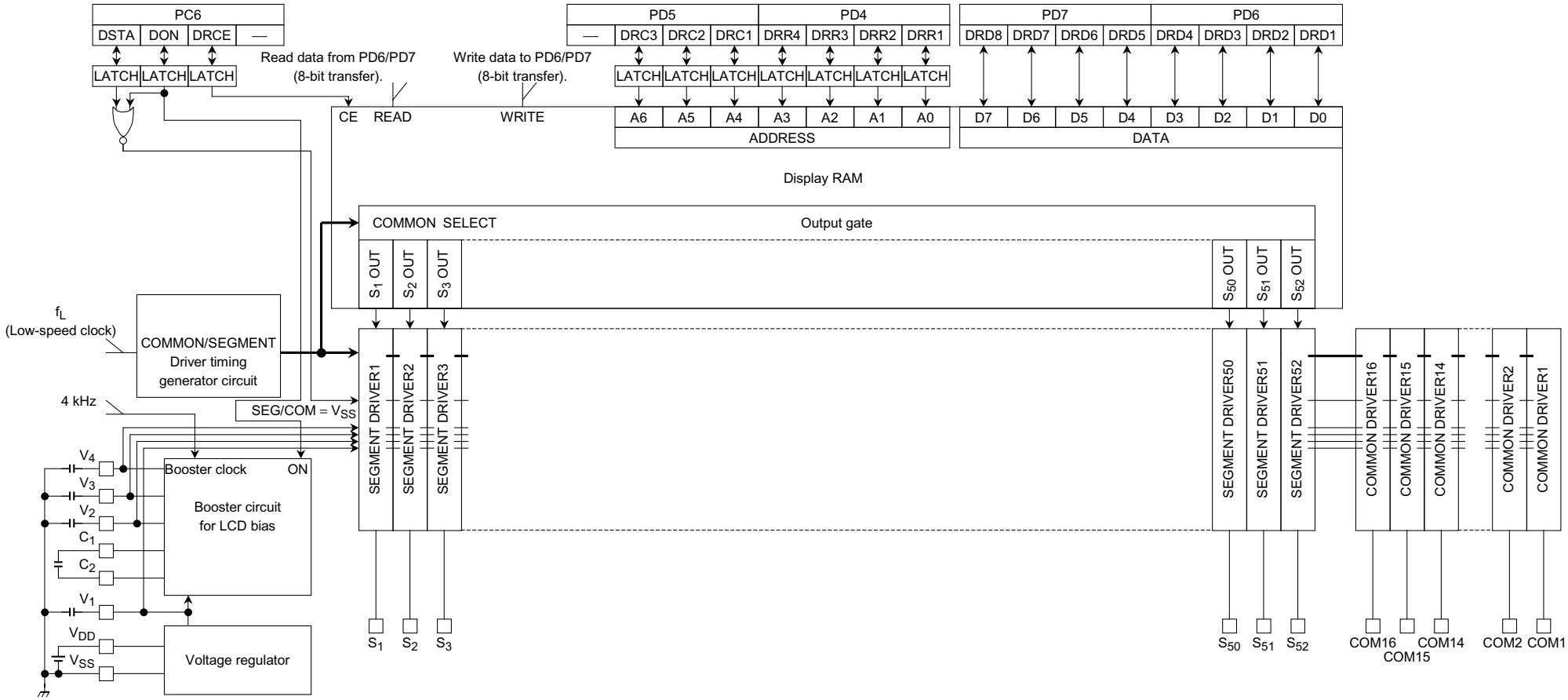


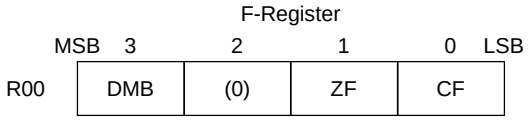
Figure 6 LCD driver

Register File

Register files consist of (1) general-purpose registers, (2) system registers, and (3) peripheral I/O registers. Figure 6 shows the overall configuration of register files.

1. General Register

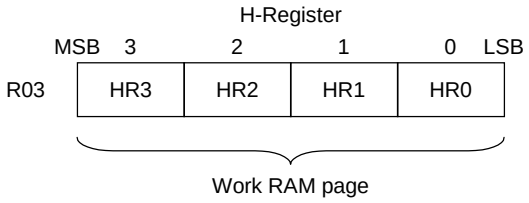
1. Flag Register: F-Register (PAGE/AD = 0/0)

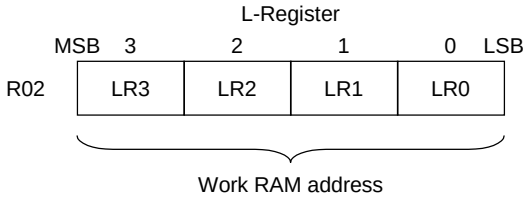


CF : Carry Flag
ZF : Zero Flag
(0) : Not use
DMB : Work RAM Bank

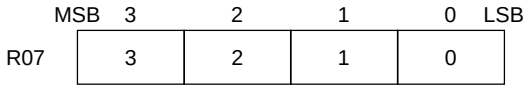
2. Accumulater Register: A-Register (PAGE/AD = 0/1)
   Accumulator for arithmetic operations.
   When consecutive instructions are executed, used as a counter register.

3. H.L Register (PAGE/AD = 0/3 to 2)
   H.L Register are used for Work RAM address setting with DMB.





4. Bank Register (PAGE/AD = 0/7): B-Register
   B-Register is used for ROM page.



0000 = Page 0
0001 = Page 1
0010 = Page 2
0011 = Page 3

5. E-Register, D-Register, P-Register (B-Register) (PAGE/AD = 0/4, 0/5, 0/6, 0/7)
   General purpose register.
   When using ROM as Data Table Function, B, P, D, E-Register are used for ROM address setting. (Data table function: user can use ROM area for store the constant, and can access those constant by LDBL and LDBH instruction.)

2. System Registers

1. Stack pointer (PAGE/AD = 1/0, 1/1)

The stack pointer shows the location (63 to 0) in the stack area in work RAM.

	MSB 3	2	1	0
R10	SP4	SP2	SP1	—

	MSB 3	2	1	0
R11	—	SP32	SP16	SP8

2. Interrupt Enable/Disable Registers (PAGE/AD = 1/2, 1/3)

Enable/disable interrupts. There are five interrupt vectors (INT0 to INT4). Writing data in the bit corresponding to an interrupt enables/disables the interrupt. The details are described in the section on peripheral circuits.

	MSB 3	2	1	0
R12	INT2	INT1	INT0	(0)

	MSB 3	2	1	0
R13	—	—	INT4	INT3

3. Input/Output Registers (PAGE/AD = 1/4, 1/5)

Used for the input/output pins (IO11 to IO14, IO21 to IO24). Using the bit that corresponds to a pin, output data can be set or input data can be read. The details are described in the section on peripheral circuits.

	MSB 3	2	1	0
R14	IO14	IO13	IO12	IO11

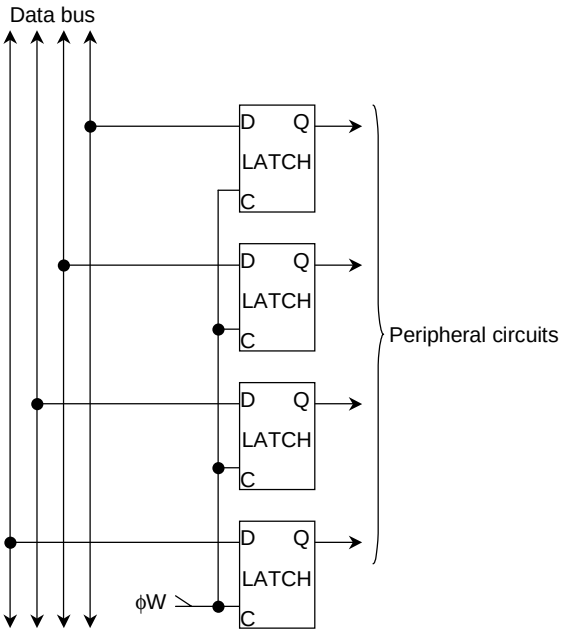
	MSB 3	2	1	0
R15	IO24	IO23	IO22	IO21

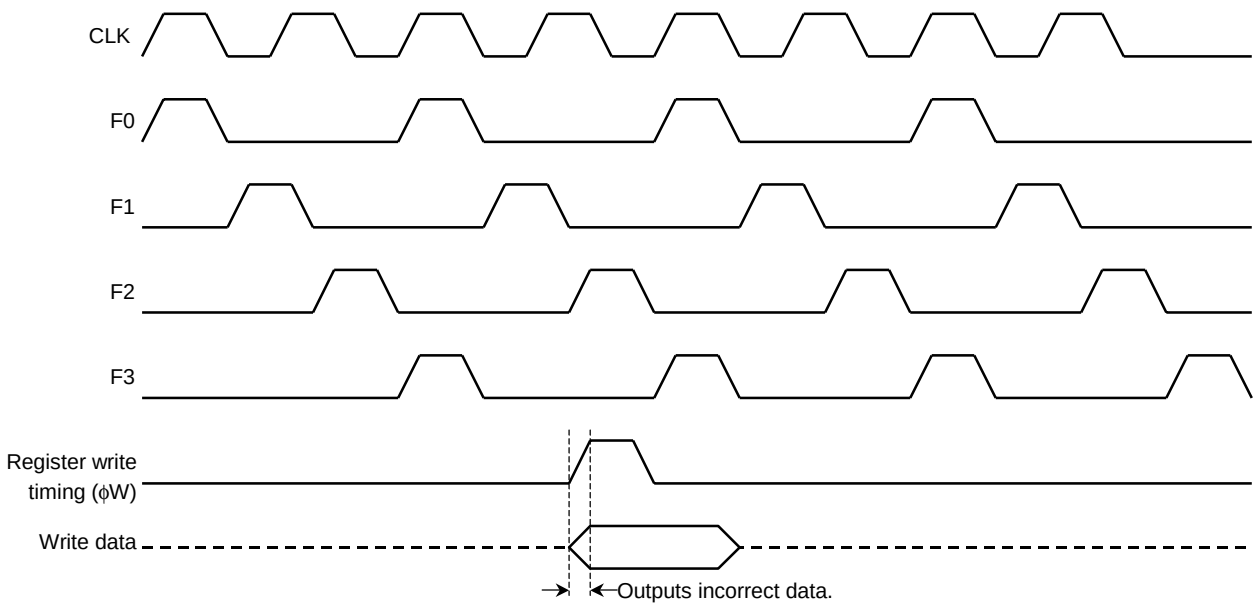
3. Peripheral I/O Registers

Registers used to control peripheral circuits specific to the product are allocated to pages 2 to 7. The details are described in the section on peripheral circuits.

Note: A precaution relating to Writes to System Registers/Peripheral I/O Registers.

Writing to System Register and I/O Registers is performed in synchronization with ϕW. Because rising edges of ϕW coincides with the timing at which Write data is output on the data bus, it is possible that incorrect data is output to the peripheral circuits for a very short period of time. Please take this into account when programming.





Page (RFB)	Address	0		1		2		3		4		5		6		7	
	8 bit Address	0				2				4				6			
		LOWER4BIT		UPPER4BIT		L4BIT		H4BIT		L4BIT		H4BIT		L4BIT		H4BIT	
	R/W	Read	Write	Read	Write	Read	Write	Read	Write	Read	Write	Read	Write	Read	Write	Read	Write
0	MSB BIT 3	F REGISTER		A REGISTER		L REGISTER		H REGISTER		E REGISTER		D REGISTER		P REGISTER		B REGISTER	
	BIT 2																
	BIT 1																
	LSB BIT 0																
1 (P1x)	MSB BIT 3	STACK POINTER (SP)		0		INT2				IOD14	IOO14	IOD24	IOO24				
	BIT 2					INT1				IOD13	IOO13	IOD23	IOO23				
	BIT 1					INT0		INT4		IOD12	IOO12	IOD22	IOO22				
	LSB BIT 0	0				0		INT3		IOD11	IOO11	IOD21	IOO21				
2 (PAx)	MSB BIT 3	IND4		IOD04	IOO04												RST4
	BIT 2	IND3		IOD03	IOO03									LOWCP			RST3
	BIT 1	IND2		IOD02	IOO02									CPMODE2			RST2
	LSB BIT 0	IND1		IOD01	IOO01									CPMODE1			RST1
3 (PBx)	MSB BIT 3																
	BIT 2																
	BIT 1																
	LSB BIT 0																
4 (PCx)	MSB BIT 3			IIN4		IIE4											
	BIT 2	ESELT		IIN3		IIE3									DRCE		
	BIT 1	ESELIO		IIN2		IIE2									DON	P2	
	LSB BIT 0	ESELI		IIN1		IIE1		IOIE0							DSTA	P1	
5 (PDx)	MSB BIT 3	TI4		1/2			TIR4	TIE4		DRR4				DRD4		DRD8	
	BIT 2	TI3		4/8			TIR3	TIE3		DRR3		DRC3		DRD3		DRD7	
	BIT 1	TI2		16/32			TIR2	TIE2		DRR2		DRC2		DRD2		DRD6	
	LSB BIT 0	TI1		128/256			TIR1	TIE1		DRR1		DRC1		DRD1		DRD5	
6 (PEx)	MSB BIT 3	TCR14	SET14	TCR18	SET18			TC1EN								2/4 K	
	BIT 2	TCR13	SET13	TCR17	SET17	CKS13			TC1R							BZ3	
	BIT 1	TCR12	SET12	TCR16	SET16	CKS12		CMPEN1		TCI1E						BZ2	
	LSB BIT 0	TCR11	SET11	TCR15	SET15	CKS11		WDT1			TCI1R					BZ1	
7 (PFx)	MSB BIT 3	TCR24	SET24	TCR28	SET28	TCPS		TC2EN									
	BIT 2	TCR23	SET23	TCR27	SET27	CKS23			TC2R								
	BIT 1	TCR22	SET22	TCR26	SET26	CKS22		CMPEN2		TCI2E							
	LSB BIT 0	TCR21	SET21	TCR25	SET25	CKS21					TCI2R						

Figure 7 Register file

Note: Blank columns are indeterminate.

Peripheral Circuit

Each peripheral circuits can be accessed (Read/Write/Circuit setting) by Register files.

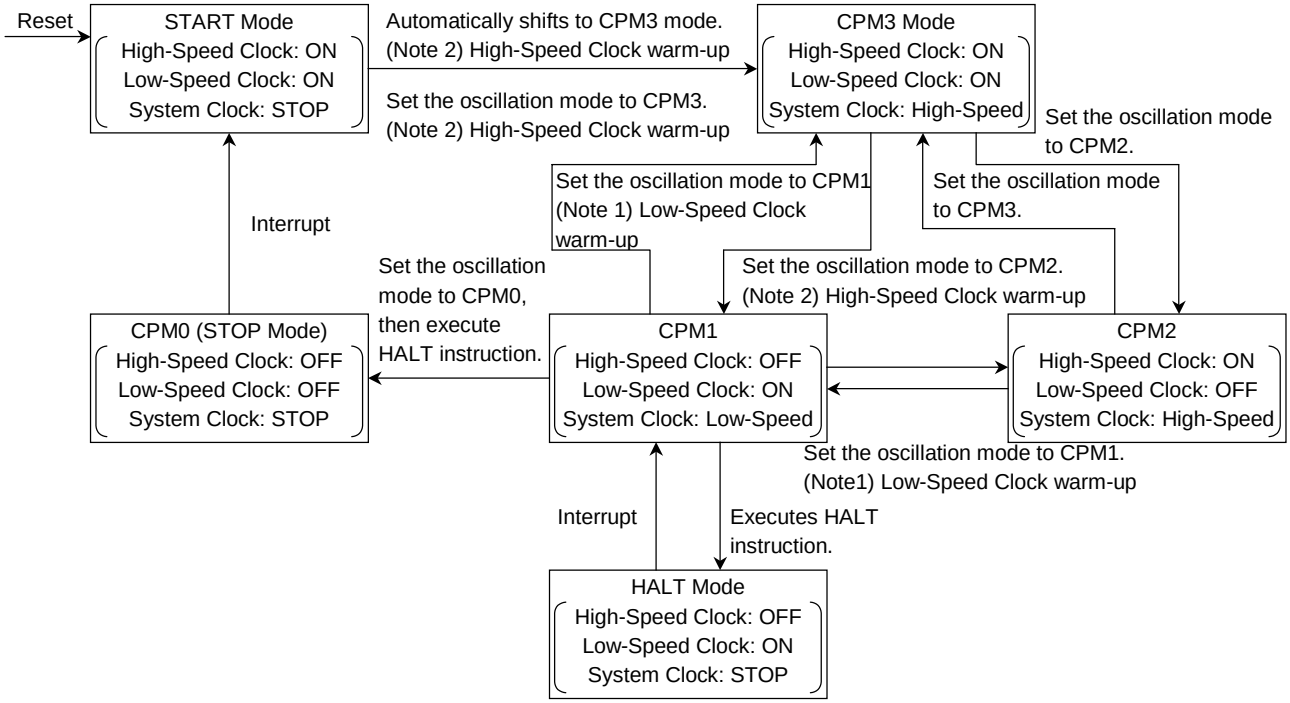
1. Oscillator Block

	MSB 3	2	1	0 LSB
PA6	—	LOWCP	CPMODE2	CPMODE1

The CPU clock is generated by the asynchronous oscillator switching circuit which has low-speed and high-speed clock oscillator circuit.
This block also provides the clock for the timer circuit, LCD driver, Quadrupler.
Oscillation mode is controlled by Register files “CPMODE1” and “CPMODE2” (PAGE/AD = 2/6), as follows.

CPMODE 1	CPMODE 2	Low-speed OSC	High-speed OSC	System CP	Mode Name
0	0	OFF	OFF	OFF	(CPM0)
1	0	ON	OFF	Low-speed	(CPM1)
0	1	OFF	ON	High-speed	(CPM2)
1	1	ON	ON	High-speed	(CPM3)

CPMODE 1, 2 are initially 1 (CPM3).
“LOWCP” is the display clock control bit. When “LOWCP” is set to 1, Low-speed OSC clock is supplied to LCD circuit. “LOWCP” is initially “0”. Even if LOWCP is set to 1, clock cannot be occupied to display circuit during Low-speed OSC stopped, and display cannot be shown.
Low-speed OSC circuit can select X’tal or internal CR oscillation by Mask option.
High-speed OSC circuit can select X’tal or external CR oscillation by Mask option.
Setting a register to CPM1 and executing a HALT instruction sets the mode to Halt (system CP off, high-speed oscillator off, low-speed oscillator on). Setting a register to CPM0 and executing a HALT instruction sets the mode to Stop (system CP off, high-speed oscillator and low-speed oscillators off). Even if, mode is changed to MODE 0 from MODE 1/2/3, there are no changing until use “HALT” instruction.
The High/Low-speed OSC circuit has WARM UP function.
The warm-up function disables the crystal oscillator as the system clock from when the crystal oscillator starts oscillation to when the frequency stabilizes. The warm-up circuit in the high-speed crystal oscillator circuit consists of a 15-stage binary counter. The warm-up time is 16,384 pulses of the high-speed clock.
The warm-up circuit in the low-speed crystal oscillator circuit consists of a 9-stage binary counter.
The warm-up time is 256 pulses of the high-speed clock.
The low-speed oscillation does not have enough warm-up time, therefore, when the oscillation is started, software need to make warming up time enoughly.
Set the warm-up time by software to approx. 500 ms as standard.
When the System CP is changed between Low and High (CPM1→CPM2/3 or CPM2→CPM1), changing System CP waits to finish the warming up time.
Also that until the system CP is changed, instructions are executed with the previous system CP.
If the CR oscillator is selected as the high- or low-speed oscillator circuit, the warm-up function is disabled.



Note 1: Low-Speed Clock warm-up

If X'tal oscillation circuit is selected for low-speed oscillation, it takes some time before low-speed oscillation is used for system clock.

Note 2: High-Speed Clock warm-up

If X'tal oscillation circuit is selected for high-speed oscillation, it takes some time before high-speed oscillation is used for system clock.

Figure 8 Mode transition

TMP04CH01FXXX has 21 bits Divider.

The divider circuit of bits 1 to 6 generates a clock from 1 MHz to 32 kHz by dividing the high-speed clock (2 MHz). The divider circuit of bits 7 to 21 generates a clock from 16 kHz to 1 Hz by dividing the 32 kHz clock. When the low-speed oscillator circuit is on (CPM1/CPM3), a low-speed clock (32 MHz) is supplied to the divider circuit of bits 7 to 21. When the low-speed oscillator circuit is off (CPM2), output from bit 6 is supplied.

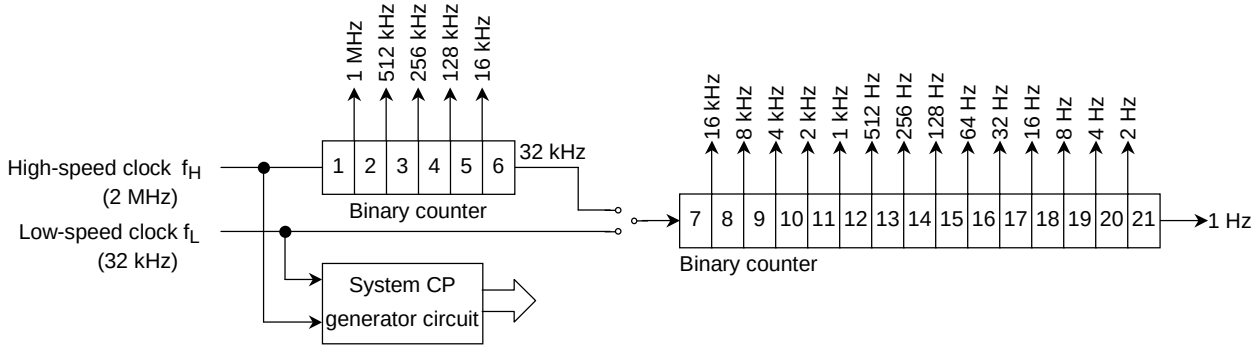


Figure 9 Divider circuit

The reset for this Divider circuit is done by Register file RST1 to RST4 (PA7W).

	MSB 3	2	1	0 LSB
PA7W	RST4	RST3	RST2	RST1

RST1: Binary counter 1 to 6 (2 M to 32 kHz) reset
RST2: Binary counter 7 to 12 (16 k to 512 Hz) reset
RST3: Binary counter 13 to 17 (256Hz to 16 Hz) reset
RST4: Binary counter 18 to 21 (8Hz to 1 Hz) reset
(when using 2 MHz, 32 kHz crystal)

CAUTION:

1. Do not set System CP to low speed when the Low-speed OSC is not in operation or before stable.
2. Do not set System CP to high speed when the High-speed OSC is not in operation or before stable.
3. And, when Low-speed OSC is on, low-speed frequency is supplied from 7th bit Divider circuit (when use 2 MHz crystal for High-speed OSC and 32 kHz crystal for Low-speed OSC and the mode is CPM3, 1 MHz to 32 kHz are made by 2 MHz crystal, 16 kHz to 1 Hz are made by 32 kHz crystal. And when the mode is CPM2, all frequency are made by 2 MHz crystal. Therefore if the mode change between CPM1 and CPM2 or CPM2 and CPM3, the frequency which is supplied by Binary counter 7 to 21 shift the timing).
4. When operated with a 1.5 V power supply, the oscillation frequency on the high-speed side is 200 kHz (max), so that the output of binary counter 6 is 3.125 kHz (max).
Consequently, if the mode is changed from CPM1 or CPM3 to CPM2 or from CPM2 to CPM1 or CPM3, the generated timing changes greatly.
5. When the crystal oscillator circuit is used for low-speed oscillation, a long time is required from oscillation stop to oscillation start. The LCD circuit operates using a low-speed clock. LCD cannot be performed until oscillation starts. After power on, operate the low-speed oscillator circuit at all times and do not change to STOP mode.

Example 1

START mode (After warming up, program start at address 0000.)
↓
CPM3 (High/Low speed ON, SYSCP = High, LOWCP OFF)
↓ LD 26O, 7H
CPM3 (High/Low speed ON, SYSCP = High, LOWCP ON)
↓ LD 26O, 4H
CPM0 (High/Low speed ON, SYSCP = High, LOWCP ON)
(There are no change after shift to CPM0)
↓ HALT
STOP mode (High/Low-speed OSC, STOP, SYSCP OFF, LOWCP OFF)

When an interruption occurs, the mode is changed to START mode and program start at the address which is decided by each interruption (refer to Figure 2).

Example 2

START mode (After warming up, program start at address 0000.)
↓
CPM3 (High/Low speed ON, SYSCP = High, LOWCP OFF)
↓ LD 26O, 5H
CPM1 (Low speed ON, SYSCP = low, LOWCP ON)
↓ HALT
HALT mode (High speed OSC OFF, Low-speed OSC ON, SYSCP OFF, LOWCP ON)

When an interruption occurs, the mode is changed to slow mode (CPM1) and program start at the address which is decided by each interruption.

Example 3

START mode (After warming up, program start at address 0000.)

↓

CPM3 (High/Low speed ON, SYSCP = High, LOWCP OFF)

↓ LD 26O, 7H

CPM3 (High/Low speed ON, SYSCP = High, LOWCP ON)

↓ LD 26O, 4H

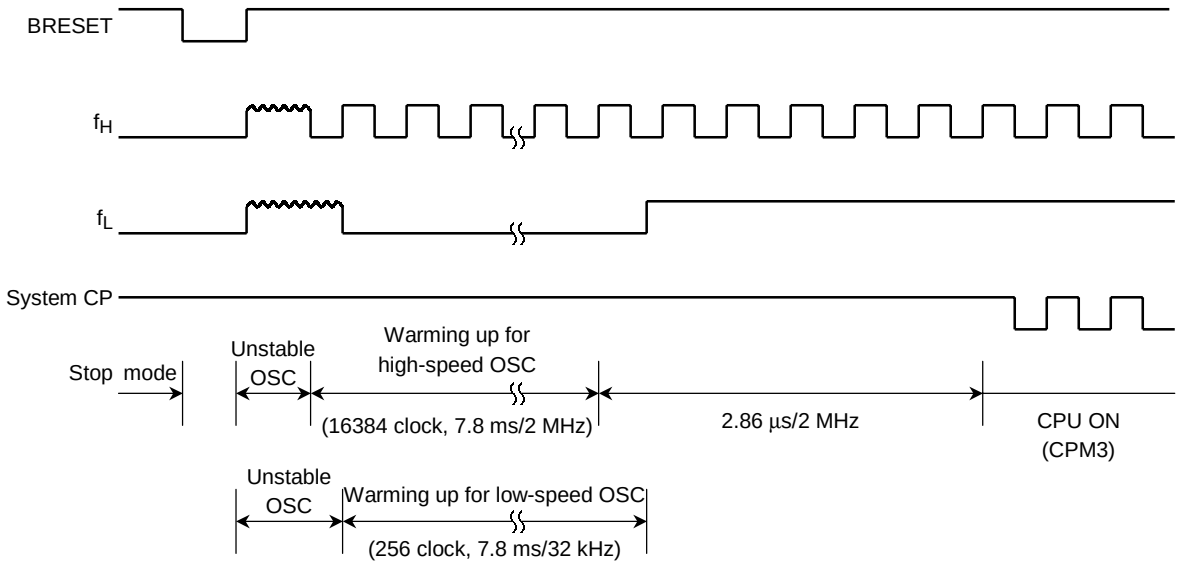
CPM0 (High/Low speed ON, SYSCP = High, LOWCP ON)

(There are no change after shift to CPM0.)

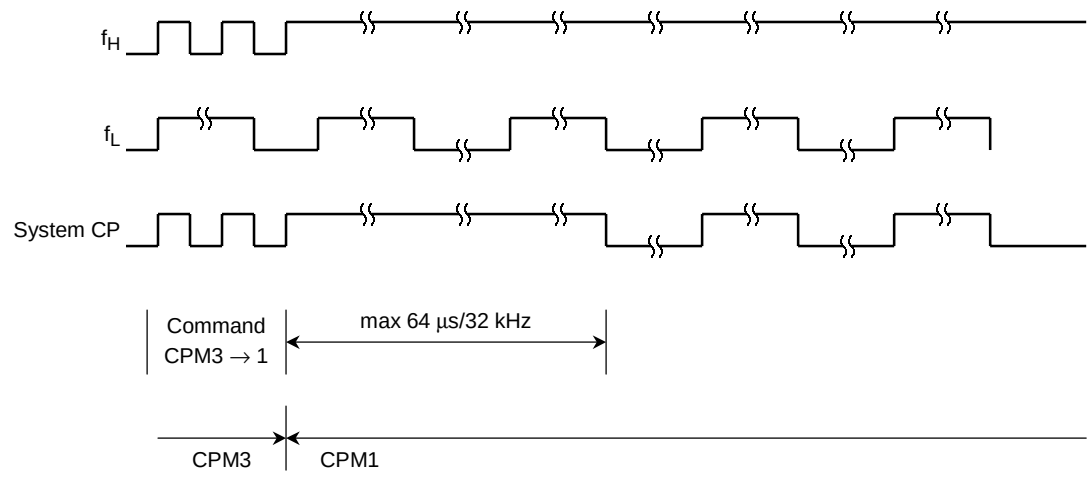
↓ LD 26O, 7H

CPM3 (High/Low speed ON, SYSCP = High, LOWCP ON)

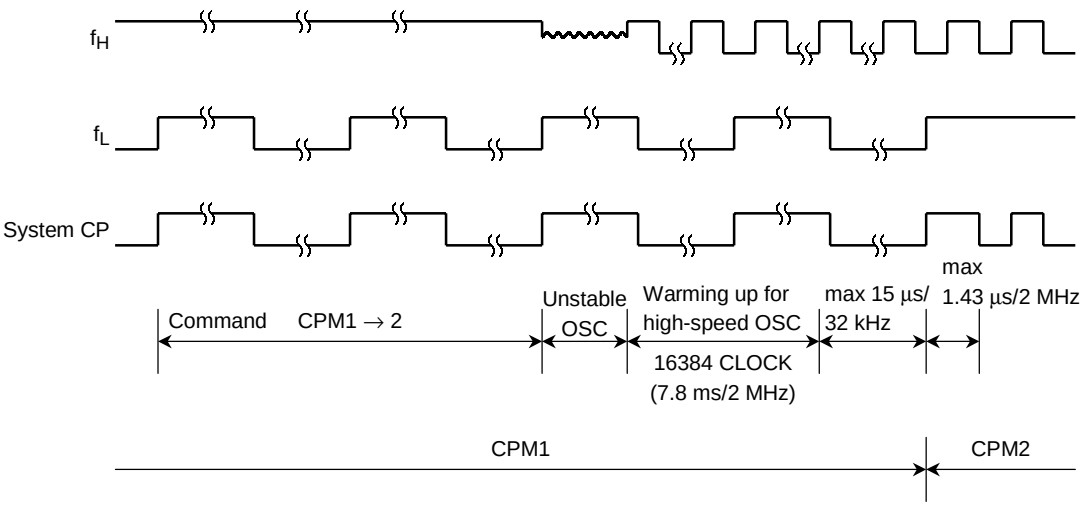
Example 4 (After reset)



Example 5 (CPM3 → 1)



Example 6 (CPM1 → 2)



Note: No warm-up is provided for high-speed and low-speed RC oscillations by mask options.

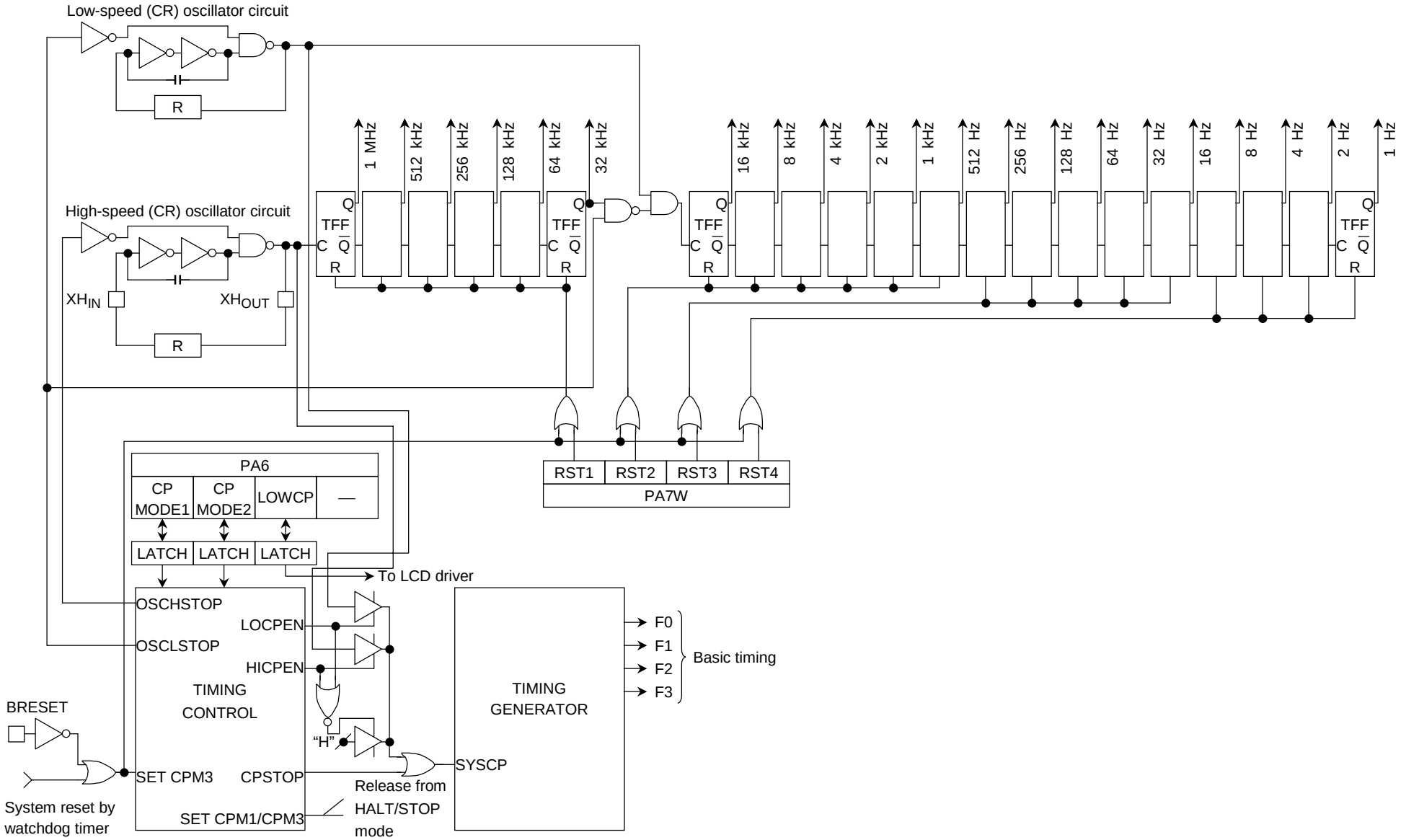


Figure 10 Oscillator circuit/Divider circuit

2. Interruption Block

Interruption is supplied by IN1to IN4, IO01 to IO04, Timer/Counter, Timing.

(Interruption priority)

Interruption priority can be selected by Register file P1 and P2.
Interrupt priority is valid only when multiple interrupts occur simultaneously.
P1 and P2 are initially 0.

	MSB 3	2	1	0 LSB
PC7	—	—	P2	P1

P1	P2	INT0	INT1	INT2	INT3	INT4
0	0	IIN	IOIN	TIN	TCIN1	TCIN2
1	0	IOIN	IIN	TIN	TCIN1	TCIN2
0	1	TIN	IIN	IOIN	TCIN1	TCIN2
1	1	TCIN1	IIN	IOIN	TIN	TCIN2

(Higher) ← → (Lower)
Priority

IIN: IN1 to IN4, IOIN: IO01 to IO04, TIN: TIMING, TCIN1/2: TIMER/COUNTER1/2

(Interruption enable/disable)

Each interruption (IIN, IOIN, TIN, TCIN1, TCIN2) is decided enable/disable as follows.

IIN : IIE1 to IIE4 (R42-BIT 0 to 3)
IOIN : IOIE0 (R43-BIT 0)
TIN : TIE1 to TIE4 (R53-BIT 0 to 3)
TCIN1 : TCI1E (R64-BIT 1)
TCIN2 : TCI2E (R74-BIT 1)

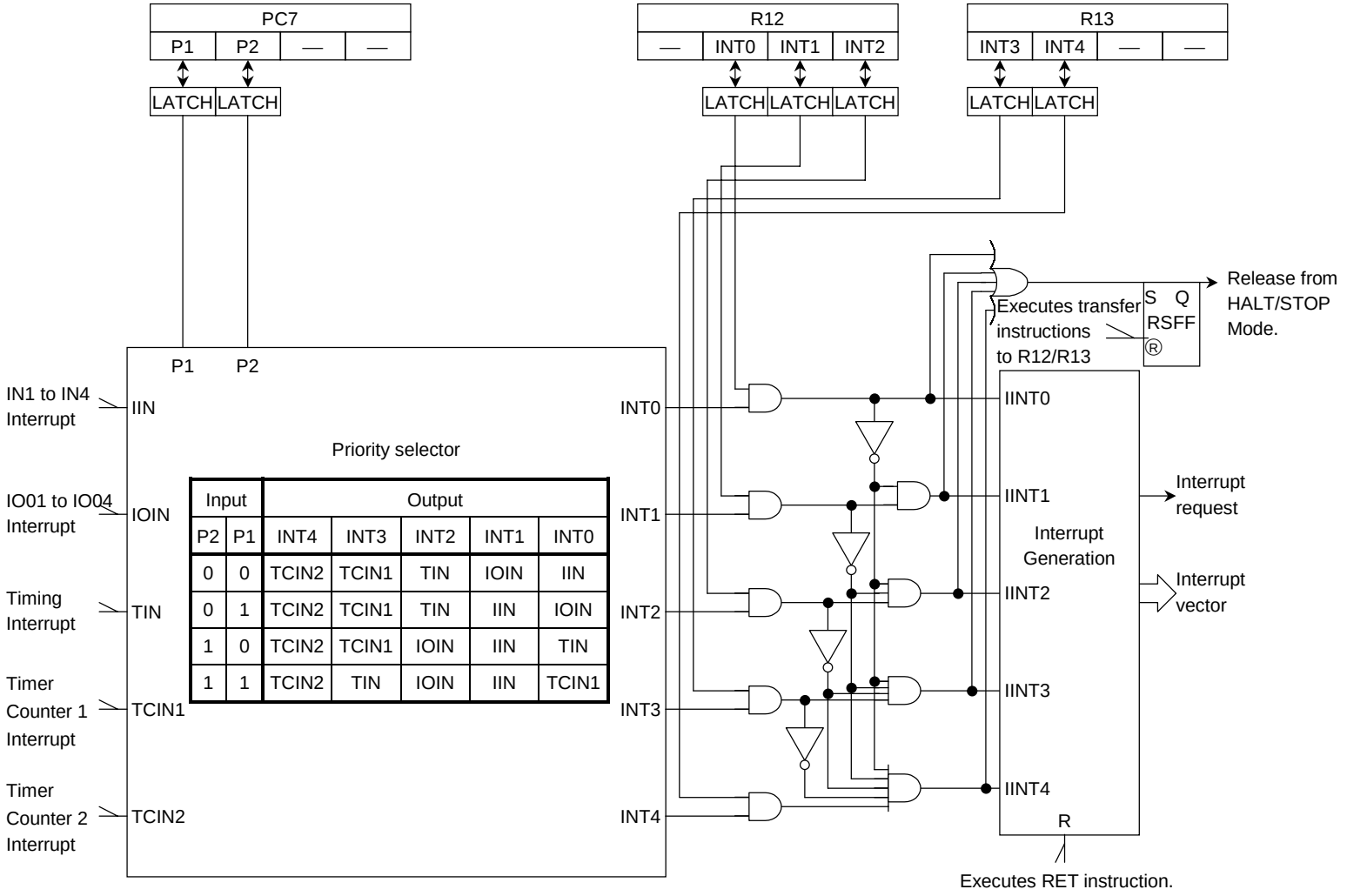
After deciding priority by P1, P2 each interruption is decided enable/disable by INT0 to INT4.
Disable the unnecessary interrupts in your application by initial settings of IIE1-4, IOIE, TIE1-4, and TCI1E/2E.
INT0 to INT4 are initially 0 (disable)

	MSB 3	2	1	0 LSB
R12	INT2	INT1	INT0	(0)
R13	—	—	INT4	INT3

INT0 to INT4 = 0 INT0 to INT4 disable
= 1 INT0 to INT4 enable

(Interrupt reset)

After an interrupt occurs, reset the interrupt following the procedures described below.
First, reset IN1 to IN4 interrupt/IO01 to IO04 Interrupt/Timing Interrupt/Timer Counter 1 Interrupt/Timer Counter 2 Interrupt.
Then reset the signal “Release from HALT/STOP Mode” by executing a transfer instruction to R12 or R13. (Re-enable interrupts by executing a transfer instruction to R12 or R13, as you need.)
How to deactivate respective interrupts will be explained in the sections which describe each of the interrupts.



Input		Output				
P2	P1	INT4	INT3	INT2	INT1	INT0
0	0	TCIN2	TCIN1	TIN	IOIN	IIN
0	1	TCIN2	TCIN1	TIN	IIN	IOIN
1	0	TCIN2	TCIN1	IOIN	IIN	TIN
1	1	TCIN2	TIN	IOIN	IIN	TCIN1

Figure 11 Interruption circuit block

2-1. Iuput/Inoutput Interruption

(Interruption enable/disable)

	MSB 3	2	1	0 LSB
PC2	IIE4	IIE3	IIE2	IIE1

IIE1 = 0 IN1 Interruption disable
1 IN1 Interruption enable
IIE2 = 0 IN2 Interruption disable
1 IN2 Interruption enable
IIE3 = 0 IN3 Interruption disable
1 IN3 Interruption enable
IIE4 = 0 IN4 Interruption disable
1 IN4 Interruption enable

IIE1 to IIE4 are initially 0 (IN1 to IN4 interruption disable).

	MSB 3	2	1	0 LSB
PC3	—	—	—	IOIE0

IOIE0 = 0 IO01 to IO04 Interruption disable
1 IO01 to IO04 Interruption enable

IOIE0 is initially 0 (disable).
Interruption enable/disable bit can use as interruption reset.
When the interruption occurs and after recognizing the interruption, it can be resetted INT latch by setting IIE1 to IIE4 or IOIE0.

(Interruption data read)
Interruption Data of IN1 to IN4 can be read by Register file IIN1 to IIN4.

	MSB 3	2	1	0 LSB
PC1R	IIN4	IIN3	IIN2	IIN1

Example

```
LD 42O, 0FH     (set enable to IN1 to IN4 interruption)
    ↓   IN1 interruption occurs.
        Program goes to the address which is decided by each interruption.
LD M, 41O       (read IN1 to IN4 interruption)
    ↓   Recognize which interruption is occurred.
        (recognize IN1 interruption is occurred.)
LD 42O, 0EH     (reset IN1 interruption)
    ↓
LD 12O, 0FH     (set enable to INT0 to INT2)
    ↓
LD 13O, 0FH     (set enable to INT3 to INT4)
    ↓
LD 42O, 0FH     (set enable to IN1 to IN4 interruption)
```

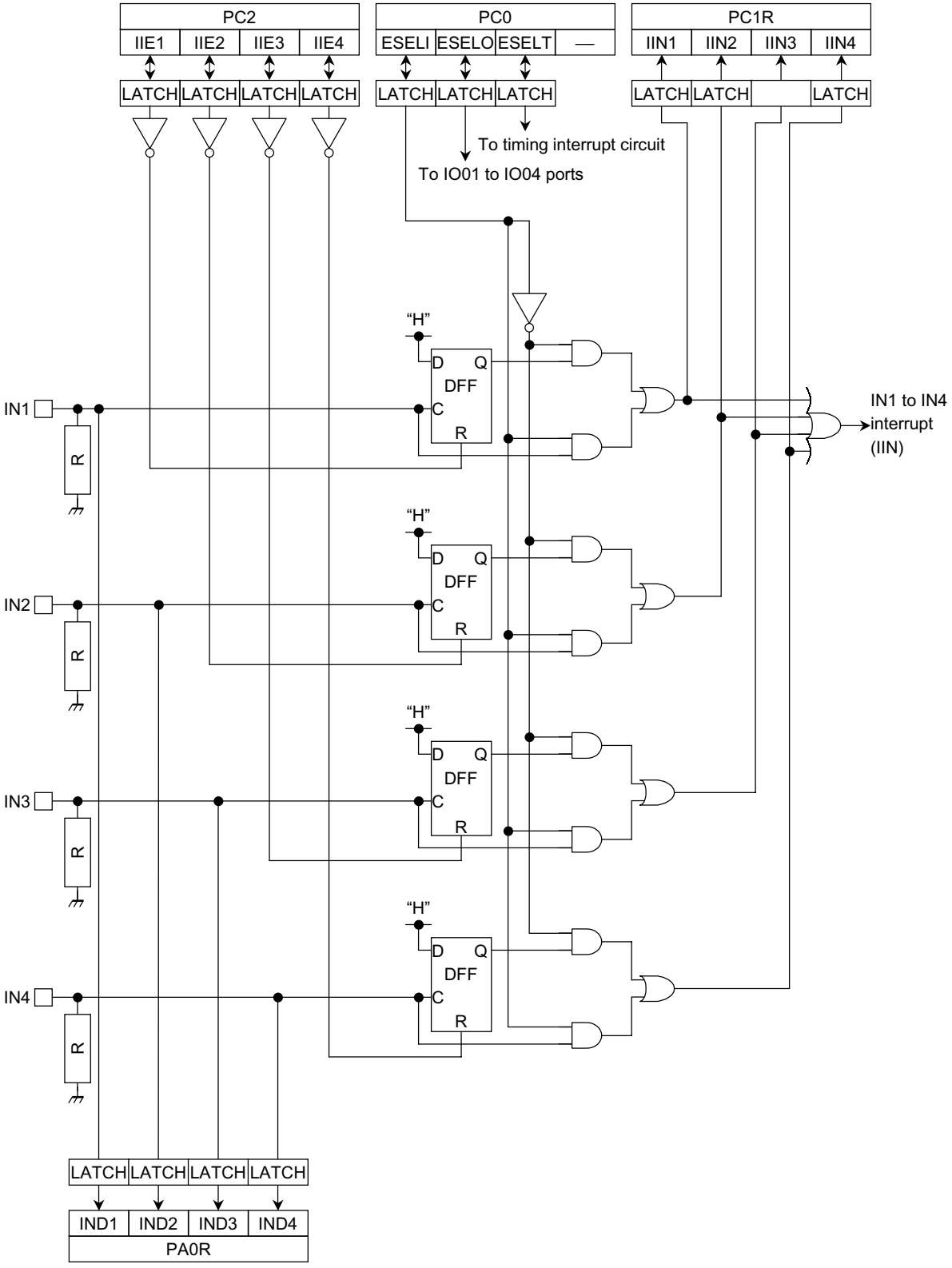


Figure 12 IN1 to IN4 interrupts

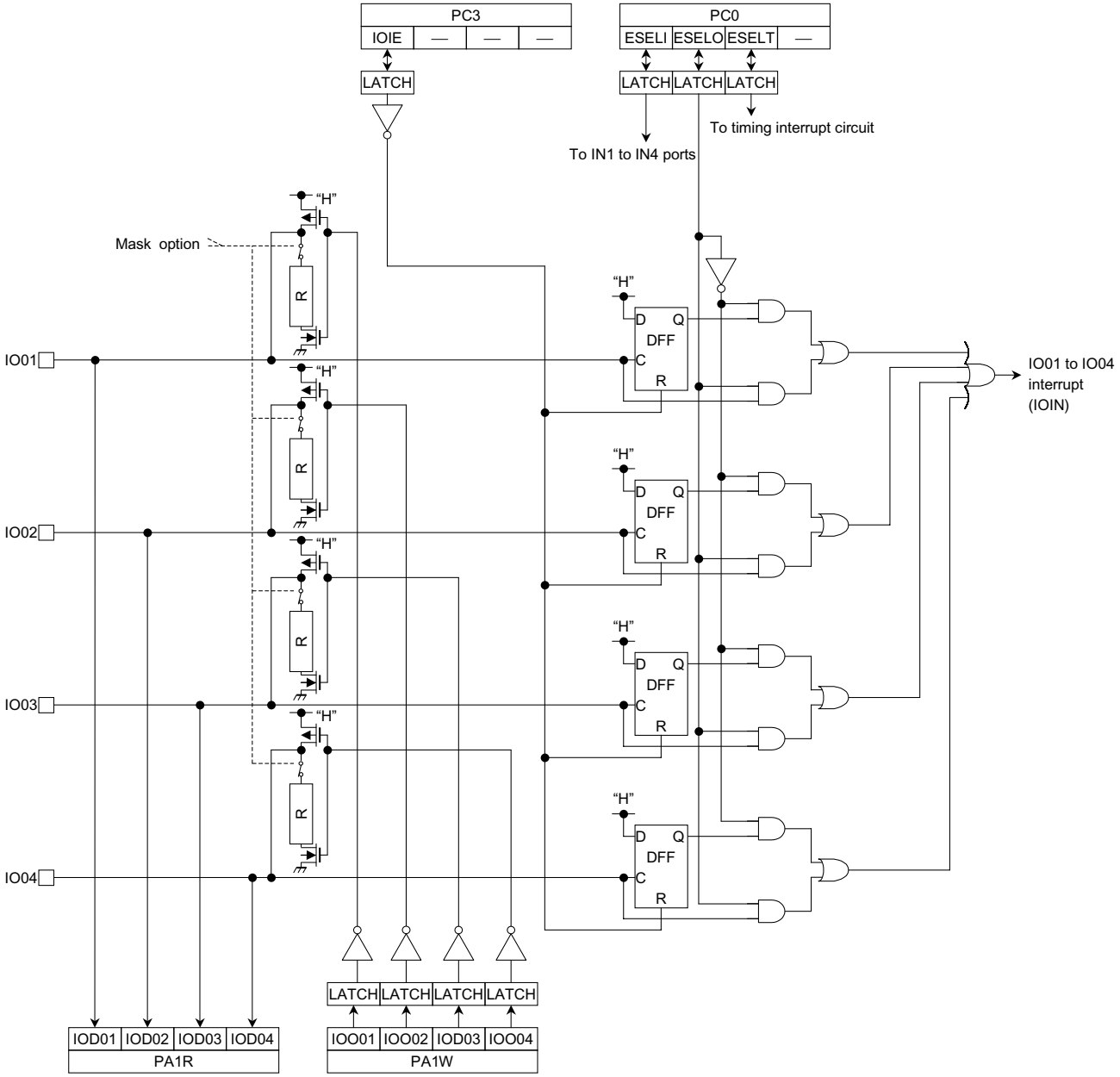


Figure 13 IO01 to IO04 interrupts

Note: Disabling input or input/output interrupts using PC2 or PC3 is valid only when a rising edge interrupt (see 4, Input/Output ports) is selected. If a level interrupt is selected, disabling interrupts using PC2 or PC3 is invalid.

2-2. Timing Interruption

(Timing Interruption selecting)

Timing Interruptions are selectable by Register file (PD1) 128/256, 16/32, 4/8, 1/2. 128/256, 16/32, 4/8 and 1/2 are initially 0 (1 Hz, 4 Hz, 16 Hz, 128 Hz is selected).

	MSB 3	2	1	0 LSB
PD1	1/2	4/8	16/32	128/256

128/256 = 0 128 Hz INT. select
1 256 Hz INT. select
16/32 = 0 16 Hz INT. select
1 32 Hz INT. select
4/8 = 0 4 Hz INT. select
1 8 Hz INT. select
1/2 = 0 1 Hz INT. select
1 2 Hz INT. select

(Timing Interruption enable/disable)

Selected Timing Interruption can be controlled enable/disable by Register file (PD3) TIE1 to TIE4 (R53).

TIE1 to TIE4 are initially 0 (disable).

	MSB 3	2	1	0 LSB
PD3	TIE4	TIE3	TIE2	TIE1

TIE1 = 0 1 Hz or 2 Hz INT. disable
1 1 Hz or 2 Hz INT. enable
TIE2 = 0 4 Hz or 8 Hz INT. disable
1 4 Hz or 8 Hz INT. enable
TIE3 = 0 16 Hz or 32 Hz INT. disable
1 16 Hz or 32 Hz INT. enable
TIE4 = 0 128 Hz or 256 Hz INT. disable
1 128 Hz or 256 Hz INT. enable

(Timing Interruption Reset)

The timing interruption for the selected timing interruption is reset by register files TIR1 to TIR4 (PD2W).

TIR1 to TIR4 are initially 0 (disable).

	MSB 3	2	1	0 LSB
PD2W	TIR4	TIR3	TIR2	TIR1

TIR1 = 1 1 Hz or 2 Hz Interruption reset
TIR2 = 1 4 Hz or 8 Hz Interruption reset
TIR3 = 1 16 Hz or 32 Hz Interruption reset
TIR4 = 1 128 Hz or 256 Hz Interruption reset

(Timing Interruption Read)

Selected Timing Interruption can be read by Register file TI1 to TI4 (PD0R).

	MSB 3	2	1	0 LSB
PD0R	TI4	TI3	TI2	TI1

TI1: Interruption data of 1 Hz or 2 Hz
TI2: Interruption data of 4 Hz or 8 Hz
TI3: Interruption data of 16 Hz or 32 Hz
TI4: Interruption data of 128 Hz or 256 Hz

(Interruption Edge Selection)

TIN Interruption can be selected the reading point (↑ or ↓) by Register file ESELT.

ESTLT is initially 0 (rising edge).

	MSB 3	2	1	0 LSB
PC0	—	ESELT	(ESLIO)	(ESELI)

ESELT = 0: Interruption at rising Edge of Timing INT.
1: Interruption at down Edge of Timing INT.

Example

```
LD 51O, 01H (256 Hz, 16 Hz, 4 Hz and 1 Hz select)
  ↓
LD 53O, 07H (256 Hz disable, 16 Hz, 4 Hz, 1 Hz enable)
  ↓   When the 1Hz interruption occurs.
LD M, 50O (read timing interruption)
  ↓   Recognize 1Hz interruption.
LD 52O, 01H (reset 1Hz interruption)
```

Note: A mode transition from CPM1 or CPM3 to CPM2 or from CPM2 to CPM1 or CPM3 causes the timings of binary counters 7-21 to change. Therefore, the timing interrupts also have their timings changed.

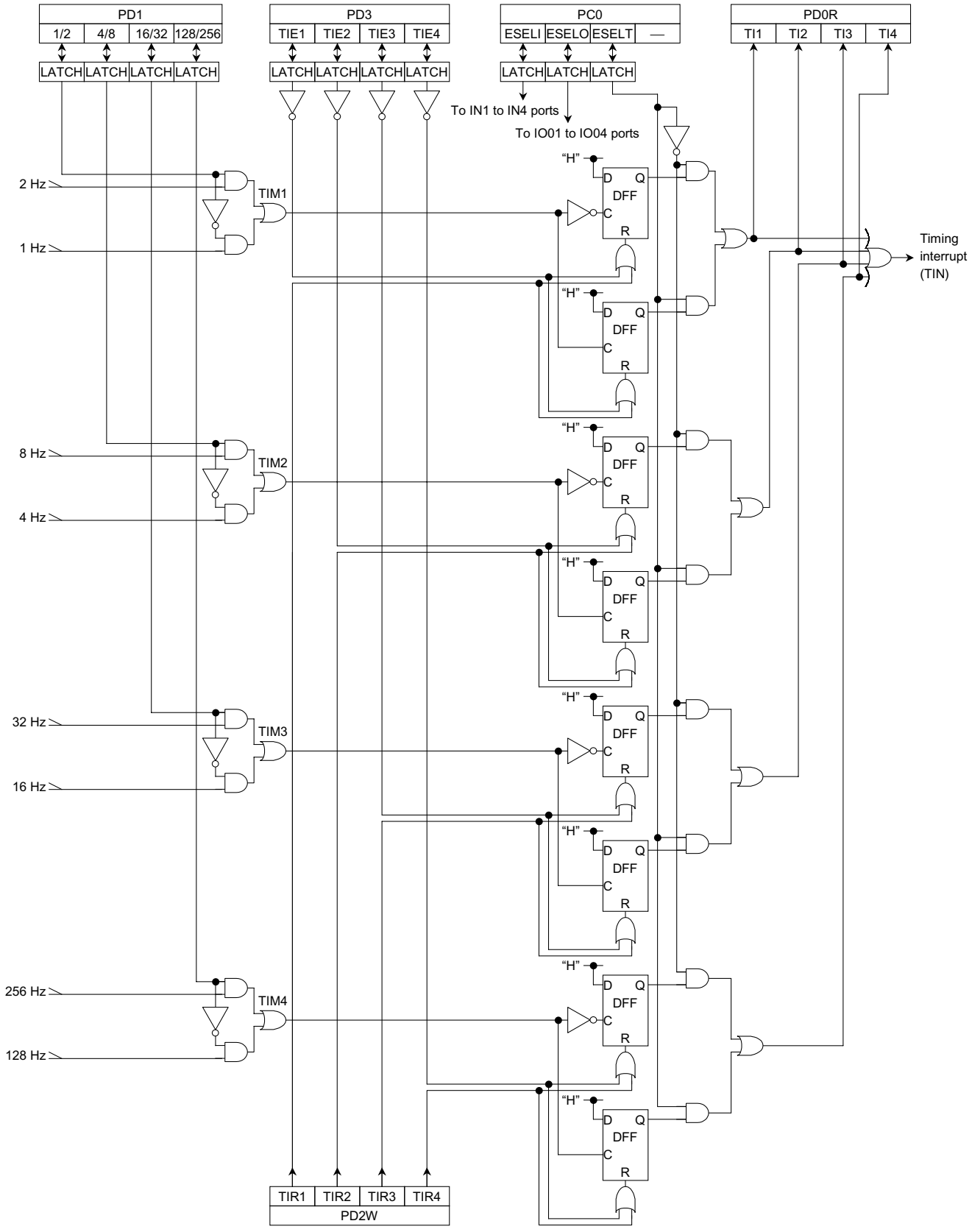
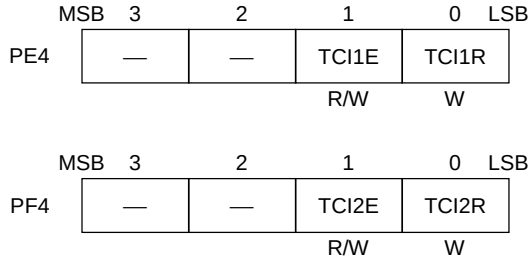


Figure 14 Timing interrupt circuit

2-3. 8 bits/16 bits Timer Counter Interruption

When Timer/Counter1, 2 overflow or coincide with setting Time/Count each Interruption occurs.



TCI1E/TCI2E = 0 Timer/Counter1, 2 Interruption disable
= 1 Timer/Counter1, 2 Interruption enable
TCI1R/TCI2R = 1 Timer/Counter1, 2 Interruption reset

TCI1E, TCI2E and TCI2R are initially 0 (DISABLE).

3. Timer/Counter

The Timer/Counter circuit can use as 8 bit × 2ch or 16 bit × 1ch Timer/Counter.
And there Time/Counter can be use as general Timer/Counter, Watch Dog Timer, or Multi Interruption Timer.
8 bits/16 bits can be changed by Register file TCPS. And input frequency also can be changed by Register CKS11 to CKS13 and CKS21 to CKS23, as follows.

	MSB 3	2	1	0 LSB
PE2	—	CKS13	CKS12	CKS11

	MSB 3	2	1	0 LSB
PF2	TCPS	CKS23	CKS22	CKS21

CKS 11	CKS 12	CKS 13	Input Frequency for Timer Counter1 (f_H = 2 MHz、f_L = 32 kHz)	
0	0	0	$f_H/2^{21}$ ($f_L/2^{15}$)	1 Hz (1.0 s)
1	0	0	$f_H/2^{12}$ ($f_L/2^{6}$)	512 Hz (19.5 ms)
0	1	0	$f_H/2^{8}$ ($f_L/2^{2}$)	2^{13} Hz (122 μs)
1	1	0	$f_H/2^{3}$	2^{18} Hz (3.81 μs)
—	—	1	OFF	

CKS 21	CKS 22	CKS 23	Input Frequency for Timer Counter2 (f_H = 2 MHz、f_L = 32 kHz)	
0	0	0	$f_H/2^{15}$ ($f_L/2^{9}$)	64 Hz (15.6 ms)
1	0	0	$f_H/2^{9}$ ($f_L/2^{3}$)	2^{12} Hz (244 μs)
0	1	0	$f_H/2^{5}$	2^{16} Hz (15.2 μs)
1	1	0	$f_H/2^{2}$	2^{19} Hz (1.90 μs)
—	—	1	OFF	

TCPS = 0 8 bit × 2 ch Timer/Counter
= 1 16 bit × 1 ch Timer/Counter

(When Timer/Counter is used as 16 bits timer, TIMER2 is used as lower bits.
And CKS11 to CKS13 are ignored. Input Frequency is decided by CKS21 to CKS23.)

CKS11 to CKS13, CKS21 to CKS23 and TCPS are initially 0.
(Timer/Counter1 : 1Hz, Timer/Counter2: 64 Hz, 8 bit × 2 ch)

CAUTION: 256 kHz of Timer/Counter1, 512 kHz, 64 kHz of Timer/Counter2 can be used when High-speed OSC is on.

Timer function can be selected by Register file/WDT1 and CMPEN1, 2.
Timer/Counter1 can be used as Watch Dog Timer.
And Input Frequency can be controlled by Register file TC1EN and TC2EN.
Timer/Counter is resetted by Register file TC1R, TC2R.

	MSB 3	2	1	0 LSB
PE3	TC1EN	TC1R	CMPEN1	WDT1
	R/W	W	R/W	R/W

	MSB 3	2	1	0 LSB
PF3	TC2EN	TC2R	CMPEN2	(Note)
	R/W	W	R/W	

Note: Writing 1 invalidates TC2 interrupts.

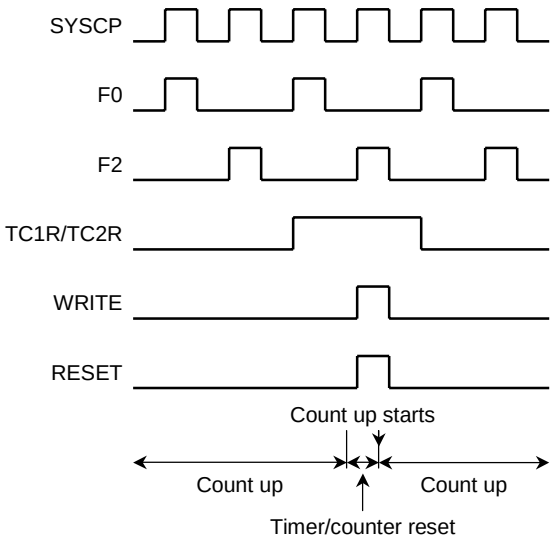
Timer/Counter1 setting is made in PE3.
Timer/Counter2 setting is made in PF3.

All the bits of PE3 and PF3 are initially 0.

PE3 WDT1 = 0: Used as 8-bit Timer/Counter.
= 1: Used as Watchdog Timer.
CMPEN1 = 0: An interrupt is generated if Timer/Counter1 overflows.
(The entire system is reset if WDT1 = 1.)
= 1: An interrupt is generated if Timer/Counter1 values match Time/Count set values
(The entire system is reset if WDT1 = 1.)
TC1R = 1: Timer/Counter1 is reset (cleared).
Timer/Counter1 resumes counting up after reset. (Refer to the timing chart below.)
TC1EN = 0: Reference clock input on Timer/Counter1 is stopped.
= 1: Reference clock input on Timer/Counter1 is started.

PF3 BIT 0 = 1: Timer/Counter2 cannot be used as 8-bit Timer/Counter.
= 0: Timer/Counter2 is used as 8-bit Timer/Counter.
CMPEN2 = 0: An interrupt occurs if Timer/Counter2 overflows.
= 1: An interrupt occurs if Timer/Counter2 values match Time/Count set values.
TC2R = 1: Timer/Counter2 is reset (cleared).
Timer/Counter2 resumes counting up after reset. (Refer to the timing chart below.)
TC2EN = 0: Reference clock input on Timer/Counter2 is stopped.
= 1: Reference clock input on Timer/Counter2 is started.

Timing chart for timer/counter 1/2 reset



Timer/Counter1,2 data can read from Register file TCR11 to TCR18 and TCR21 to TCR28.

	MSB 3	2	1	0 LSB
PE0R	TCR14	TCR13	TCR12	TCR11
PE1R	TCR18	TCR17	TCR16	TCR15
PF0R	TCR24	TCR23	TCR22	TCR21
PF1R	TCR28	TCR27	TCR26	TCR25

Timer/Counter1, 2 Comparison data is set by Register file SET11 to SET18 and SET21 to SET28.

	MSB 3	2	1	0 LSB
PE0W	SET14	SET13	SET12	SET11
PE1W	SET18	SET17	SET16	SET15
PF0W	SET24	SET23	SET22	SET21
PF1W	SET28	SET27	SET26	SET25

SET11 to SET18 and SET21 to SET28 are initially 0.

CAUTION:

1. When generating an interrupt for the timer/counter by comparing it with the setup value (SET11 to SET18, SET21 to SET28) or resetting the system, set the setup values in register files SET11 to SET18 and SET21 to SET28 before enabling CMPEN1 and CMPEN2.
2. When generating an interrupt by a 16-bit timer by comparing it with the setup value, enable all of CMPEN1, CMPEN2, TC1EN, and TC2EN using instructions.
3. Since the setup values and timer/counter values both are 0 after initialization, an interrupt is generated or the system is reset immediately when CMPEN1 is enabled.
4. Since a mode transition from CPM1 or CPM3 to CPM2 or from CPM2 to CPM1 or CPM3 causes the timing of the binary counters 7-21 to change, the timer/counters also have their timings changed.
5. Do not change the timer/counter from 8 bits to 16 bits in the middle of operation after the timer/counter has started counting, because such a change could cause the data to be destroyed.

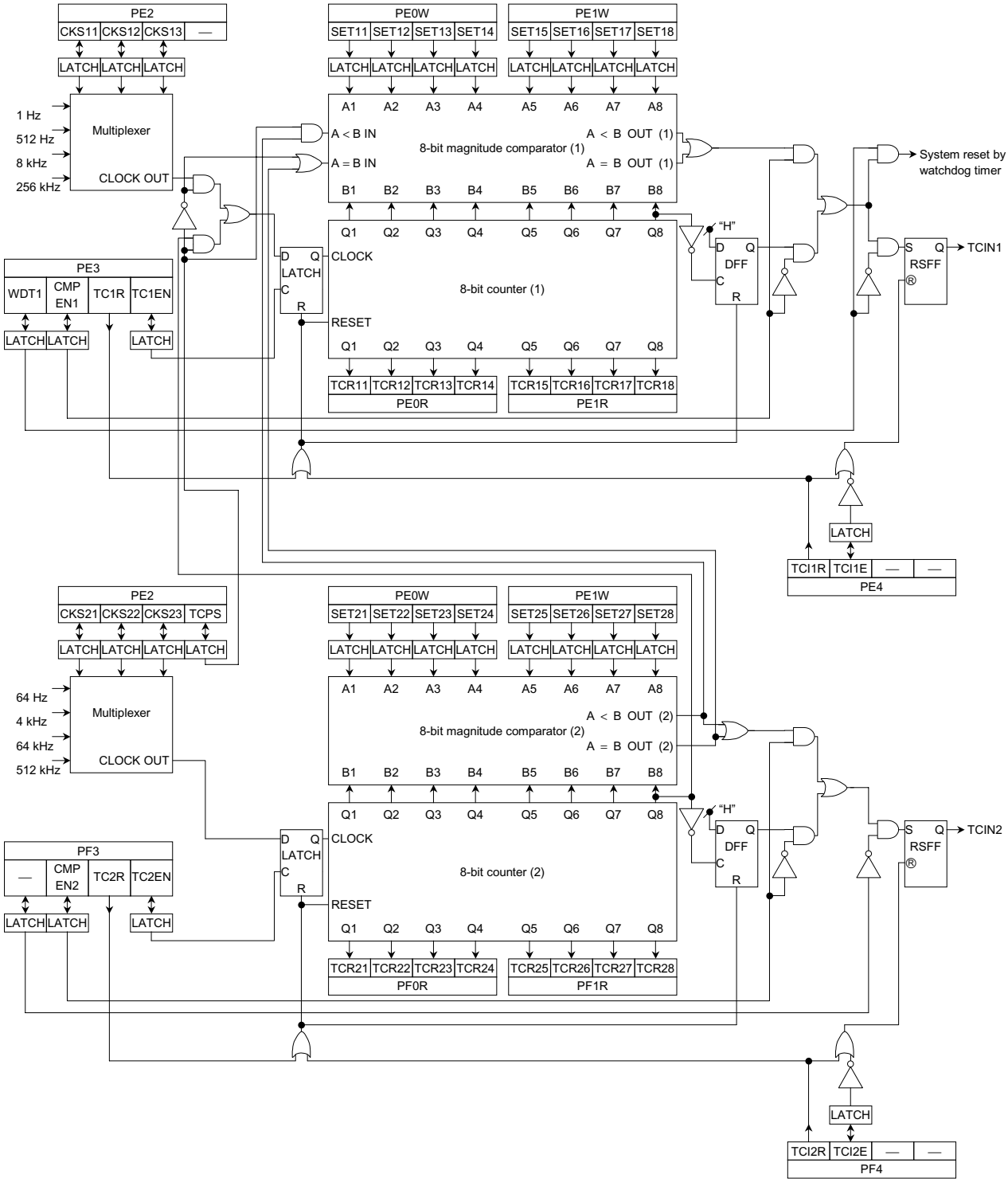


Figure 15 Timer/Counter

4. Input/IO Ports (Refer to Figure 21)

TMP04CH01FXXX has 4 inputs and 12 I/O ports.
4 input and 4 I/O ports have Interruption.
Also, these ports have a mask option available.

4-1. Input (IN1 to IN4)

Each input data can be read by Register file IND1 to IND4.

	MSB 3	2	1	0 LSB
PA0R	IND4	IND3	IND2	IND1

Each input Interruption function can be set enable/disable by Register file IIE1 to IIE4.

	MSB 3	2	1	0 LSB
PC2	IIE4	IIE3	IIE2	IIE1

IIE1 to IIE 4 = 0 IN1 to IN4 each Interruption disable
= 1 IN1 to IN4 each Interruption enable

Note 1: IIE1 to IIE4 interrupt disable/enables are register files that are effective when rising-edge interrupts are selected.
When level interrupts are selected, interrupts are disabled/enabled by the data input from ports. In this case, therefore, interrupts cannot be disabled/enabled by the register files. After the level-triggered interrupt is selected, do not apply 61-μs or less pulse (low speed, two cycles) to the IN pin. Malfunction may occur.

4 inputs (IN1 to IN4) Interruption data can be read by Register file IIN1 to IIN4.

	MSB 3	2	1	0 LSB
PC1R	IIN4	IIN3	IIN2	IIN1

Note 2 Interrupt data IO01 to IO04 cannot be read out. Only the data input form ports can be read out. (refer to Figure 13.)
Interrupt timings (rising edge/evel) can be selected using register file ESELI.

	MSB 3	2	1	0 LSB
PC0	—	(ESELT)	(ESELIO)	ESELI

ESELI = 0 IN1 to IN4: Interruption at rising edge of input INT.
1 IN1 to IN4: High level of input INT.

Input level-triggered interrupts are possible when ESELI = 1. In this case, if interrupts have been enabled by register files INT0-4, the interrupt remain asserted while the input level is high.

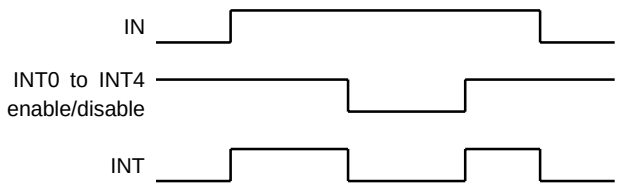


Figure 16 Interruption by high level-read

4-2. I/O ports (IO01 to IO04, IO11 to IO14, IO21 to IO24)

Each input data can be read by following Register file, when using input port.

	MSB 3	2	1	0 LSB
PA1R	IOD04	IOD03	IOD02	IOD01
R14R	IOD14	IOD13	IOD12	IOD11
R15R	IOD24	IOD23	IOD22	IOD21

IOD01 to IOD04 have interruption, each interruption can be disable/enable by register file IOIE0. (Four interrupt sources are collectively disabled/enabled by IOIE0.)

	MSB 3	2	1	0 LSB
PC3	—	—	—	IOIE0

IOIE0 = 0 IO01 to IO04 are disabled.
1 IO01 to IO04 are enabled.

Note: The IO01 to IO04 interrupt disable/enables are the register files that are effective when rising-edge interrupts are selected.
When level interrupts are selected, interrupts are disabled/enabled by the data input from ports. In this case, therefore, interrupts cannot be disabled/enabled by the register files.
After the level-triggered interrupt is selected, do not apply 61-μs or less pulse (low speed, two cycles) to the IO0 pin. Malfunction may occur.

IO01 to IO04 Interruption recoginized timing (rising edge/High level) can be selected by register file ESELIO.

	MSB 3	2	1	0 LSB
PC0	—	(ESELT)	ESELIO	(ESELI)

ESELIO = 0 Interruptions IO01 to IO04 are rising edge-triggered.
1 Interruptions IO01 to IO04 level-triggered.

Output data can be read by following register file, when using each I/O ports as output.

	MSB 3	2	1	0 LSB
RA1W	IOO04	IOO03	IOO02	IOO01
R14W	IOO14	IOO13	IOO12	IOO11
R15W	IOO24	IOO23	IOO22	IOO21

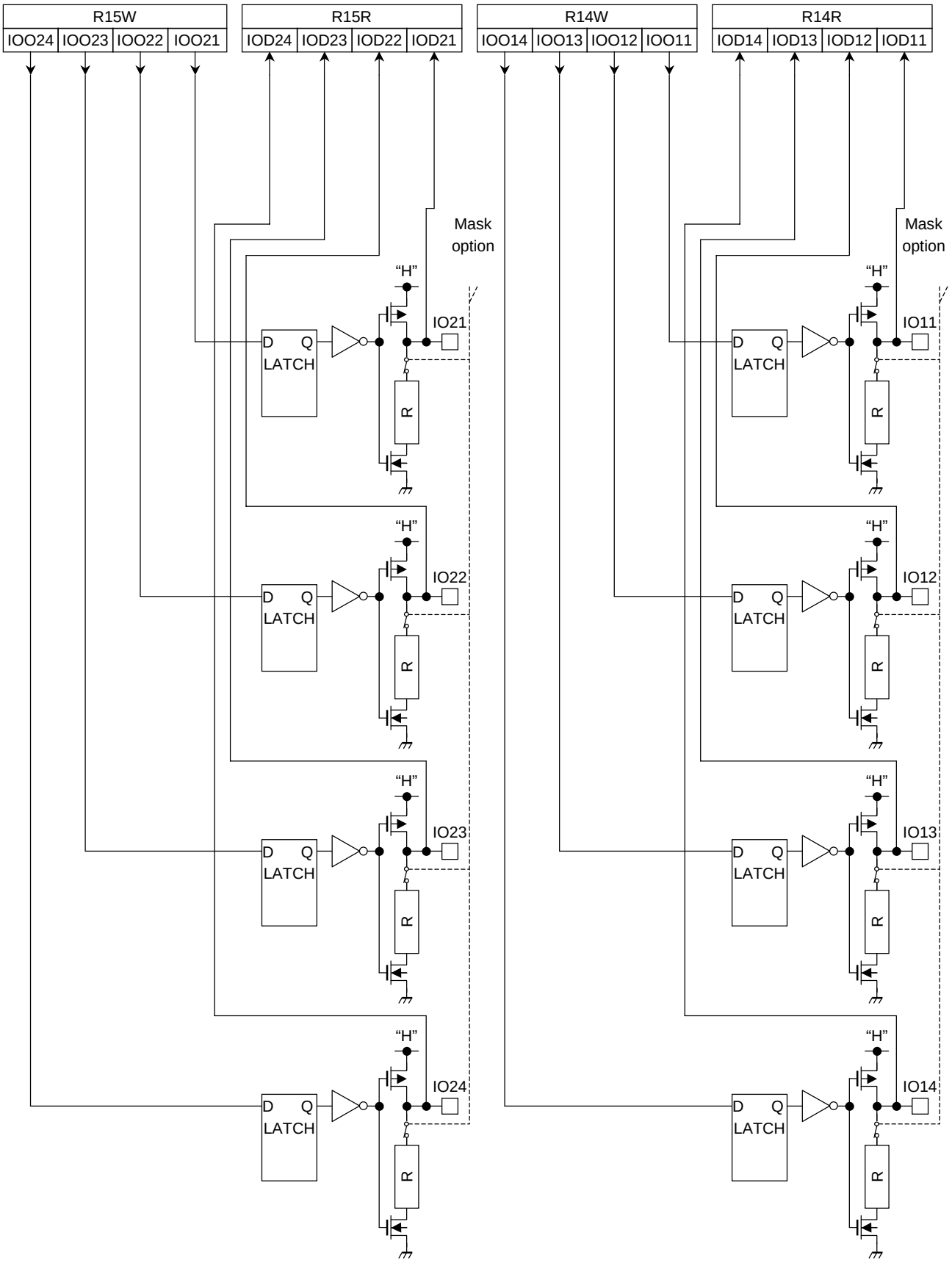


Figure 17 IO11 to IO14, IO21 to IO24

5. Buzzer Circuit

Buzzer sound can be selected by Register file BZ1, BZ2, BZ3 and 2k/4k.

	MSB 3	2	1	0 LSB
PE7	2 k/4 k	BZ3	BZ2	BZ1

2 k/4 k = 0 Basic frequency 2 kHz
= 1 Basic frequency 4 kHz

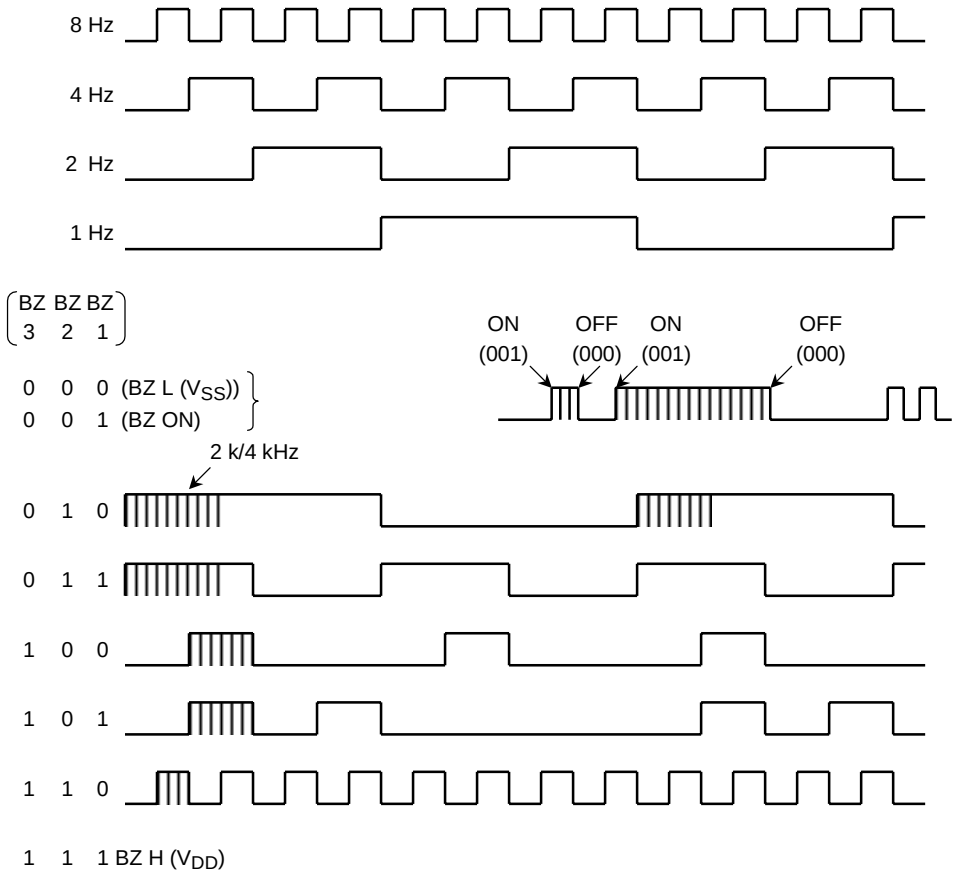
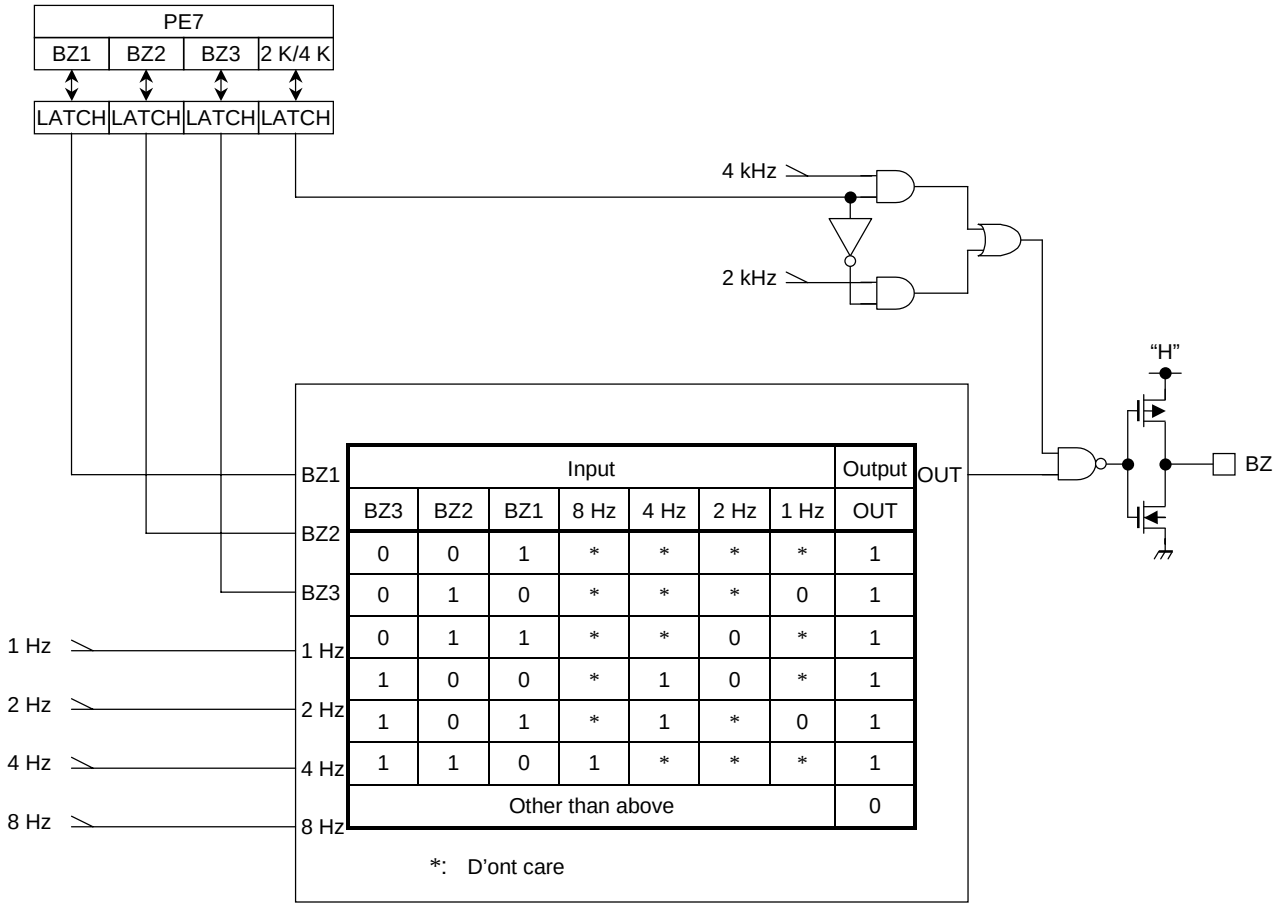


Figure 18 Buzzer sound

Buzzer sound can be made by software using (000), (001) or (000), (111) setting, as above.
When the Register file R67 is set the above ((BZ3, BZ2, BZ1) = (010) to (110)), each Buzzer sound is continuously released setting (BZ3, BZ2, BZ1) to (000).

Note: The above buzzer sounds are shown with respect to timings in the CPM2 mode where the high-speed oscillation frequency is 2 MHz, the CPM1/3 mode where the low-speed oscillation frequency is 32 kHz, and in the HALT mode.



Input							Output
BZ3	BZ2	BZ1	8 Hz	4 Hz	2 Hz	1 Hz	OUT
0	0	1	*	*	*	*	1
0	1	0	*	*	*	0	1
0	1	1	*	*	0	*	1
1	0	0	*	1	0	*	1
1	0	1	*	1	*	0	1
1	1	0	1	*	*	*	1
Other than above							0

*: D'ont care

Figure 19 Buzzer circuit

6. LCD Circuit

The LCD driver circuit has common signals and segment signals to drive 4.5 V, 1/16 duty, 1/4 bias LCD.

Duty	Frame Frequency	Common	Segment
1/16	97.5 Hz	COM1 to COM16	S_1 to S_{52}

The LCD driver circuit is controlled by Register file both DSTA and DON, and Display RAM is enable on DRCE = 1

	MSB 3	2	1	0 LSB
PC6W	—	DRCE	DON	DSTA

DON	DSTA	Behavior of LCD Driver
0	0	The booster circuit (Quadrupler) is turned off and all common & segment is fixed to V_{SS} level. LCD shows full off display.
1	1	The booster circuit (Quadrupler) is turned on and LCD driver is enabled to display the data on Display RAM.
Other than above		The setting other than above can cause mal-function. Do not set.

DRCE = 0 disable Display RAM
= 1 enable Display RAM

CAUTION:

1. Display signals from segment and common are made by the clock which come from low- speed oscillation. Even though the high-speed oscillator may be operating no display is output unless the low-speed oscillator is operating.
2. Register file DON and DSTA are read to Display Driver circuit by the clock which is made by LOWCP. When the LOWCP is needed OFF it is needs max. 103 ms after changing the data of DON and DSTA.

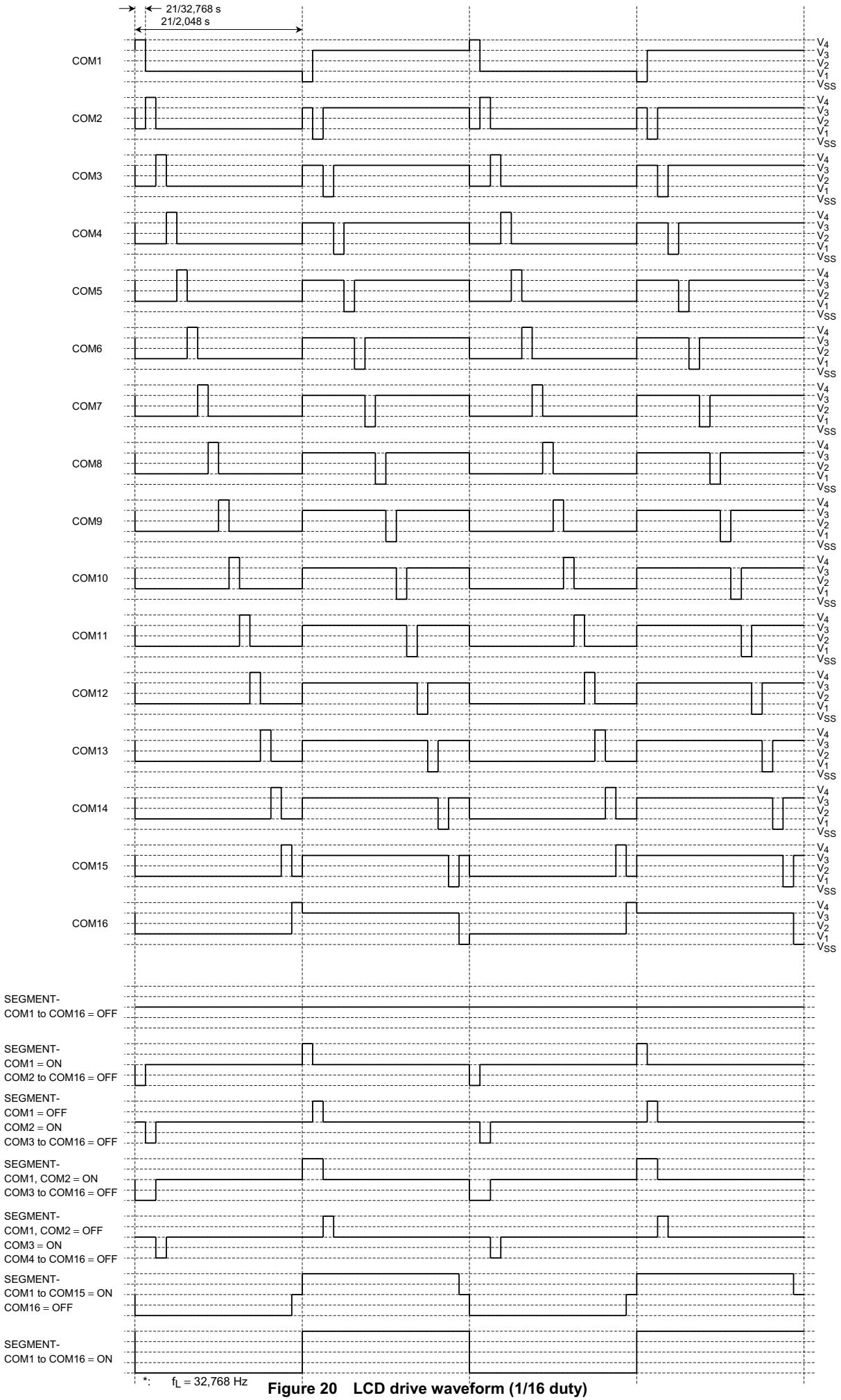


Figure 20 LCD drive waveform (1/16 duty)

7. Mask option

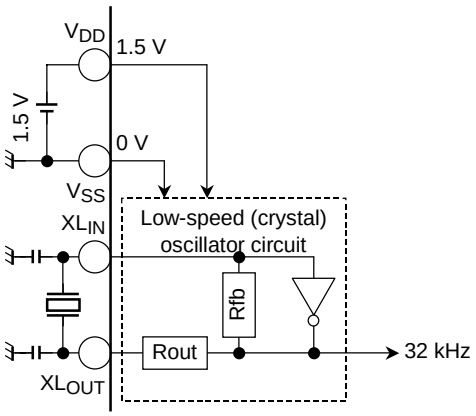
TMP04CH01FXXX has 8 Mask option.

Mask code	Battery	IN	I00	I01	I02	High-speed OSC	Low-speed OSC	Remark
A11F1	1.5 V	IN (1)	I/O (1)	I/O (1)	I/O (2)	CR	X'tal	(*)
A11F3	1.5 V	IN (1)	I/O (1)	I/O (1)	I/O (2)	CR	CR	(*)
A32F0	3.0 V	IN (1)	I/O (2)	I/O (2)	I/O (2)	X'tal	X'tal	(*)
A32F1	3.0 V	IN (1)	I/O (2)	I/O (2)	I/O (2)	CR	X'tal	(*)
A32F3	3.0 V	IN (1)	I/O (2)	I/O (2)	I/O (2)	CR	CR	(*)
A33F0	3.0 V	IN (1)	I/O (1)	I/O (1)	I/O (1)	X'tal	X'tal	(*)
A33F1	3.0 V	IN (1)	I/O (1)	I/O (1)	I/O (1)	CR	X'tal	—
A33F3	3.0 V	IN (1)	I/O (1)	I/O (1)	I/O (1)	CR	CR	(*)

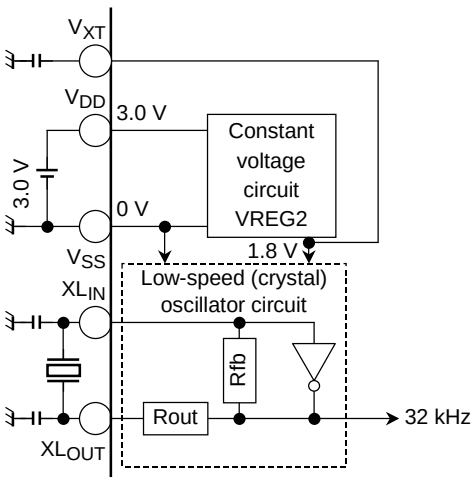
(*) Under development

(1) Supply voltage

Either 1.5 V or 3.0 V can be selected as the supply voltage. When 3.0 V is used, the low-speed oscillator circuit is driven by output from the internal constant voltage circuit (V_{REG2}) thus reducing current dissipation.



When 1.5 V selected



When 3.0 V selected

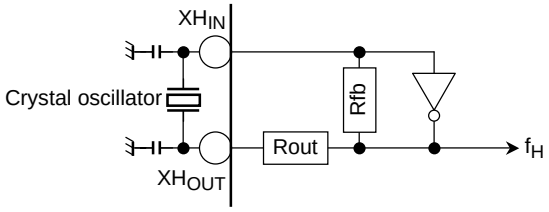
(2) Input/Output port types

Either CMOS output or P-channel open drain can be selected in units of four bits for the input/output pins: IO01 to IO04, IO11 to IO14, IO21 to IO24. For port types, see the Diagram of Input/Output Port Types.

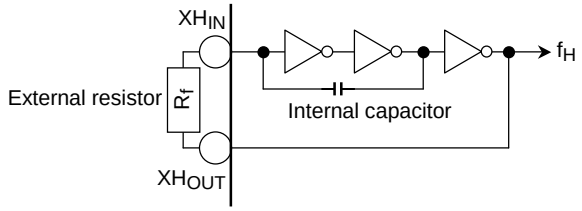
(3) High-speed oscillator circuit

Either the crystal or the CR oscillator circuit can be selected as the high-speed oscillator circuit.

Note: After a reset, the CPU starts operating using the high-speed clock as the system clock. Therefore, even if only a low-speed clock is used for the following processes, the high-speed oscillator circuit must operate normally at startup. Select either the crystal or the CR oscillator circuit and correctly connect the external component (crystal oscillator or resistor) to the XH_{IN}/XH_{OUT} pin.



When crystal oscillator circuit is selected

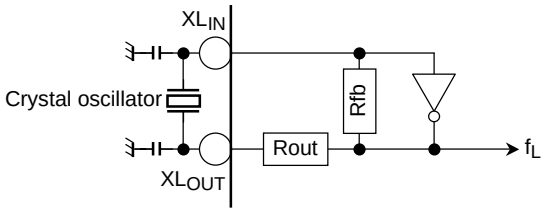


When CR oscillator circuit is selected

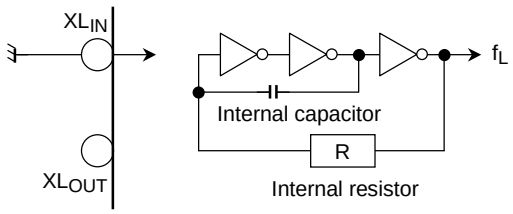
(4) Low-speed oscillator circuit

Either the crystal or the CR oscillator circuit can be selected as the low-speed oscillator circuit.

Note: A low-speed clock is used in the LCD driver circuit. To display the LCD, the low-speed oscillator circuit must be operated. When the CR oscillator circuit is selected, because both resistor and capacitor are built in, an external component is not required. Connect the XL_{IN} pin to V_{SS}. If the pin is left open, the internal circuit gates become unstable, possibly allowing surge current to flow.



When crystal oscillator circuit is selected



When CR oscillator circuit is selected

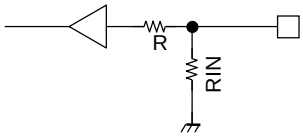
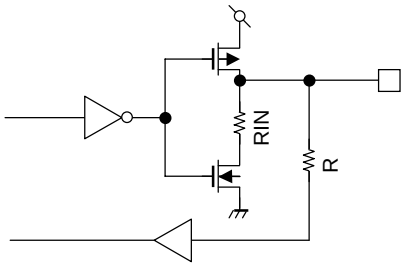
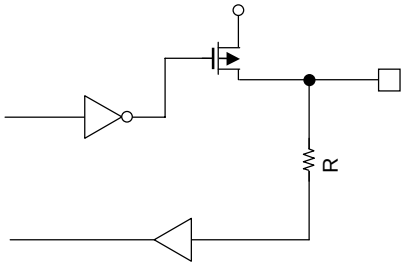
	Input/Output Circuit
IN1 (1)	
I/O (1)	
I/O (2)	

Figure 21 I/O port

RIN: Internal pull-down resistor, 400 kΩ (typ.)
R : Input protective resistor, 100 Ω (typ.)

Electrical Characteristics

Absolute Maximam Ratings (V_{SS} = 0 V)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 to 6.0	V
Input voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V
Power dissipation (T_{opr} = 80°C)	P_D	350	mW
Solder temperature	T_{sol}	260 (10 s)	°C
Storage temperature	T_{stg}	−55 to 125	°C
Operating temperature	T_{opr}	0 to 40	°C

Recommended operating condition

1.5V version (unless otherwise specified, V_{SS} = 0 V, T_{opr} = 0°C to 40°C)

Characteristics		Symbol	Test Condition		Min	Typ.	Max	Unit
Power supply voltage		V_{DD}	f_{XTH} = 200 kHz		1.2	1.5	1.8	V
Oscillation frequency		f_{XTL1}	V_{DD} = 1.2 V to 1.8 V	(Note 1)	—	32.768	—	kHz
		f_{XTL2}	V_{DD} = 1.5 V	(Note 2)	20	33	55	
		f_{XTH1}	V_{DD} = 1.5 V	(Note 3)	—	200	—	
Input voltage	"H" level	V_{IH}	V_{DD} = 1.3 V		$V_{DD} \times 0.8$	—	V_{DD}	V
			V_{DD} = 1.7 V		$V_{DD} \times 0.7$	—	V_{DD}	
	"L" level	V_{IL}	V_{DD} = 1.3 V		0	—	$V_{DD} \times 0.2$	
			V_{DD} = 1.7 V		0	—	$V_{DD} \times 0.3$	
Quadrupler capacitance		C_1, C_2	—		—	1.0	—	μF
Voltage capacitance		V_1	—		—	1.0	—	μF
		V_2	—		—	1.0	—	
		V_3	—		—	1.0	—	
		V_4	—		—	1.0	—	

Note 1: Crystal oscillation circuit is used for low-speed oscillator.

Note 2: Internal CR oscillator is used for low-speed oscillator.

Note 3: An CR oscillating circuit configured with an external R is used for the high-speed oscillator.

Oscillation

Characteristics	Symbol	Test Condition		Min	Typ.	Max	Unit
OSC starting voltage	V_{STA}	T_{STA} = 10 s, T_{opr} = 25°C	(Note 4)	1.4	—	—	V
OSC holding voltage	V_{HOLD}		(Note 4)	1.2	—	—	V
Frequency of internal CR OSC	f_{OSC1}	V_{DD} = 1.5 V	(Note 5)	20	33	55	kHz
Frequency of High-speed OSC	f_{OSC2}	V_{DD} = 1.5 V R_f = 150 kΩ	(Note 6)	—	200	—	kHz

Note 4: Crystal oscillation circuit for low-speed oscillator. Input 1.4 V or more at power-on.

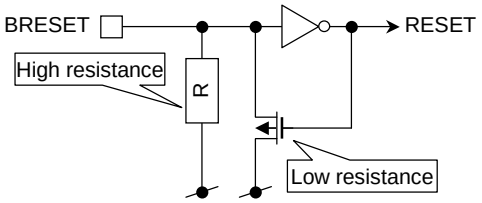
Note 5: Internal CR oscillator for low-speed oscillator.

Note 6: An CR oscillating circuit configured with an external R is used for the high-speed oscillator.

DC Characteristics

Characteristics	Symbol	Test Condition		Min	Typ.	Max	Unit
Input current (1) (IN1 to IN4, IO01 to IO04, IO11 to IO14,)	I_{IH1}	V_{DD} = 1.8 V, V_{IN} = 0 V		–500	—	500	nA
	I_{IL1}	V_{DD} = 1.8 V, V_{IN} = 1.8 V		3.21	4.5	7.5	µA
Input current (1-2) (IO21 to 24)	I_{IH1}	V_{DD} = 1.8 V, V_{IN} = 0 V		–500	—	500	nA
	I_{IL1}	V_{DD} = 1.8 V, V_{IN} = 1.8 V		–500	—	500	
Input current (2) (BRESET)	I_{IH2L} (Note)	V_{DD} = 1.8 V, V_{IN} = 0 V Low Resistor side		–60	–36	–25.7	µA
	I_{IH2H}	V_{DD} = 1.8 V, V_{IN} = 0 V High Resistor side		–6	–3.6	–2.57	
Input current (3) (TEST)	I_{IL3}	V_{DD} = 1.8 V, V_{IN} = 1.8 V		6.43	9.0	15.0	µA
Output current (1) (IO01 to 04, IO11 to 14)	I_{OH1}	V_{DD} = 1.2 V, V_{OH} = 0.7 V		—	—	–150	µA
	I_{OL1}	V_{DD} = 1.2 V, V_{OL} = 0.5 V		0.89	1.25	2.08	
Output current (1-2) (IO21 to 24)	I_{OH1}	V_{DD} = 1.2 V, V_{OH} = 0.7 V		—	—	–150	µA
Output current (2) (BZ)	I_{OH2}	V_{DD} = 1.2 V, V_{OH} = 0.7 V		—	—	–500	µA
	I_{OL2}	V_{DD} = 1.2 V, V_{OL} = 0.5 V		500	—	—	
Output current (3) (SEGMENT)	I_{OH3}	V_1 = 1.125 V, V_2 = 2.25 V, V_3 = 3.375 V, V_4 = 4.5 V	$V_{OH} = V_4 - 0.5$ V	—	—	–100	µA
	I_{OL3}		V_{OL} = 0.5 V	100	—	—	
	I_{OM3}		$V_{OM} = V_2 - 0.5$ V	—	—	–50	
Output current (4) (COMMON)	I_{OH4}	V_1 = 1.125 V, V_2 = 2.25 V, V_3 = 3.375 V, V_4 = 4.5 V	$V_{OH} = V_4 - 0.5$ V	—	—	–100	µA
	I_{OL4}		V_{OL} = 0.5 V	100	—	—	
	I_{OM4}		$V_{OM} = V_3 - 0.5$ V	—	—	–50	
	I_{OM4}		$V_{OM} = V_1 + 0.5$ V	50	—	—	
Quadrupler output	V_1	V_1 = 1.125 V, Ta = 25°C		1.075	1.125	1.175	V
	V_2			2.05	2.25	2.45	
	V_3			3.175	3.375	3.575	
	V_4			4.3	4.5	4.7	
Power supply current (1) (Low-speed crystel oscillation circuit)	I_{DDOP}	V_{DD} = 1.5 V, f_H = 200 kHz f_L = 32 kHz At High-speed operation	Display ON	—	48	77	µA
			Display OFF	—	—	73	
	I_{DDSLOW}	V_{DD} = 1.5 V, f_L = 32 kHz At Low-speed operation	Display ON	—	9.5	12	
			Display OFF	—	—	11	
	I_{DDHOLD}	V_{DD} = 1.5 V, f_L = 32 kHz In HOLD mode	Display ON	—	4	7	
			Display OFF	—	—	6	
	I_{DDSTOP}	V_{DD} = 1.5 V, In STOP mode		—	0.4	1	
Power supply current (2) (Low-speed CR oscillation circuit)	I_{DDOP}	V_{DD} = 1.5 V, f = 200 kHz f_L = Internal At High-speed operation	Display ON	—	50	77	µA
			Display OFF	—	—	73	
	I_{DDSLOW}	V_{DD} = 1.5 V, f_L = Internal At Low-speed operation	Display ON	—	12	17	
			Display OFF	—	—	16	
	I_{DDHOLD}	V_{DD} = 1.5 V, f_L = Internal In HOLD mode	Display ON	—	5	7.5	
			Display OFF	—	—	6.5	
	I_{DDSTOP}	V_{DD} = 1.5 V, In STOP mode		—	0.4	1	

Note: The BRESET pin is connected to V_{DD} (High level) via two resistors as shown below. To minimize the current that flows at reset, the low resistance consists of a P-channel FET. When the input level is V_{SS} (Low level), the FET is off. The resistance is ∞. The specified input current (2), I_{IH2L}, is the current that flows when the low resistance = P-channel FET is on. However, the low-resistance is off when VI_N = 0 V, so actual measurement is impossible.



V_{DD} = "High" level

Typical operating condition

3.0 V version (unless otherwise specified, V_{SS} = 0 V, T_{opr} = 0°C to 40°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Power supply voltage		V_{DD}	f_{XTH} = 2 MHz	2.4	3.0	3.6	V
Oscillation frequency		f_{XTL1}	V_{DD} = 2.4 V to 3.6 V (Note 1)	—	32.768	—	kHz
		f_{XTL2}	V_{DD} = 3.0 V (Note 2)	20	35	60	
		f_{XTH1}	V_{DD} = 2.4 V to 3.6 V (Note 3)	—	2.0	—	MHz
		f_{XTH2}	V_{DD} = 3.0 V (Note 4)	—	2.0	—	
Input voltage	"H" level	V_{IH}	V_{DD} = 2.4 V	$V_{DD} \times 0.8$	—	V_{DD}	V
			V_{DD} = 3.6 V	$V_{DD} \times 0.7$	—	V_{DD}	
	"L" level	V_{IL}	V_{DD} = 2.4 V	0	—	$V_{DD} \times 0.2$	
			V_{DD} = 3.6 V	0	—	$V_{DD} \times 0.3$	
Quadrupler capacitance		C_1, C_2	—	—	1.0	—	µF
Voltage capacitance		V_2	—	—	1.0	—	µF
		V_3	—	—	1.0	—	
		V_4	—	—	1.0	—	
		V_{XT}	—	—	1.0	—	

Note 1: Crystal oscillation circuit is used for low-speed oscillator.

Note 2: Internal CR oscillator is used for low-speed oscillator.

Note 3: Crystal oscillation circuit is used for high-speed oscillator.

Note 4: An CR oscillating circuit configured with an external R is used for the high-speed oscillator.

Oscillation

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
OSC starting voltage (Low-speed)	V_{STA1}	T_{STA} = 10 s, T_{opr} = 25°C	1.85	—	—	V
OSC starting voltage (High-speed)	V_{STA2}	T_{STA} = 8 ms	2.10	—	—	V
OSC holding voltage (Low-speed)	V_{HOLD1}	—	1.65	—	—	V
OSC holding voltage (High-speed)	V_{HOLD2}	—	1.90	—	—	V
Frequency of internal CR OSC	f_{OSC1}	V_{DD} = 3.0 V (Note 5)	20	35	60	kHz
Frequency of High-speed OSC	f_{OSC2}	V_{DD} = 3.0 V, R_f = 13.0 kΩ (Note 6)	—	2.0	—	MHz

Note 5: Internal CR oscillator for low-speed oscillator.

Note 6: An CR oscillating circuit configured with an external R is used for the high-speed oscillator.

DC Characteristics

Characteristics	Symbol	Test Condition		Min	Typ.	Max	Unit
Input current (1) (IN1 to IN4)	I_{IH1}	V_{DD} = 3.6 V, V_{IN} = 0 V		–500	—	500	nA
	I_{IL1}	V_{DD} = 3.6 V, V_{IN} = 3.6 V		6.43	9.0	15.0	µA
Input current (1-2) (IO01 to IO04, IO11 to IO14, IO21 to IO24) (Note 1)	I_{IH1}	V_{DD} = 3.6 V, V_{IN} = 0 V		–500	—	500	nA
	I_{IL1}	V_{DD} = 3.6 V, V_{IN} = 3.6 V		6.43	9.0	15.0	µA
Input current (1-3) (IO01 to IO04, IO11 to IO14, IO21 to IO24) (Note 2)	I_{IH1}	V_{DD} = 3.6 V, V_{IN} = 0 V		–500	—	500	nA
	I_{IL1}	V_{DD} = 3.6 V, V_{IN} = 3.6 V		–500	—	500	nA
Input current (2) (BRESET)	I_{IH2L}	V_{DD} = 3.6 V, V_{IN} = 0 V Low Resistor side		–120	–72	–51.4	µA
	I_{IH2H}	V_{DD} = 3.6 V, V_{IN} = 0 V High Resistor side		–12	–7.2	–5.14	
Input current (3) (TEST)	I_{IL3}	V_{DD} = 3.6 V, V_{IN} = 3.6 V		12.9	18.0	30.0	µA
Output current (1) (IO01 to IO04, IO11 to IO14, IO21 to IO24)	I_{OH1}	V_{DD} = 2.4 V, V_{OH} = 1.9 V		—	—	–1.5	mA
	I_{OL1} (Note 1)	V_{DD} = 2.4 V, V_{OL} = 0.5 V		0.89	1.25	2.08	µA
Output current (2) (BZ)	I_{OH2}	V_{DD} = 2.4 V, V_{OH} = 1.9 V		—	—	–2.0	mA
	I_{OL2}	V_{DD} = 2.4 V, V_{OL} = 0.5 V		2.0	—	—	
Output current (3) (SEGMENT)	I_{OH3}	V_{DD} = 3.0 V, V_{REG} = 1.125 V, V_2 = 2.25 V, V_3 = 3.375 V, V_4 = 4.5 V	V_{OH} = V_4 – 0.5 V	—	—	–100	µA
	I_{OL3}		V_{OL} = 0.5 V	100	—	—	
	I_{OM3}		V_{OM} = V_2 – 0.5 V	—	—	–50	
Output current (4) (COMMON)	I_{OH4}	V_{DD} = 3.0 V, V_{REG} = 1.125 V, V_2 = 2.25 V, V_3 = 3.375 V, V_4 = 4.5 V	V_{OH} = V_4 – 0.5 V	—	—	–100	µA
	I_{OL4}		V_{OL} = 0.5 V	100	—	—	
	I_{OM4}		V_{OM} = V_3 – 0.5 V	—	—	–50	
	I_{OM4}		V_{OM} = V_1 + 0.5 V	50	—	—	
Voltage regulater output	V_{REG1}	V_{DD} = 3.0 V, Ta = 25°C (Note 3)		1.075	1.125	1.175	V
	V_{REG2}	V_{DD} = 3.0 V, Ta = 25°C (Note 4)		—	1.8	—	
Quadrupler output	V_2	V_{DD} = 3.0 V, V_{REG} = 1.125 V, Ta = 25°C		2.05	2.25	2.45	V
	V_3			3.175	3.375	3.575	
	V_4			4.3	4.5	4.7	

Note 1: MASK CODE: A33F0, A33F1, A33F3

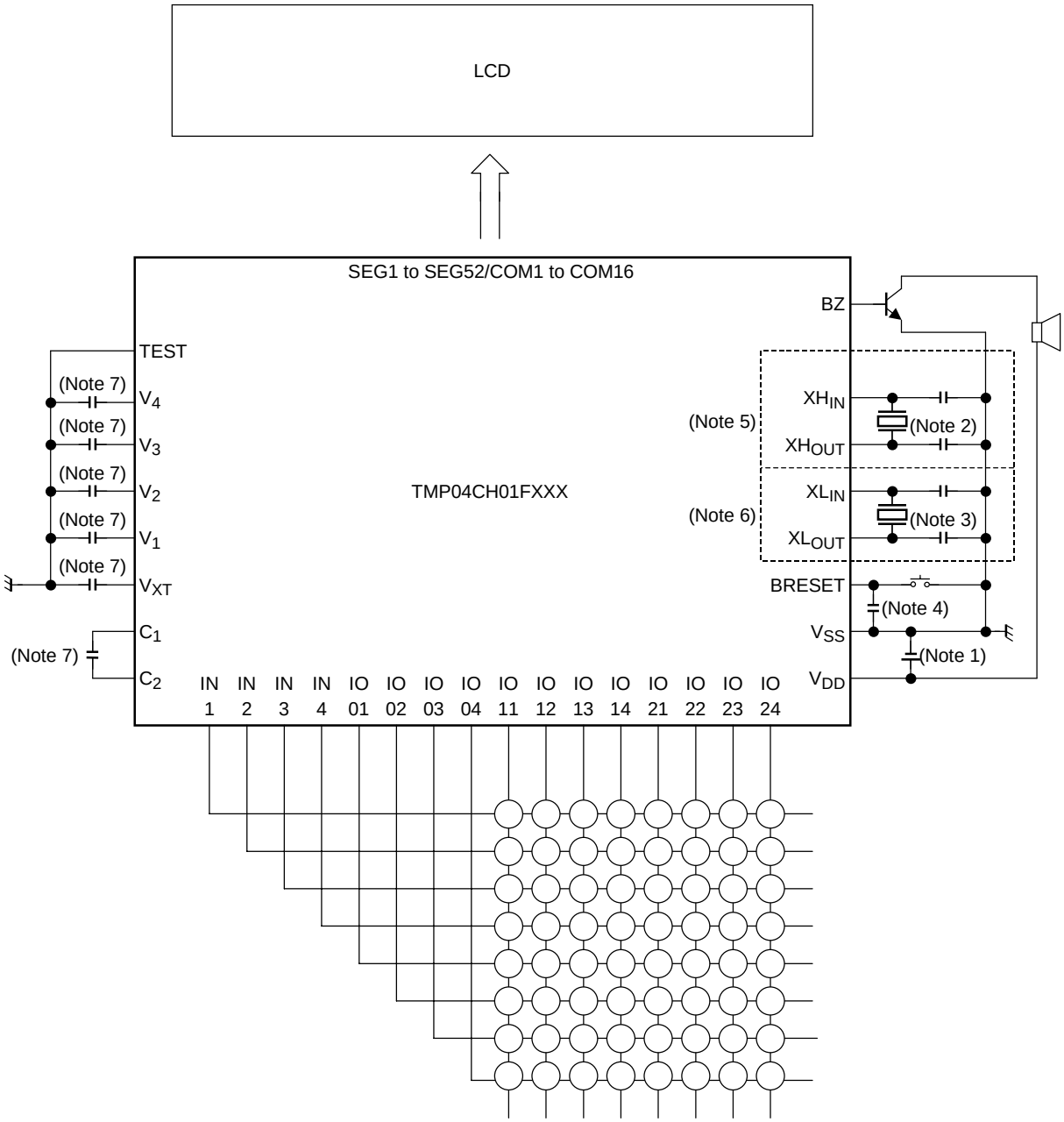
Note 2: MASK CODE : A32F0, A32F1, A32F3

Note 3: Voltage regulator for quadrupler

Note 4: Voltage output regulator for low-speed oscillator

Characteristics	Symbol	Test Condition		Min	Typ.	Max	Unit
Power supply current (1) (High-speed crystal oscillation circuit) (Low-speed crystal oscillation circuit)	I_{DDOP}	V_{DD} = 3.0 V, f_H = 2 MHz, f_L = 32 kHz At High-speed operation	Display ON	—	0.85	1.2	mA
			Display OFF	—	—	1.2	
	I_{DDSLOW}	V_{DD} = 3.0 V, f_L = 32 kHz At Low-speed operation	Display ON	—	17.0	24.0	µA
			Display OFF	—	—	23.0	
	I_{DDHOLD}	V_{DD} = 3.0 V, f_L = 32 kHz In HOLD mode	Display ON	—	5.5	11.0	
			Display OFF	—	—	10.0	
	I_{DDSTOP}	V_{DD} = 3.0 V In STOP mode		—	0.8	1.2	
Power supply current (2) (High-speed CR oscillation circuit) (Low-speed crystal oscillation circuit)	I_{DDOP}	V_{DD} = 3.0 V, f_H = 2 MHz, f_L = 32 kHz At High-speed operation	Display ON	—	0.85	1.5	mA
			Display OFF	—	—	1.5	
	I_{DDSLOW}	V_{DD} = 3.0 V, f_L = 32 kHz At Low-speed operation	Display ON	—	17.0	24.0	µA
			Display OFF	—	—	23.0	
	I_{DDHOLD}	V_{DD} = 3.0 V, f_L = 32 kHz In HOLD mode	Display ON	—	5.5	11.0	
			Display OFF	—	—	10.0	
	I_{DDSTOP}	V_{DD} = 3.0 V In STOP mode		—	0.8	1.2	
Power supply current (3) (High-speed CR oscillation circuit) (Low-speed CR oscillation circuit)	I_{DDOP}	V_{DD} = 3.0 V, f_H = 2 MHz, f_L = Internal At High-speed operation	Display ON	—	0.85	1.5	mA
			Display OFF	—	—	1.5	
	I_{DDSLOW}	V_{DD} = 3.0 V f_L = Internal At Low-speed operation	Display ON	—	23.0	40.0	µA
			Display OFF	—	—	39.0	
	I_{DDHOLD}	V_{DD} = 3.0 V, f_L = Internal In HOLD mode	Display ON	—	6.5	14.0	
			Display OFF	—	—	12.0	
	I_{DDSTOP}	V_{DD} = 3.0 V In STOP mode		—	0.8	1.4	

Example of Application Circuit



Note 1: Either 1.5 V or 3 V can be selected as the supply voltage.

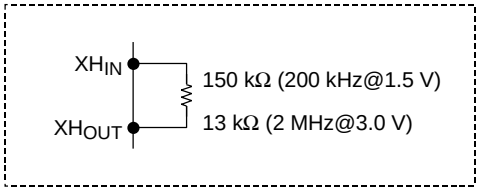
Note 2: Recommended high-speed oscillator circuit capacitor: 22 pF

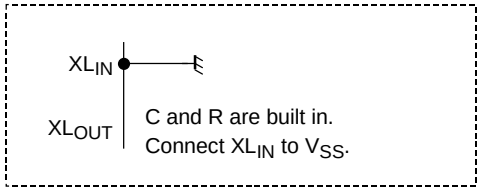
Note 3: Recommended low-speed oscillator circuit capacitor: 15 pF

Note 4: Insert a 0.1 μF capacitor between BRESET and V_{SS}.

Note 5: High-speed CR oscillator circuit (optional)

Note 6: Low-speed CR oscillator circuit (optional)

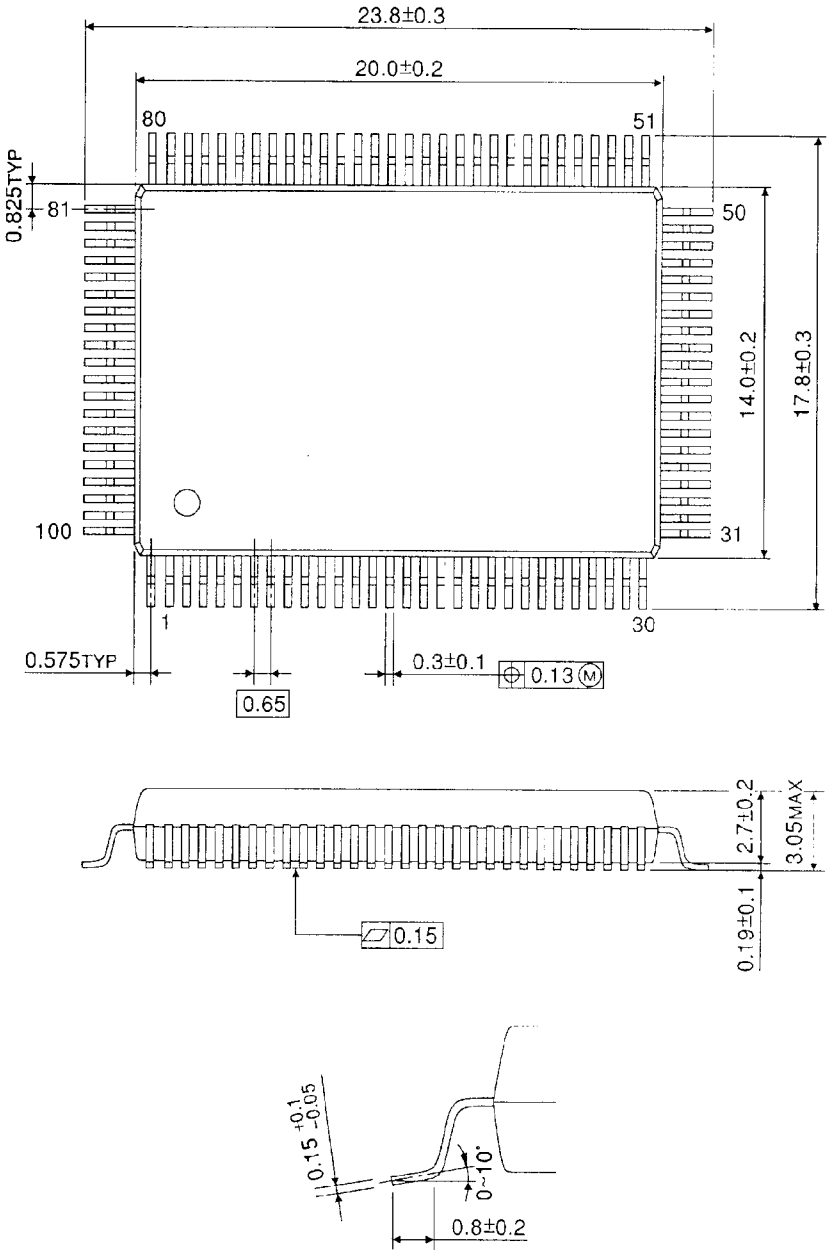




Note 7: Adjust between 0.1 to 1.0 μF depending on the size of the LCD panel used.

Package Dimensions

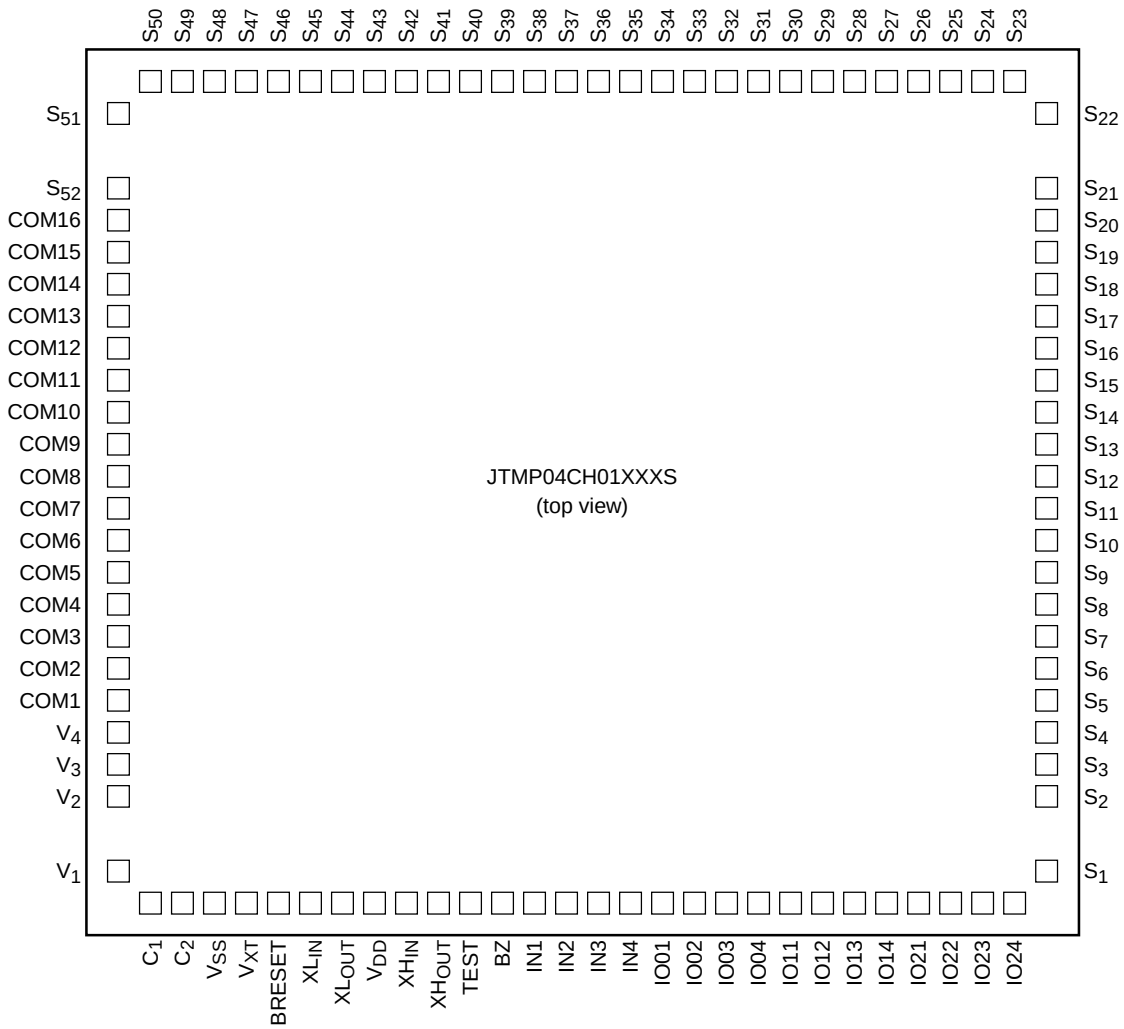
QFP100-P-1420-0.65A Unit: mm



Weight: 1.65 g (typ.)

Bare chip

1. Pad assignment



Chip size	5.04 × 5.78 (mm)
Chip thickness	450 ± 30 (μm)
Substrate voltage	V_{SS}

2. Pad location table

($\times 10^{-3}$mm)

No.	PAD Name	X Point	Y Point
1	V_1	–1957	2653
2	C_1	–2253	2375
3	C_2	–2253	2201
4	V_{SS}	–2253	2038
5	V_{XT}	–2253	1871
6	BRESET	–2253	1699
7	XL_{IN}	–2253	1519
8	XL_{OUT}	–2253	1345
9	V_{DD}	–2253	1144
10	XH_{IN}	–2253	944
11	XH_{OUT}	–2253	772
12	TEST	–2253	592
13	BZ	–2253	410
14	IN1	–2253	227
15	IN2	–2253	59
16	IN3	–2253	–112
17	IN4	–2253	–280
18	IO01	–2253	–468
19	IO02	–2253	–639
20	IO03	–2253	–815
21	IO04	–2253	–986
22	IO11	–2253	–1162
23	IO12	–2253	–1333
24	IO13	–2253	–1509
25	IO14	–2253	–1680
26	IO21	–2253	–1856
27	IO22	–2253	–2027
28	IO23	–2253	–2203
29	IO24	–2253	–2374
30	S_1	–1960	–2653
31	S_2	–1628	–2653
32	S_3	–1460	–2653
33	S_4	–1285	–2653
34	S_5	–1117	–2653
35	S_6	–942	–2653
36	S_7	–774	–2653

No.	PAD Name	X Point	Y Point
37	S_8	–599	–2653
38	S_9	–431	–2653
39	S_{10}	–256	–2653
40	S_{11}	–85	–2653
41	S_{12}	85	–2653
42	S_{13}	258	–2653
43	S_{14}	428	–2653
44	S_{15}	601	–2653
45	S_{16}	771	–2653
46	S_{17}	944	–2653
47	S_{18}	1114	–2653
48	S_{19}	1287	–2653
49	S_{20}	1457	–2653
50	S_{21}	1630	–2653
51	S_{22}	1959	–2653
52	S_{23}	2253	–2283
53	S_{24}	2253	–2112
54	S_{25}	2253	–1945
55	S_{26}	2253	–1774
56	S_{27}	2253	–1607
57	S_{28}	2253	–1436
58	S_{29}	2253	–1269
59	S_{30}	2253	–1098
60	S_{31}	2253	–931
61	S_{32}	2253	–760
62	S_{33}	2253	–593
63	S_{34}	2253	–422
64	S_{35}	2253	–255
65	S_{36}	2253	–84
66	S_{37}	2253	84
67	S_{38}	2253	255
68	S_{39}	2253	422
69	S_{40}	2253	593
70	S_{41}	2253	760
71	S_{42}	2253	931
72	S_{43}	2253	1098

No.	PAD Name	X Point	Y Point
73	S_{44}	2253	1269
74	S_{45}	2253	1436
75	S_{46}	2253	1607
76	S_{47}	2253	1774
77	S_{48}	2253	1945
78	S_{49}	2253	2112
79	S_{50}	2253	2283
80	S_{51}	1959	2653
81	S_{52}	1629	2653
82	COM16	1459	2653
83	COM15	1286	2653
84	COM14	1116	2653
85	COM13	943	2653
86	COM12	773	2653
87	COM11	600	2653
88	COM10	430	2653
89	COM9	257	2653
90	COM8	87	2653
91	COM7	–87	2653
92	COM6	–257	2653
93	COM5	–430	2653
94	COM4	–600	2653
95	COM3	–773	2653
96	COM2	–943	2653
97	COM1	–1116	2653
98	V_4	–1291	2653
99	V_3	–1468	2653
100	V_2	–1638	2653

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