DSC557-03

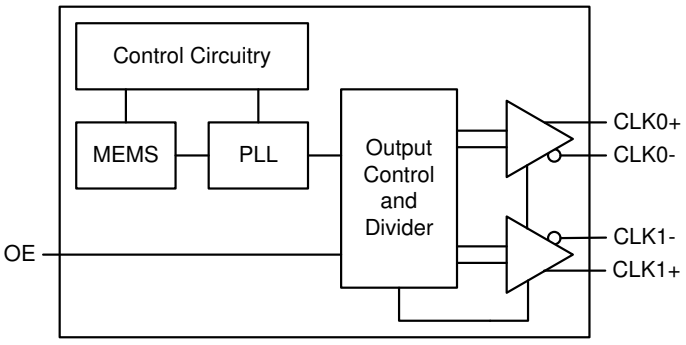
Crystal-less Two Output PCIe Gen1/2/3 Clock Generator

General Description

The DSC557-03 is a crystal-less, two output PCI express clock generator meeting Gen1, Gen2, and Gen3 specifications. The clock generator uses proven silicon MEMS technology to provide 100MHz* differential output clocks with excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the external quartz crystal, the DSSC557-03 significantly enhances reliability and accelerates product development, while meeting stringent clock performance criteria for a variety of communications, storage, and networking applications.

DSC557-03 has an Output Enable / Disable feature allowing it to disable the outputs when OE is low. The device is available in two different packages; a "drop-in" replacement 16 pin TSSOP or a space saving 14 pin QFN (77% less board space). Additional output formats are also available in any combination of LVPECL, LVDS, and HCSL.

Block Diagram



* Clk0+/- and Clk1+/- are 100 MHz as per PCIe standards. For other frequencies, please contact the factory.

Features

- **Meets PCIe Gen1, Gen2 & Gen3 specs.**
- **Available Output Formats:**
  - HCSL, LVPECL, or LVDS
  - HCSL/LVPECL, HCSL/LVDS, LVPECL/LVDS
- **Wide Temperature Range**
  - Ext. Industrial: -40° to 105° C
  - Industrial: -40° to 85° C
  - Ext. commercial: -20° to 70° C
- **Supply Range of 2.25 to 3.6 V**
- **Low Power Consumption**
  - 30% lower than competing devices
- **Excellent Shock & Vibration Immunity**
  - Qualified to MIL-STD-883
- **Available Footprints:**
  - 16 TSSOP
  - 14 QFN
- **Lead Free & RoHS Compliant**
- **Short Lead Time: 2 Weeks**

Applications

- **Communications/Networking**
  - **Ethernet**
  - **1G, 10GBASE-T/KR/LR/SR, and FcoE**
  - **Routers and Switches**
  - **Gateways, VoIP, Wireless AP's**
  - **Passive Optical Networks**
- **Storage**
  - **SAN, NAS, SSD, JBOD**
- **Embedded Applications**
  - **Industrial, Medical, and Avionics**
  - **Security Systems and Office Automation**
  - **Digital Sinage, POS and others**
- **Consumer Electronics**
  - **Smart TV, Bluray, STB**

Specifications (Unless specified otherwise: T=25° C, VDD =3.3V)

Parameter		Condition	Min.	Typ.	Max.	Unit
Supply Voltage[1]	V_{DD}		2.25		3.6	V
Supply Current	I_{DD}	EN pin low – outputs are disabled		21	23	mA
Supply Current[2] (Two HCSL Outputs)	I_{DD}	EN pin high – outputs are enabled R_L=50 Ω, F_{O1}=F_{O2}=100 MHz		60		mA
Frequency Stability	Δf	Includes frequency variations due to initial tolerance, temp. and power supply voltage			±100 ±50	ppm
Startup Time[3]	t_{SU}				5	ms
Input Logic Levels Input logic high Input logic low	 V_{IH} V_{IL}		 0.75xV_{DD} -		 - 0.25xV_{DD}	V
Output Disable Time[4]	t_{DA}				5	ns
Output Enable Time	t_{EN}				20	ns
Pull-Up Resistor[2]		Pull-up on OE pin		40		kΩ

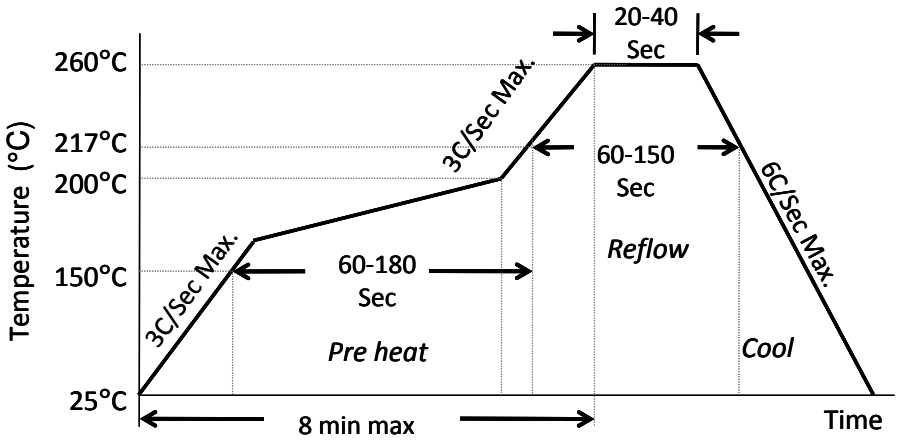
HCSL Outputs[6]						
Parameter		**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Output Logic Levels Output logic high Output logic low	 V_{OH} V_{OL}	R_L=50Ω	 0.725 -		 - 0.1	V
Pk to Pk Output Swing		Single-Ended		750		mV
Output Transition time[4] Rise Time Fall Time	 t_R t_F	20% to 80% R_L=50Ω, C_L= 2pF	200		400	ps
Frequency	f_0	Single Frequency	2.3	100[7]	460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter[5]	J_{PER}	F_{O1}=F_{O2}=100 MHz		2.5		ps_{RMS}
Jitter, Phase (Common Clock Architecture)	R_J	PCIe Gen 1.1 T_J=D_J + 14.069 x R_J (BER 10-12)		0.540		Ps_{RMS}
	D_J T_J	PCIe Gen 1.1 T_J=D_J + 14.069 x R_J (BER 10-12)		0.832 8.536	41.9[8] 86.0[8]	ps_{p-p}
	$J_{RMS-CCHF}$	PCIe Gen 2.1, 1.5 MHz to Nyquist		0.458	3.1[8]	ps_{RMS}
	$J_{RMS-CCLF}$	PCIe Gen 2.1, 10 kHz to 1.5 MHz		0.030	3.0[8]	ps_{RMS}
	J_{RMS-CC}	PCIe Gen 3.0		0.165	1.0[8]	ps_{RMS}
Integrated Phase Noise (Data Clock Architecture)	$J_{RMS-DCHF}$	PCIe Gen 2.1, 1.5 MHz to Nyquist		0.561	4.0[8]	ps_{RMS}
	$J_{RMS-DCLF}$	PCIe Gen 2.1, 10 kHz to 1.5 MHz		1.778	7.5[8]	ps_{RMS}
	J_{RMS-DC}	PCIe Gen 3.0		0.147	1.0[8]	ps_{RMS}

Notes:
1. V_{DD} should be filtered with 0.01uf capacitor.
2. Output is enabled if OE pin is floated or not connected.
3. t_{su} is time to 100PPM stable output frequency after V_{DD} is applied and outputs are enabled.
4. Output Waveform and Connection Diagram define the parameters.
5. Period Jitter includes crosstalk from adjacent output.
6. Contact Sales@Discera.com for alternate output options (LVPECL, LVDS, LVCMOS).
7. Contact Sales@Discera.com for alternative frequency options
8. Jitter limits established by Gen 1.1, Gen 2.1, and Gen 3.0 PCIe standards.

Absolute Maximum Ratings

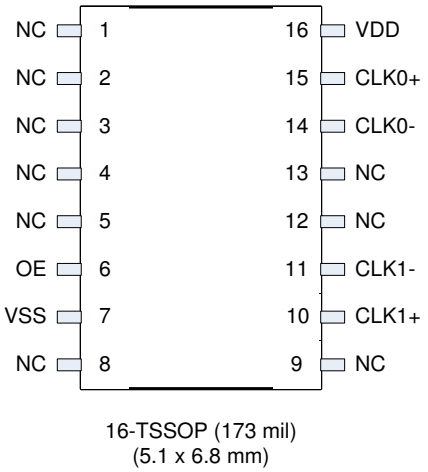
Item	Min	Max	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	V_{DD}+0.3	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD HBM MM CDM	-	 4000 400 1500	V	

Solder Reflow Profile



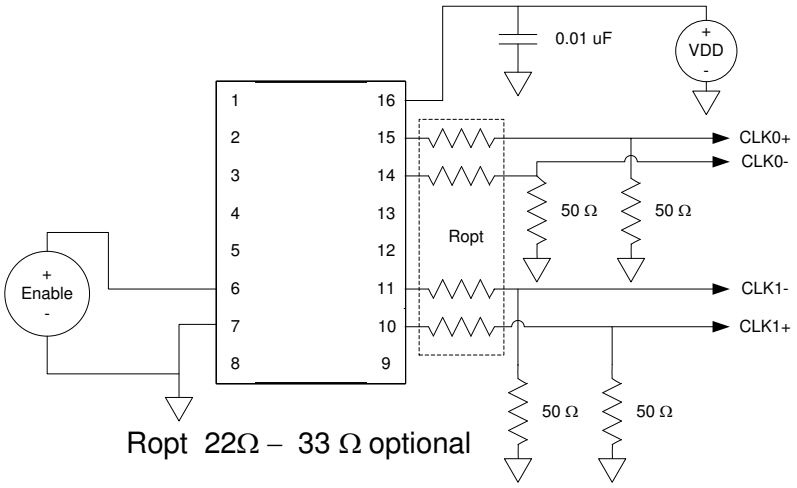
14 QFN MSL 1 @ 260°C refer to JSTD-020C 16 TSSOP MSL 3 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

Pin Diagram (16 TSSOP)



16-TSSOP (173 mil)
(5.1 x 6.8 mm)

Connection Diagram (16 TSSOP Two HCSL Outputs)

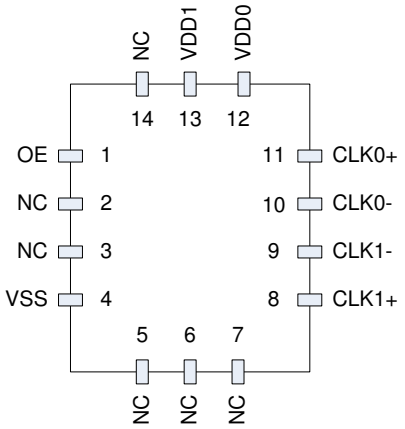


Ropt 22Ω – 33 Ω optional

Pin Description (16 TSSOP)

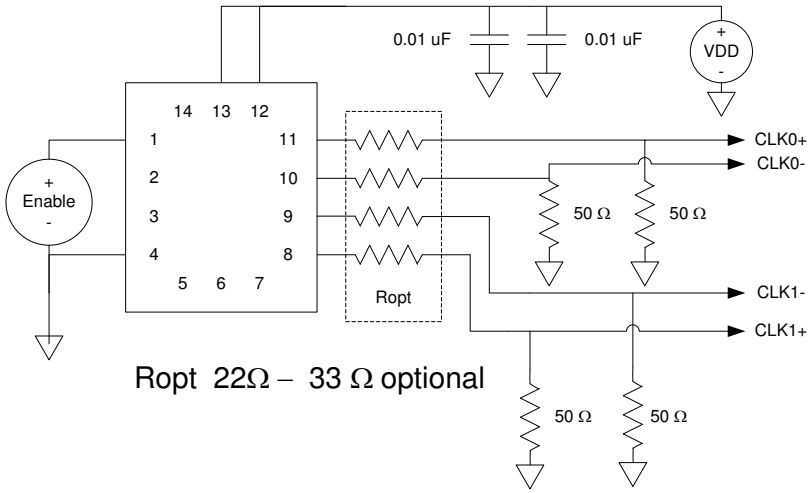
Pin No.	Pin Name[9]	Pin Type	Description
1	NC	NA	No connect
2	NC	NA	No connect
3	NC	NA	No connect
4	NC	NA	No connect
5	NC	NA	No connect
6	OE	I	Output Enable; active high
7	VSS	Power	Ground
8	NC	NA	No connect
9	NC	NA	No connect
10	CLK1+	O	True output of differential pair
11	CLK1-	O	Complement output of differential pair
12	NC	NA	No connect
13	NC	NA	No connect
14	CLK0-	O	Complement output of differential pair
15	CLK0+	O	True output of differential pair
16	VDD	Power	Power Supply

Pin Diagram (14 QFN)



14 QFN 3.2x2.5mm

Connection Diagram (14 QFN Two HCSL Outputs)

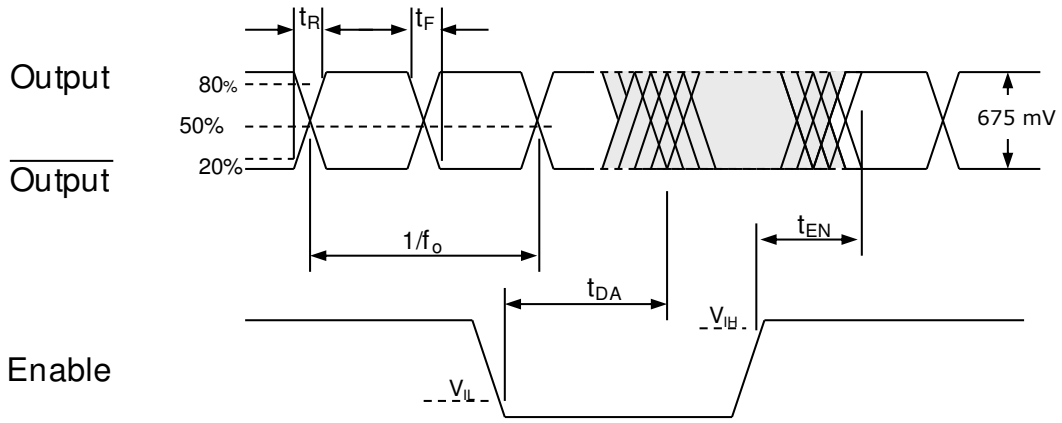


Ropt 22Ω – 33 Ω optional

Pin Description (14 QFN)

Pin No.	Pin Name	Pin Type	Description
1	OE	I	Output Enable; active high
2	NC	NA	Ground recommended or leave as a NC
3	NC	NA	Ground recommended or leave as a NC
4	VSS	Power	Ground
5	NC	NA	Ground recommended or leave as a NC
6	NC	NA	Ground recommended or leave as a NC
7	NC	NA	Ground recommended or leave as a NC
8	CLK1+	O	True output of differential pair
9	CLK1-	O	Complement output of differential pair
10	CLK0-	O	Complement output of differential pair
11	CLK0+	O	True output of differential pair
12	VDD1	Power	Power Supply for Core and Output 1 (CLK0+/-)
13	VDD0	Power	Power Supply for Output 0 (CLK1+/-)
14	NC	NA	Ground recommended or leave as a NC

OE Function and Output Waveform: HCSL



Ordering Information[9]

DSC557-03 4 4 F I 0 - T

CLK 1 Output Format
1: LVCMOS
2: LVPECL
3: LVDS
4: HCSL

CLK 0 Output Format
1: LVCMOS
2: LVPECL
3: LVDS
4: HCSL

Packing
T: Tape & Reel

Stability
0: ±100ppm
1: ±50ppm

Temp Range
E: -20 to 70
I: -40 to 85
L: -40 to 105

Package
F: 14 QFN
S: 16 TSSOP

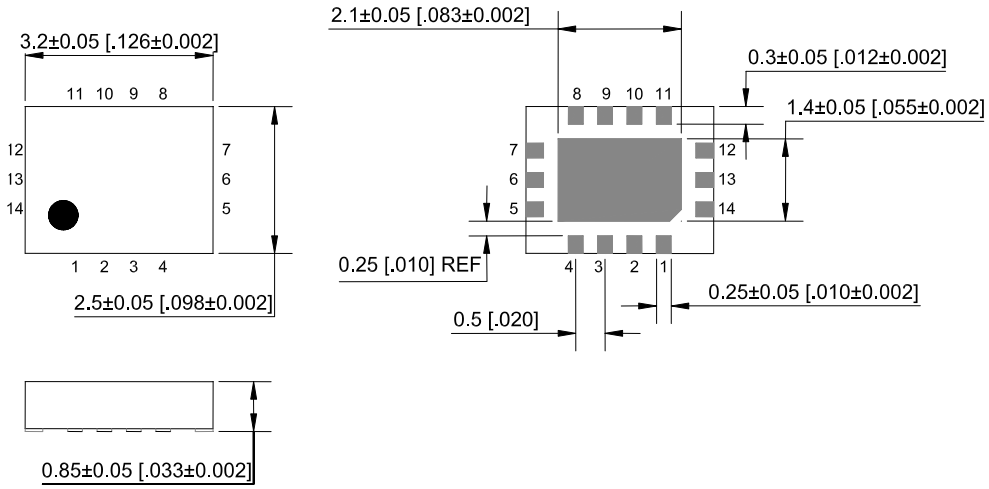
Note 9. CLK0 and CLK1 are configured at the factory to 100 MHz. (For other frequencies, contact the factory at sales@discera.com.)

Package Dimensions

F: 14 QFN, 3.2 x 2.5 mm

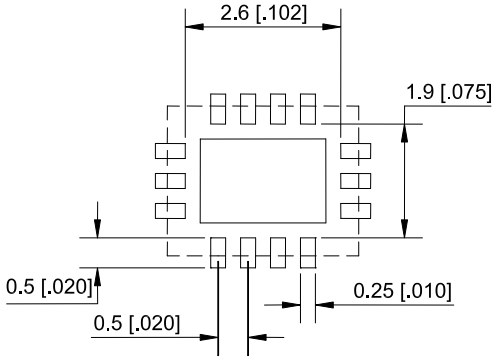
External Dimensions

units: mm[inch]

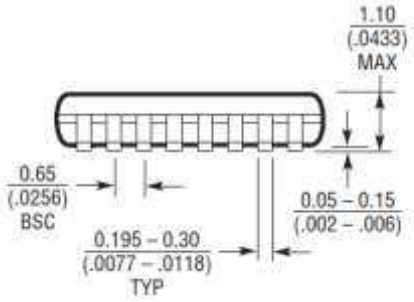


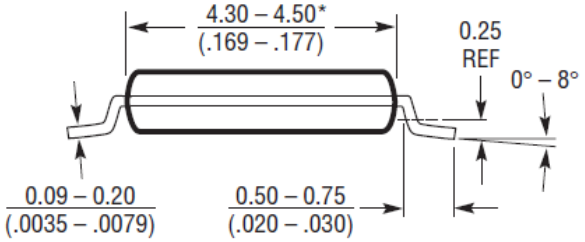
Recommended
Solder Pad Layout

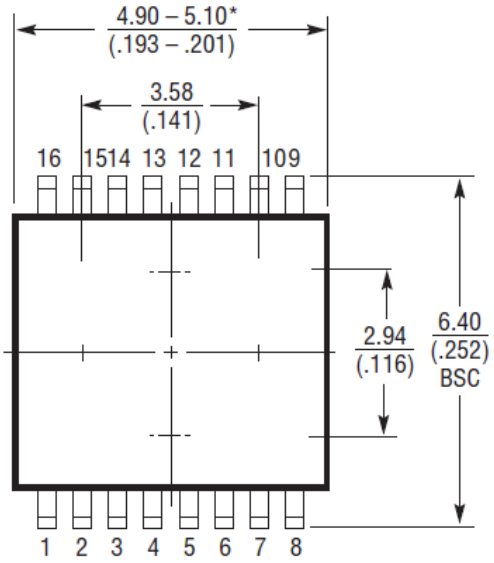
units: mm[inch]



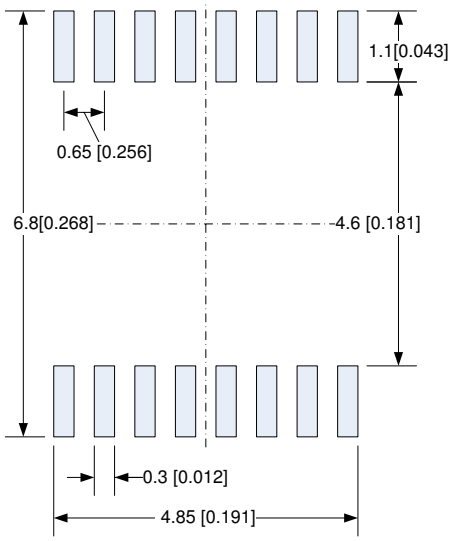
S: 16 TSSOP (173 mil body width)







Recommended Solder
Pad Layout
Units mm [in]



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE

4. RECOMMENDED MINIMUM PCB METAL SIZE
FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH
SHALL NOT EXCEED 0.150mm (.006") PER SIDE

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