S6C1108

6 BIT 384 CHANNEL RSDS TFT-LCD SOURCE DRIVER

Nov. 2002.

Ver. 0.2

INTRODUCTION

The S6C1108 is a Source Driver suitable for Reduced Swing Differential Signaling(RSDS) digital interface.
It converts 18-bit digital data into the analog voltage for 384 channels, charging each sub-pixel to the correct gray level corresponding to the digital value.

The RSDS path to the panel timing controller contributes toward lowering radiated EMI, reducing system power consumption and eliminates one of the two pixel busses used in typical XGA, SXGA TFT LCD panels.
This single 9-bit differential bus conveys the 18-bit color data for XGA, SXGA panels.

FEATURES

- TFT active matrix LCD source driver LSI
- 64G/S is possible through 14(7 by 2) external power supply and D/A converter
- Both dot inversion display and N-line inversion display are possible
- Compatible with gamma-correction
- Charge sharing function
- Logic supply voltage[VDD1] : 2.7 to 3.6 V
- LCD driver supply voltage[VDD2] : 7.0 to 12.0 V
- Output dynamic range: VSS2+0.2V to VDD2-0.2V
- Maximum operating frequency: fmax=85 MHz (internal data transmission rate at 2.7 V operation)
- Output: 384 outputs
- Reduced Swing Differential Signaling(RSDS) interface for low power consumption and low EMI.
- Minimum RSDS input swing level(CLKP, CLKN, DATAP, DATAN): 100mV
- Data bus interface control pin (DATPOL)
- TCP or COF supported

BLOCK DIAGRAM

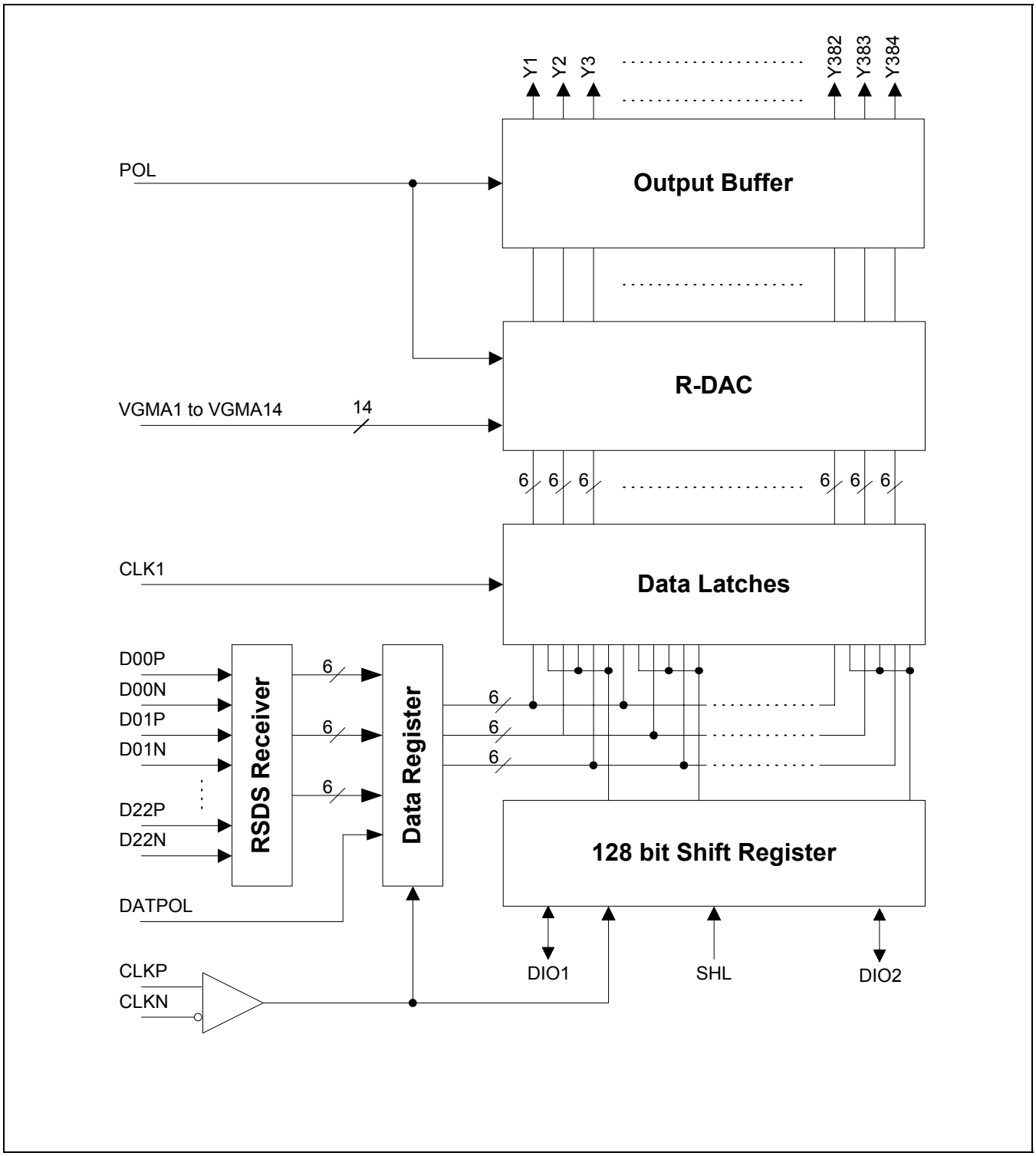


Figure 1. S6C1108 Block Diagram

PIN ASSIGNMENTS

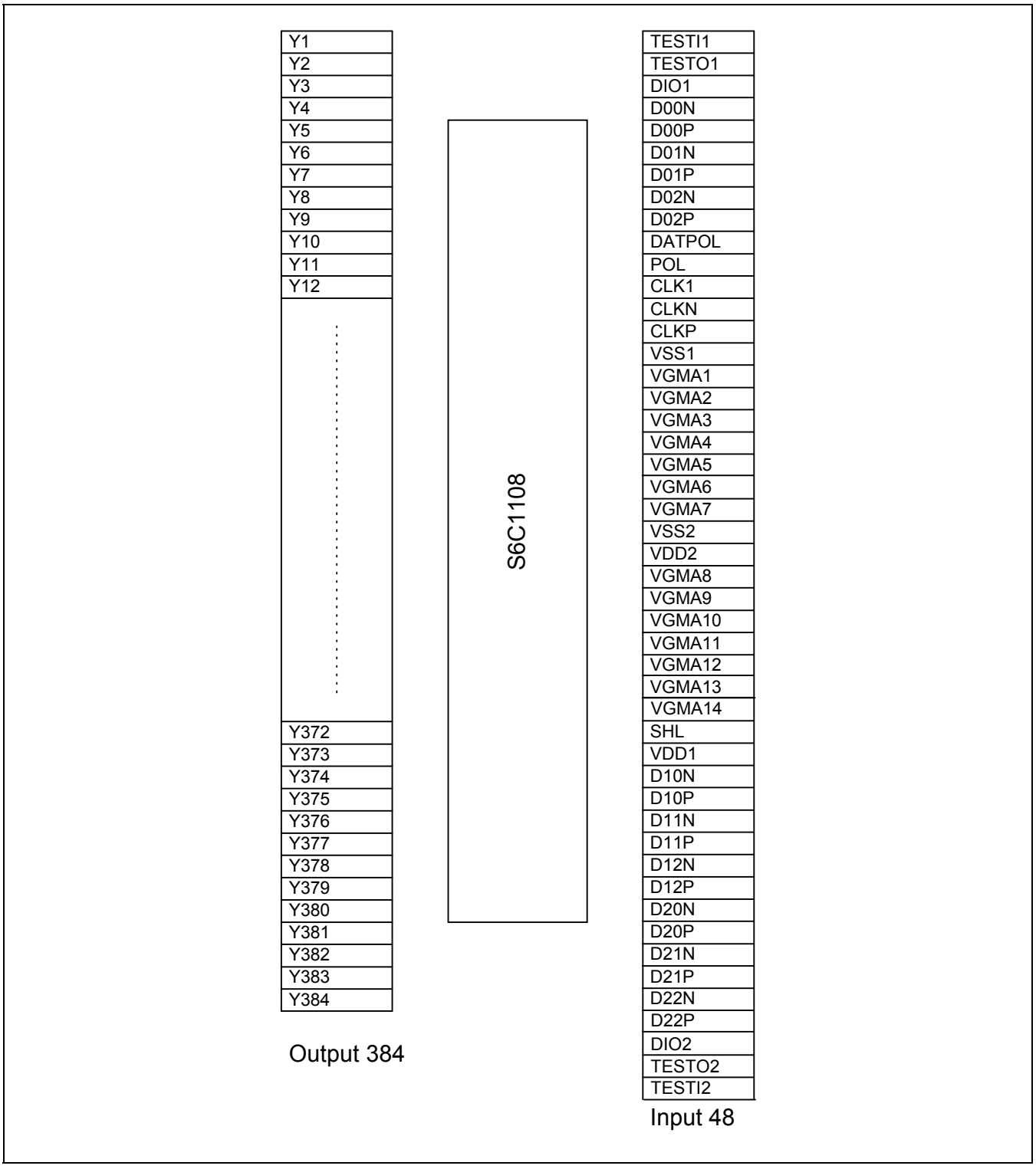


Figure 2. S6C1108 Pin Assignments

PIN DESCRIPTIONS

Symbol	Pin Name	Description
VDD1	Logic power supply	2.7 to 3.6 V
VDD2	Driver power supply	7.0 to 12.0 V
VSS1	Logic ground	Ground (0 V)
VSS2	Driver ground	Ground (0 V)
Y1 to Y384	Driver outputs	The D/A converted 64 gray-scale analog voltage is output.
D0P<0:2> D0N<0:2> D1P<0:2> D1N<0:2> D2P<0:2> D2N<0:2>	RSDS data input	Total data lines consist of 18 data bus. (6-bit digital, 3 colors(R, G, B) and 2 differential input pairs) The 3-bit differential input pairs generate the internal 6-bit data through the comparison between DxxP and DxxN.
SHL	Shift direction control input	This pin controls the direction of shift register in cascade connection. When SHL=H: DIO1 input, Y1→Y384, DIO2 output When SHL=L: DIO2 input, Y384→Y1, DIO1 output
DIO1	Start pulse input/output	SHL=H: Used as the start pulse input pin. SHL=L: Used as the start pulse output pin.
DIO2	Start pulse input/output	SHL=H: Used as the start pulse output pin. SHL=L: Used as the start pulse input pin.
DATPOL	Data inversion input	DATPOL= L: No inversion DATPOL= H: Data polarity inversion (DATPOL must be fixed VSS1 or VDD1.)
POL	Polarity input	POL=H: The reference voltage for odd number outputs are VGMA1 to VGMA7 and those for even number outputs are VGMA8 to VGMA14. POL=L: The reference voltage for odd number outputs are VGMA8 to VGMA14 and those for even number outputs are VGMA1 to VGMA7.
CLKP CLKN	RSDS shift clock input	The RSDS clock input pairs generate the internal shift clock, CLK2, through the comparison between CLKP and CLKN.
CLK1	Latch input	S6C1108 clears 128 shift registers at the rising edge of CLK1 and outputs the analog data to the each channel at the falling edge.
VGMA1 to VGMA14	Gamma corrected power supplies	Input the gamma corrected power supplies from external source. VDD2>VGMA1>VGMA2>……>VGMA13>VGMA14>VSS2 Keep power supplies unchanged during the gray-scale voltage output.
TESTI1/O1, TESTI2/O2	Amp test input/output	These pins are used for Amp test. TESTI1(=TESTI2)=L : Normal operation mode

OPERATION DESCRIPTION

RSDS RECEIVER AND DEMUX

The S6C1108 adapts the RSDS interface for EMI solution. The internal RSDS receiver block operates the comparison between the transmitted differential input pair data. The input data lines from the timing controller to the RSDS receiver consist of 6-bit digital, 3 colors, 1 port, 2 differential pairs(DxxP/DxxN).
The input common mode voltage range at the RSDS receiver is 1.2V. The differential data and clock signals from the panel timing controller arrive at the S6C1108 as multiplexed, even and odd data fields. (i.e., the data is 2:1 multiplexed). The nominal peak to peak swing of this data is 200mV across a termination resistor.

RSDS DATA BUS INTERFACE CONTROL

DATPOL controls the internal data inversion. When DATPOL=”H”, the internal data is inverted. The inverted data is the same that the RSDS receiver operates the comparison between the cross-transmitted differential input pair data. Using the data inversion input pin, DATPOL, the RSDS data bus interface can be changed.

DISPLAY DATA TRANSFER

When DIO1 (or DIO2) pulse is loaded into the internal latch on the falling edge of CLKP, DIO1 (or DIO2) pulse enables the operation of data transfer, so display data is valid on the 2nd falling edge of CLKP. Once all the data of 384 channels is loaded into internal latch, it goes into stand-by state automatically, and any new data is not accepted even though CLKP is provided until next DIO1 (or DIO2) input. When next DIO1 (or DIO2) is provided, new display data is valid on the 2nd falling edge of CLKP after the rising edge of DIO1 (or DIO2).

EXTENSION OF OUTPUT

Output pin can be adjusted to an extended screen by cascade connection.
When SHL="L", Connect DIO1 pin of the previous stage to the DIO2 pin of the next stage and all the input pins except DIO1 and DIO2 are connected together in each device.
When SHL="H", Connect DIO2 pin of the previous stage to the DIO1 pin of the next stage and all the input pins except DIO2 and DIO1 are connected together in each device.

RELATIONSHIP BETWEEN INPUT DATA VALUE AND OUTPUT VOLTAGE

The LCD drive output voltages are determined by the input data and 14 (7 by 2) gamma corrected power supplies (VGMA1 to VGMA14). Besides, to be able to deal with dot line inversion when mounted on a single-side, gradation voltages with different polarity can be output to the odd number output pins and the even number output pins. Among 7-by-2 gamma corrected voltages, input gray-scale voltages of the same polarity with respect to the common voltage, for the respective 7 gamma corrected voltages of VGMA1 to VGMA7 and VGMA8 to VGMA14.

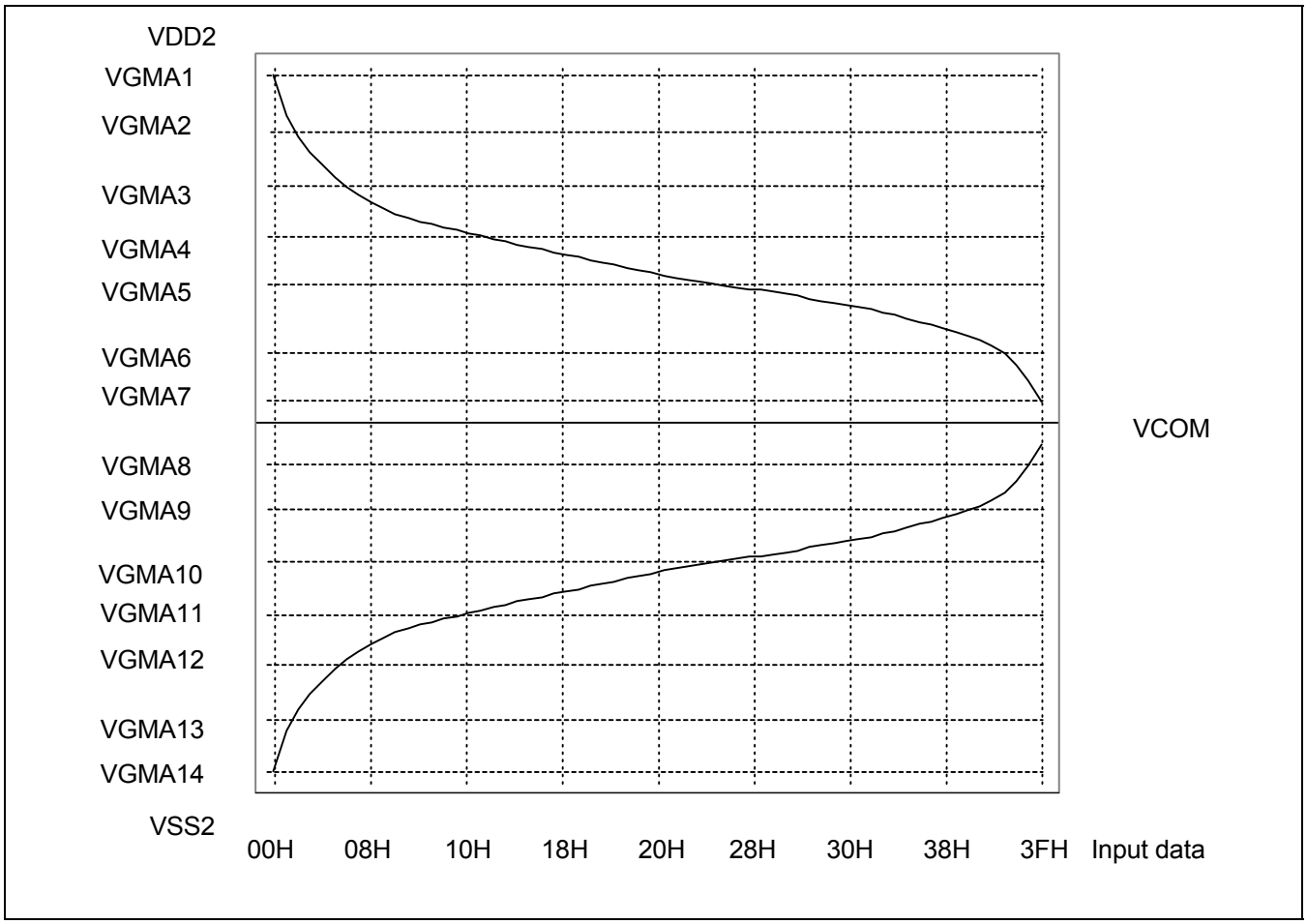
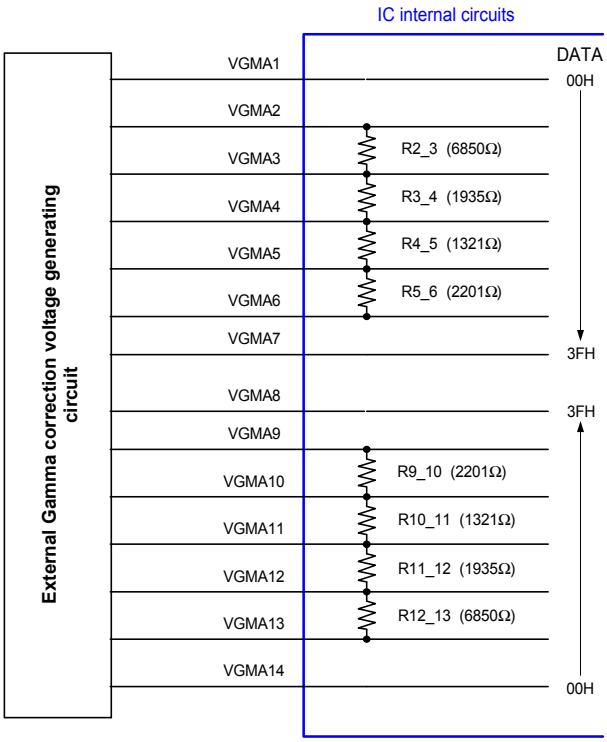


Figure 3. Gamma Correction Curve

Table 1. Resistor Strings (R0 to R62, unit: Ω)

Name	Value	Name	Value	Name	Value	Name	Value
R0	2008	R16	169	R32	88	R48	85
R1	1307	R17	156	R33	86	R49	88
R2	958	R18	149	R34	84	R50	92
R3	731	R19	140	R35	83	R51	97
R4	606	R20	133	R36	81	R52	103
R5	507	R21	126	R37	81	R53	110
R6	431	R22	122	R38	81	R54	118
R7	373	R23	119	R39	81	R55	126
R8	328	R24	115	R40	81	R56	136
R9	292	R25	112	R41	81	R57	152
R10	263	R26	108	R42	81	R58	187
R11	243	R27	104	R43	81	R59	234
R12	226	R28	101	R44	81	R60	289
R13	209	R29	97	R45	83	R61	384
R14	195	R30	94	R46	84	R62	508
R15	181	R31	90	R47	84		

Total R : 14823Ω



The S6C1108 has on-chip dividing resistors.

The gamma correction voltage input pins are divided into two parts. Each part is connected in series with resistors. Each of these resistor series has a total typical value of 14823Ω.

Note that since these voltages are resistor divided internally, the voltages applied to the VGMAn pins should be applied through a low-impedance circuit.

If the voltages are directly applied by the resistor divider, the desired output voltages may not result (Recommend you to use operational amplifier).

SAMSUNG ELECTRONICS

Table 2. Relationship between Input Data and Output Voltage Value

Input Data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output Voltage
00H	0	0	0	0	0	0	VH0	VGMA1
01H	0	0	0	0	0	1	VH1	VGMA2
02H	0	0	0	0	1	0	VH2	VGMA2+(VGMA3-VGMA2) × 1307/6850
03H	0	0	0	0	1	1	VH3	VGMA2+(VGMA3-VGMA2) × 2265/6850
04H	0	0	0	1	0	0	VH4	VGMA2+(VGMA3-VGMA2) × 2996/6850
05H	0	0	0	1	0	1	VH5	VGMA2+(VGMA3-VGMA2) × 3602/6850
06H	0	0	0	1	1	0	VH6	VGMA2+(VGMA3-VGMA2) × 4109/6850
07H	0	0	0	1	1	1	VH7	VGMA2+(VGMA3-VGMA2) × 4540/6850
08H	0	0	1	0	0	0	VH8	VGMA2+(VGMA3-VGMA2) × 4913/6850
09H	0	0	1	0	0	1	VH9	VGMA2+(VGMA3-VGMA2) × 5241/6850
0AH	0	0	1	0	1	0	VH10	VGMA2+(VGMA3-VGMA2) × 5533/6850
0BH	0	0	1	0	1	1	VH11	VGMA2+(VGMA3-VGMA2) × 5796/6850
0CH	0	0	1	1	0	0	VH12	VGMA2+(VGMA3-VGMA2) × 6039/6850
0DH	0	0	1	1	0	1	VH13	VGMA2+(VGMA3-VGMA2) × 6265/6850
0EH	0	0	1	1	1	0	VH14	VGMA2+(VGMA3-VGMA2) × 6474/6850
0FH	0	0	1	1	1	1	VH15	VGMA2+(VGMA3-VGMA2) × 6669/6850
10H	0	1	0	0	0	0	VH16	VGMA3
11H	0	1	0	0	0	1	VH17	VGMA3+(VGMA4-VGMA3) × 169/1935
12H	0	1	0	0	1	0	VH18	VGMA3+(VGMA4-VGMA3) × 325/1935
13H	0	1	0	0	1	1	VH19	VGMA3+(VGMA4-VGMA3) × 474/1935
14H	0	1	0	1	0	0	VH20	VGMA3+(VGMA4-VGMA3) × 614/1935
15H	0	1	0	1	0	1	VH21	VGMA3+(VGMA4-VGMA3) × 747/1935
16H	0	1	0	1	1	0	VH22	VGMA3+(VGMA4-VGMA3) × 873/1935
17H	0	1	0	1	1	1	VH23	VGMA3+(VGMA4-VGMA3) × 995/1935
18H	0	1	1	0	0	0	VH24	VGMA3+(VGMA4-VGMA3) × 1114/1935
19H	0	1	1	0	0	1	VH25	VGMA3+(VGMA4-VGMA3) × 1229/1935
1AH	0	1	1	0	1	0	VH26	VGMA3+(VGMA4-VGMA3) × 1341/1935
1BH	0	1	1	0	1	1	VH27	VGMA3+(VGMA4-VGMA3) × 1449/1935
1CH	0	1	1	1	0	0	VH28	VGMA3+(VGMA4-VGMA3) × 1553/1935
1DH	0	1	1	1	0	1	VH29	VGMA3+(VGMA4-VGMA3) × 1654/1935
1EH	0	1	1	1	1	0	VH30	VGMA3+(VGMA4-VGMA3) × 1751/1935
1FH	0	1	1	1	1	1	VH31	VGMA3+(VGMA4-VGMA3) × 1845/1935

NOTE: VDD2>VGMA1>VGMA2>VGMA3>VGMA4>VGMA5>VGMA6>VGMA7

Table 2. Relationship between Input Data and Output Voltage Value (Continued)

Input Data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output Voltage
20H	1	0	0	0	0	0	VH32	VGMA4
21H	1	0	0	0	0	1	VH33	VGMA4+(VGMA5-VGMA4) × 88/1321
22H	1	0	0	0	1	0	VH34	VGMA4+(VGMA5-VGMA4) × 174/1321
23H	1	0	0	0	1	1	VH35	VGMA4+(VGMA5-VGMA4) × 258/1321
24H	1	0	0	1	0	0	VH36	VGMA4+(VGMA5-VGMA4) × 341/1321
25H	1	0	0	1	0	1	VH37	VGMA4+(VGMA5-VGMA4) × 422/1321
26H	1	0	0	1	1	0	VH38	VGMA4+(VGMA5-VGMA4) × 503/1321
27H	1	0	0	1	1	1	VH39	VGMA4+(VGMA5-VGMA4) × 584/1321
28H	1	0	1	0	0	0	VH40	VGMA4+(VGMA5-VGMA4) × 665/1321
29H	1	0	1	0	0	1	VH41	VGMA4+(VGMA5-VGMA4) × 746/1321
2AH	1	0	1	0	1	0	VH42	VGMA4+(VGMA5-VGMA4) × 827/1321
2BH	1	0	1	0	1	1	VH43	VGMA4+(VGMA5-VGMA4) × 908/1321
2CH	1	0	1	1	0	0	VH44	VGMA4+(VGMA5-VGMA4) × 989/1321
2DH	1	0	1	1	0	1	VH45	VGMA4+(VGMA5-VGMA4) × 1070/1321
2EH	1	0	1	1	1	0	VH46	VGMA4+(VGMA5-VGMA4) × 1153/1321
2FH	1	0	1	1	1	1	VH47	VGMA4+(VGMA5-VGMA4) × 1237/1321
30H	1	1	0	0	0	0	VH48	VGMA5
31H	1	1	0	0	0	1	VH49	VGMA5+(VGMA6-VGMA5) × 85/2201
32H	1	1	0	0	1	0	VH50	VGMA5+(VGMA6-VGMA5) × 173/2201
33H	1	1	0	0	1	1	VH51	VGMA5+(VGMA6-VGMA5) × 265/2201
34H	1	1	0	1	0	0	VH52	VGMA5+(VGMA6-VGMA5) × 362/2201
35H	1	1	0	1	0	1	VH53	VGMA5+(VGMA6-VGMA5) × 465/2201
36H	1	1	0	1	1	0	VH54	VGMA5+(VGMA6-VGMA5) × 575/2201
37H	1	1	0	1	1	1	VH55	VGMA5+(VGMA6-VGMA5) × 693/2201
38H	1	1	1	0	0	0	VH56	VGMA5+(VGMA6-VGMA5) × 819/2201
39H	1	1	1	0	0	1	VH57	VGMA5+(VGMA6-VGMA5) × 955/2201
3AH	1	1	1	0	1	0	VH58	VGMA5+(VGMA6-VGMA5) × 1107/2201
3BH	1	1	1	0	1	1	VH59	VGMA5+(VGMA6-VGMA5) × 1294/2201
3CH	1	1	1	1	0	0	VH60	VGMA5+(VGMA6-VGMA5) × 1528/2201
3DH	1	1	1	1	0	1	VH61	VGMA5+(VGMA6-VGMA5) × 1817/2201
3EH	1	1	1	1	1	0	VH62	VGMA6
3FH	1	1	1	1	1	1	VH63	VGMA7

Table 2. Relationship between Input Data and Output Voltage Value (Continued)

Input Data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output Voltage
00H	0	0	0	0	0	0	VL0	VGMA14
01H	0	0	0	0	0	1	VL1	VGMA13
02H	0	0	0	0	1	0	VL2	VGMA13+(VGMA12-VGMA13) × 1307/6850
03H	0	0	0	0	1	1	VL3	VGMA13+(VGMA12-VGMA13) × 2265/6850
04H	0	0	0	1	0	0	VL4	VGMA13+(VGMA12-VGMA13) × 2996/6850
05H	0	0	0	1	0	1	VL5	VGMA13+(VGMA12-VGMA13) × 3602/6850
06H	0	0	0	1	1	0	VL6	VGMA13+(VGMA12-VGMA13) × 4109/6850
07H	0	0	0	1	1	1	VL7	VGMA13+(VGMA12-VGMA13) × 4540/6850
08H	0	0	1	0	0	0	VL8	VGMA13+(VGMA12-VGMA13) × 4913/6850
09H	0	0	1	0	0	1	VL9	VGMA13+(VGMA12-VGMA13) × 5241/6850
0AH	0	0	1	0	1	0	VL10	VGMA13+(VGMA12-VGMA13) × 5533/6850
0BH	0	0	1	0	1	1	VL11	VGMA13+(VGMA12-VGMA13) × 5796/6850
0CH	0	0	1	1	0	0	VL12	VGMA13+(VGMA12-VGMA13) × 6039/6850
0DH	0	0	1	1	0	1	VL13	VGMA13+(VGMA12-VGMA13) × 6265/6850
0EH	0	0	1	1	1	0	VL14	VGMA13+(VGMA12-VGMA13) × 6474/6850
0FH	0	0	1	1	1	1	VL15	VGMA13+(VGMA12-VGMA13) × 6669/6850
10H	0	1	0	0	0	0	VL16	VGMA12
11H	0	1	0	0	0	1	VL17	VGMA12+(VGMA11-VGMA12) × 169/1935
12H	0	1	0	0	1	0	VL18	VGMA12+(VGMA11-VGMA12) × 325/1935
13H	0	1	0	0	1	1	VL19	VGMA12+(VGMA11-VGMA12) × 474/1935
14H	0	1	0	1	0	0	VL20	VGMA12+(VGMA11-VGMA12) × 614/1935
15H	0	1	0	1	0	1	VL21	VGMA12+(VGMA11-VGMA12) × 747/1935
16H	0	1	0	1	1	0	VL22	VGMA12+(VGMA11-VGMA12) × 873/1935
17H	0	1	0	1	1	1	VL23	VGMA12+(VGMA11-VGMA12) × 995/1935
18H	0	1	1	0	0	0	VL24	VGMA12+(VGMA11-VGMA12) × 1114/1935
19H	0	1	1	0	0	1	VL25	VGMA12+(VGMA11-VGMA12) × 1229/1935
1AH	0	1	1	0	1	0	VL26	VGMA12+(VGMA11-VGMA12) × 1341/1935
1BH	0	1	1	0	1	1	VL27	VGMA12+(VGMA11-VGMA12) × 1449/1935
1CH	0	1	1	1	0	0	VL28	VGMA12+(VGMA11-VGMA12) × 1553/1935
1DH	0	1	1	1	0	1	VL29	VGMA12+(VGMA11-VGMA12) × 1654/1935
1EH	0	1	1	1	1	0	VL30	VGMA12+(VGMA11-VGMA12) × 1751/1935
1FH	0	1	1	1	1	1	VL31	VGMA12+(VGMA11-VGMA12) × 1845/1935

NOTE: VGMA8>VGMA9>VGMA10>VGMA11>VGMA12> VGMA13>VGMA14>VSS2

Table 2. Relationship between Input Data and Output Voltage Value (Continued)

Input Data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output Voltage
20H	1	0	0	0	0	0	VL32	VGMA11
21H	1	0	0	0	0	1	VL33	VGMA11+(VGMA10-VGMA11) × 88/1321
22H	1	0	0	0	1	0	VL34	VGMA11+(VGMA10-VGMA11) × 174/1321
23H	1	0	0	0	1	1	VL35	VGMA11+(VGMA10-VGMA11) × 258/1321
24H	1	0	0	1	0	0	VL36	VGMA11+(VGMA10-VGMA11) × 341/1321
25H	1	0	0	1	0	1	VL37	VGMA11+(VGMA10-VGMA11) × 422/1321
26H	1	0	0	1	1	0	VL38	VGMA11+(VGMA10-VGMA11) × 503/1321
27H	1	0	0	1	1	1	VL39	VGMA11+(VGMA10-VGMA11) × 584/1321
28H	1	0	1	0	0	0	VL40	VGMA11+(VGMA10-VGMA11) × 665/1321
29H	1	0	1	0	0	1	VL41	VGMA11+(VGMA10-VGMA11) × 746/1321
2AH	1	0	1	0	1	0	VL42	VGMA11+(VGMA10-VGMA11) × 827/1321
2BH	1	0	1	0	1	1	VL43	VGMA11+(VGMA10-VGMA11) × 908/1321
2CH	1	0	1	1	0	0	VL44	VGMA11+(VGMA10-VGMA11) × 989/1321
2DH	1	0	1	1	0	1	VL45	VGMA11+(VGMA10-VGMA11) × 1070/1321
2EH	1	0	1	1	1	0	VL46	VGMA11+(VGMA10-VGMA11) × 1153/1321
2FH	1	0	1	1	1	1	VL47	VGMA11+(VGMA10-VGMA11) × 1237/1321
30H	1	1	0	0	0	0	VL48	VGMA10
31H	1	1	0	0	0	1	VL49	VGMA10+(VGMA9-VGMA10) × 85/2201
32H	1	1	0	0	1	0	VL50	VGMA10+(VGMA9-VGMA10) × 173/2201
33H	1	1	0	0	1	1	VL51	VGMA10+(VGMA9-VGMA10) × 265/2201
34H	1	1	0	1	0	0	VL52	VGMA10+(VGMA9-VGMA10) × 362/2201
35H	1	1	0	1	0	1	VL53	VGMA10+(VGMA9-VGMA10) × 465/2201
36H	1	1	0	1	1	0	VL54	VGMA10+(VGMA9-VGMA10) × 575/2201
37H	1	1	0	1	1	1	VL55	VGMA10+(VGMA9-VGMA10) × 693/2201
38H	1	1	1	0	0	0	VL56	VGMA10+(VGMA9-VGMA10) × 819/2201
39H	1	1	1	0	0	1	VL57	VGMA10+(VGMA9-VGMA10) × 955/2201
3AH	1	1	1	0	1	0	VL58	VGMA10+(VGMA9-VGMA10) × 1107/2201
3BH	1	1	1	0	1	1	VL59	VGMA10+(VGMA9-VGMA10) × 1294/2201
3CH	1	1	1	1	0	0	VL60	VGMA10+(VGMA9-VGMA10) × 1528/2201
3DH	1	1	1	1	0	1	VL61	VGMA10+(VGMA9-VGMA10) × 1817/2201
3EH	1	1	1	1	1	0	VL62	VGMA9
3FH	1	1	1	1	1	1	VL63	VGMA8

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings (VSS1 = VSS2 = 0 V)

Parameter	Symbol	Ratings	Unit
Logic supply voltage	VDD1	-0.3 to 4.0	V
Driver supply voltage	VDD2	-0.3 to 13.0	V
Input voltage	VGMA1 to 14	-0.3 to VDD2 + 0.3	V
	TESTI1, TESTI2	-0.3 to VDD2 + 0.3	
	Others	-0.3 to VDD1 + 0.3	
Output voltage	DIO1, DIO2	-0.3 to VDD1 + 0.3	V
	Y1 to Y384	-0.3 to VDD2 + 0.3	
Operating power dissipation	Pd	300	mW
Operation temperature	Top	-20 to 75	°C
Storage temperature	Tstg	-55 to 125	°C

CAUTIONS:

If LSIs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
Turn on power order: VDD1 → control signal input → VDD2 → VGMA1 to VGMA14
Turn off power order: VGMA1 to VGMA14 → VDD2 → control signal input → VDD1

RECOMMENDED OPERATION CONDITIONS

Table 4. Recommended Operation Conditions (Ta = - 20 to 75 °C, VSS1 = VSS2 = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic supply voltage	VDD1	2.7	3.0	3.6	V
Driver supply voltage	VDD2	7.0	10.0	12.0	V
Gamma corrected voltage	VGMA1 to VGMA7	0.5VDD2	-	VDD2 - 0.2	V
	VGMA8 to VGMA14	VSS2+ 0.2	-	0.5VDD2	V
Driver part output voltage	Vyo	VSS2+ 0.2	-	VDD2 - 0.2	V
Maximum clock frequency	fmax	VDD1 = 2.7V		85	MHz
Output load capacitance	CL	-	-	150	pF / PIN

DC CHARACTERISTICS

Table 5 . DC Characteristics
(Ta = -20 to 75 °C, VDD1 = 2.7 to 3.6 V, VDD2 = 7.0 to 12.0 V, VSS1 = VSS2 = 0)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	VIH	SHL, CLK1, POL, DATPOL, DIO1 (DIO2)	0.7VDD1	-	VDD1	V
Low level input voltage	VIL		VSS1	-	0.3VDD1	
Input leakage current	IL1		- 1	-	1	μA
TESTI input leak current	IL2	TESTI1(TESTI2)	- 1	-	1	
High level output voltage	VOH	DIO1(DIO2), IO = - 1.0 mA	VDD1 - 0.5	-	-	V
Low level output voltage	VOL	DIO1(DIO2), IO = + 1.0 mA	-	-	0.5	
Resistance between gamma voltage	R0 to R62	Refer to Table 1. Resistor Strings	Rn × 0.7		Rn × 1.3	Ω
Driver output current	IVOH1	VDD2 = 10.0 V, Vx(1) = 5.0 V, Vyo(2) = 9.0 V	-	- 0.8	- 0.4	mA
	IVOL1	VDD2 = 10.0 V, Vx = 5.0 V, Vyo = 1.0 V	0.4	0.8	-	
Output swing voltage difference deviation	DVrms(3)	VDD2 = 10.0V Vyo = 1.5 V ~ 8.5 V	-	± 3	± 10	mV
		VDD2 = 10.0V Vyo = 0.2 V ~ 1.5 V Vyo = 8.5 V ~ 9.8 V	-	-	± 30	
Output pin voltage difference deviation	Dvo	VDD2 = 10.0V Vyo = 1.5 V ~ 8.5 V	-	± 20	± 30	
		VDD2 = 10.0V Vyo = 0.2 V ~ 1.5 V Vyo = 8.5 V ~ 9.8 V	-	± 30	-	
Output average voltage	AVo	VDD2 = 10.0V Dxx = 20H (32 G/S)	-	-	± 7	mV
Output voltage range	Vyo	Input data: 00H to 3FH	VSS2 + 0.2	-	VDD2 - 0.2	V
Logic part dynamic current	IDD1	VDD1 = 3.0 V (4)	-	-	6	mA
Driver part dynamic current	IDD2	VDD2 = 10.0V Load condition 120pF(5)(6)	-	-	25	
	IDD3	VDD2 = 10.0V No load condition(5)(7)	-	-	15	

NOTES: 1. Vx is the voltage applied to analog output pins Y1 to Y384.
2. Vyo is the output voltage of analog output pins Y1 to Y384.
3. dVrms = max. deviation of (VHx-VLx)
VHx; the x gray level positive polarity driver output voltage
VLx; the x gray level negative polarity driver output voltage
4. CLK1 period = 20.68 μs raster cycle at fCLKP = 65 MHz, input data pattern = 1010……, (checkerboard pattern) alternating data pattern per CLKP, Ta = 25 °C.

5. CLK1 period = 20.68 μs raster cycle at fCLKP = 65 MHz, input data 00H fixed, alternating POL per raster cycle and VGMA1 = VDD2-0.2V, VGMA14 = VSS2 + 0.2V fixed, Ta = 25 °C.
6. Yout load condition : 120pF(tester load). Refer to Figure 4.
7. Yout load condition : No load(Yout open). Refer to Figure 4.

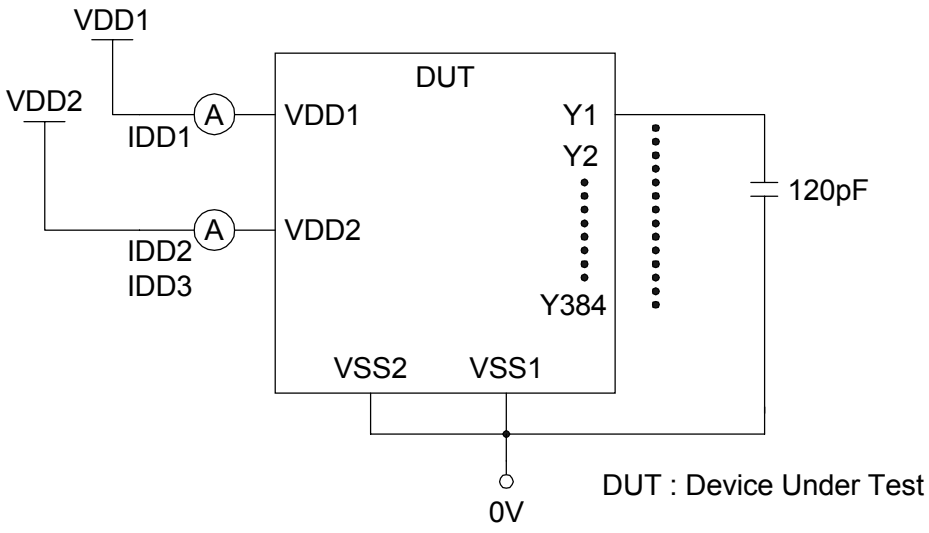


Figure 4. Yout Load Condition(IDD2&3)

RSDS CHARACTERISTICS

Table 6 . RSDS Characteristics
(Ta = - 20 to 75 °C, VDD1 = 2.7 to 3.6 V, VDD2 = 7.0 to 12.0 V, VSS1 = VSS2 = 0)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
RSDS high input voltage	VIH_{RSDS}	VCM_{RSDS} = + 1.1 V (1)	100	200	-	mV
RSDS low input voltage	VIL_{RSDS}	VCM_{RSDS} = + 1.1 V (1)	-	- 200	- 100	
RSDS common mode input voltage range	VCM_{RSDS}	VIH_{RSDS}=+100 mV VIL_{RSDS}=-100mV (2)	0.9	-	1.3	V
RSDS input leakage current	IDL	DxxP, DxxN, CLKP, CLKN	- 10	-	10	µA

NOTES:
1. VCM_{RSDS} = (VCLKP + VCLKN) / 2 or VCM_{RSDS} = (VDxxP + VDxxN) / 2
2. The positive sign means that DxxP(or CLKP) is higher than RSDS ground DxxN(or CLKN).
   The negative sign means that DxxP(or CLKP) is lower than RSDS ground DxxN(or CLKN).

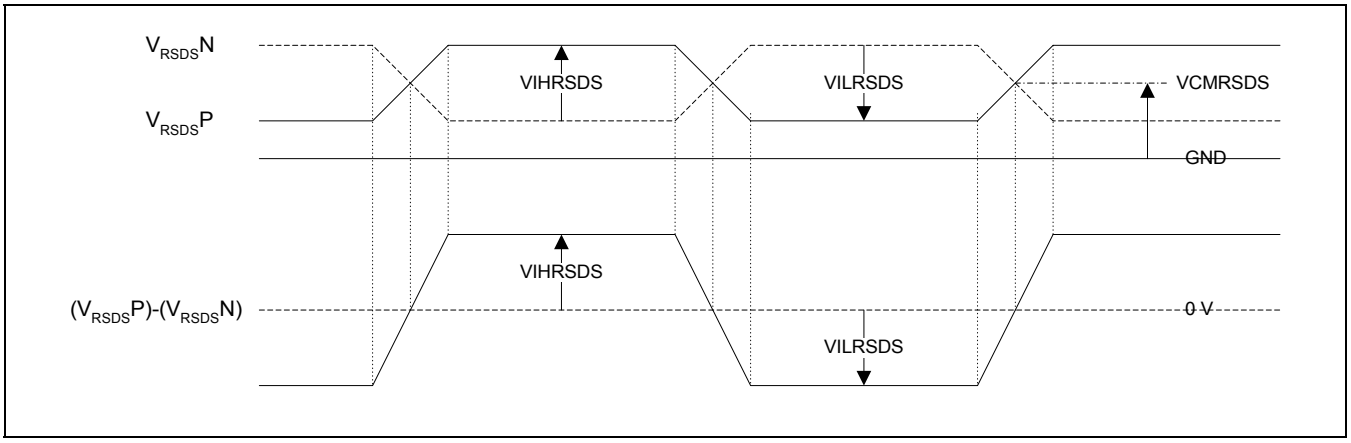


Figure 5. RSDS signal definition

AC CHARACTERISTICS

Table 7. AC Characteristics
(Ta = - 20 to 75 °C, VDD1 = 2.7 to 3.6 V, VDD2 = 7.0 to 12.0 V, VSS1 = VSS2 = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse width	PWCLK	-	11.7	-	-	ns
Clock pulse low period	PWCLK(L)	-	4	-	-	
Clock pulse high period	PWCLK(H)	-	4	-	-	
Data setup time	tSETUP1	(1)	2	-	-	
Data hold time	tHOLD1	(1)	0	-	-	
Start pulse setup time	tSETUP2	(1)	4	-	-	
Start pulse hold time	tHOLD2	(1)	2	-	-	
Start pulse delay time	tPLH1	CL = 15pF	-	-	7.7	
DIO signal pulse width	PWDIO	-	1CLKP	-	2CLKP	CLKP period
CLK1 setup time	tSETUP3	-	2CLKP	-	-	
CLK1 high pulse width	PWCLK1	-	5CLKP	-	-	
Driver output delay time1	tPHL1	(2) (4)	-	-	6	µs
Driver output delay time2	tPHL2	(3) (4)	-	-	10	
Last data timing	tLDT	-	1CLKP	-	-	CLKP period
CLK1-CLKP time	tCLK1-CLKP	CLK1 ↑ → CLKP ↓	4	-	-	ns
POL-CLK1 time	tPOL-CLK1	POL ↑ or ↓ → CLK1 ↑	14	-	-	
CLK1-POL time	tCLK1-POL	CLK1↓ → POL ↑ or ↓	10	-	-	

NOTES:
(1). VCM_{RSDS} = +1.1V, $VDIFF_{RSDS}$ = $V_{RSDS}P$ - $V_{RSDS}N$ = ±200mV
(2). The value is specified when the drive voltage value reaches the target output voltage level of 90%
(3). The value is specified when the drive voltage value reaches the target output voltage level of 6-bit accuracy.
(4). Yout load condition (refer to Figure 6)

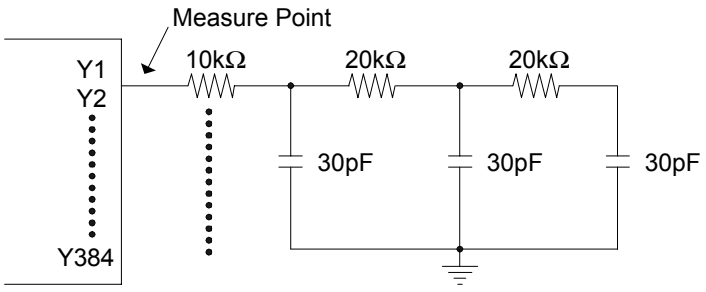


Figure 6. Yout load condition

WAVEFORMS

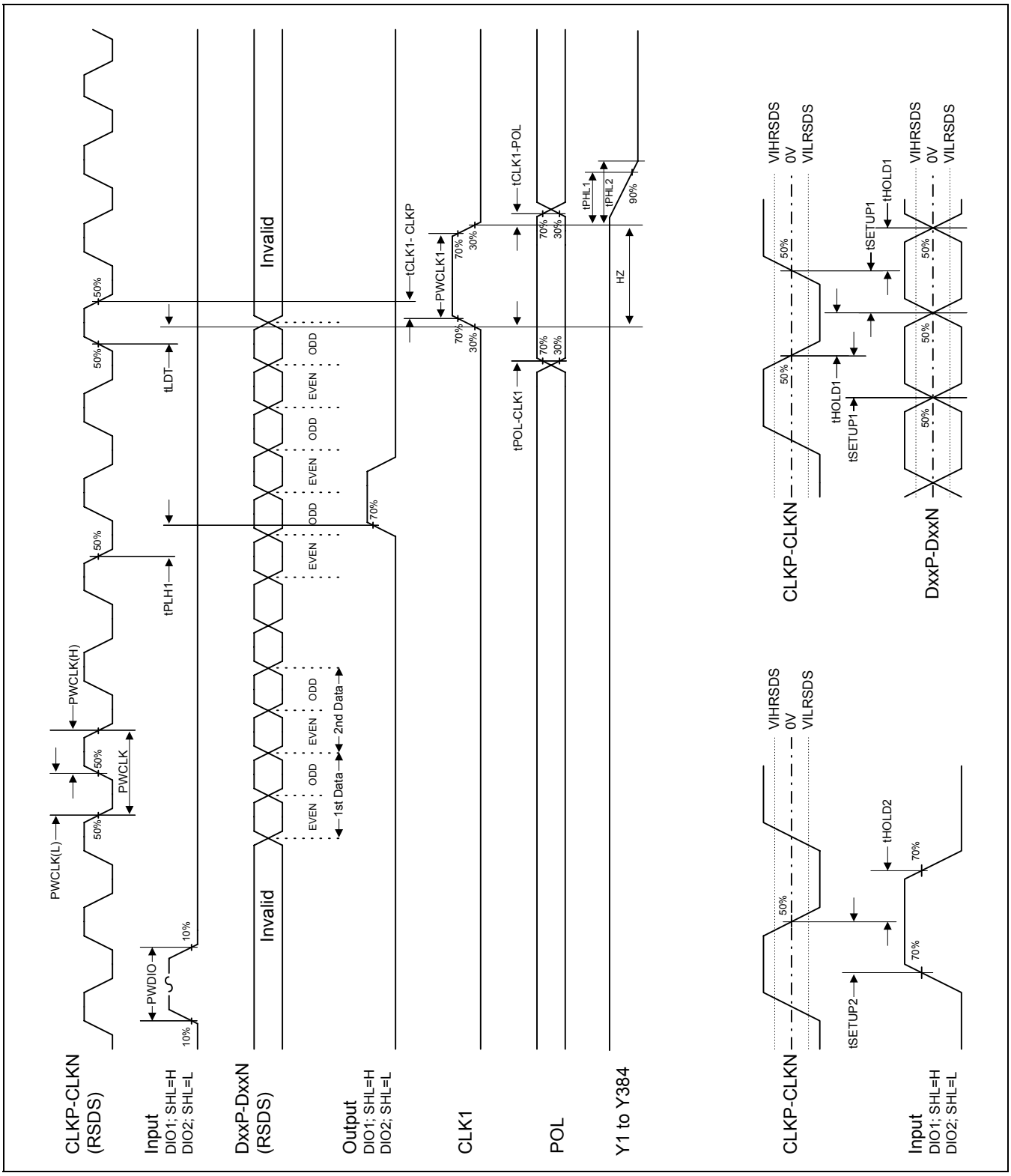


Figure 7. Waveforms

SAMSUNG ELECTRONICS

RELATIONSHIPS BETWEEN CLK1, START PULSE (DIO1, DIO2) AND BLANKING PERIOD

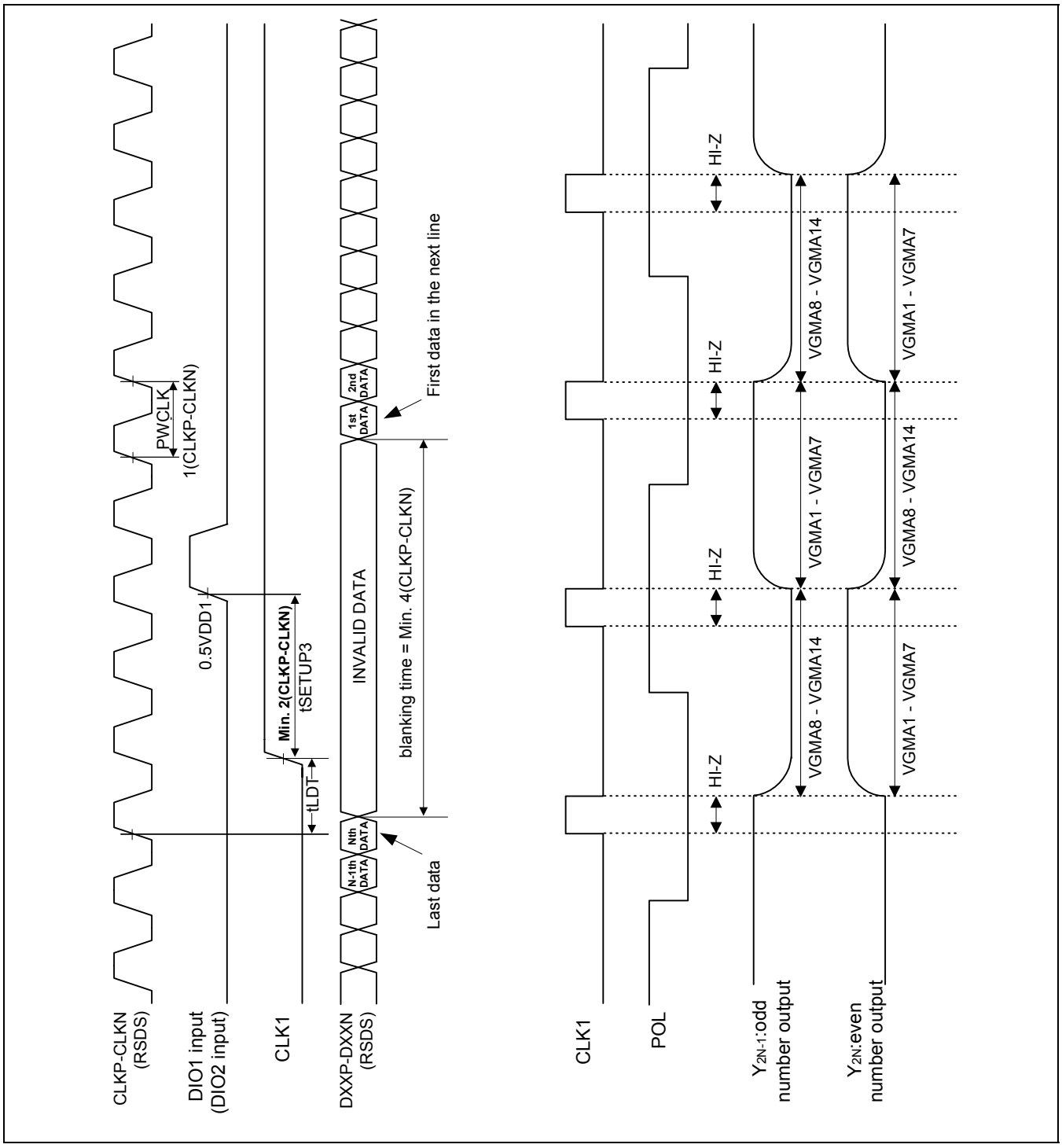


Figure 8. Waveforms

RSDS DATA TIMING DIAGRAM

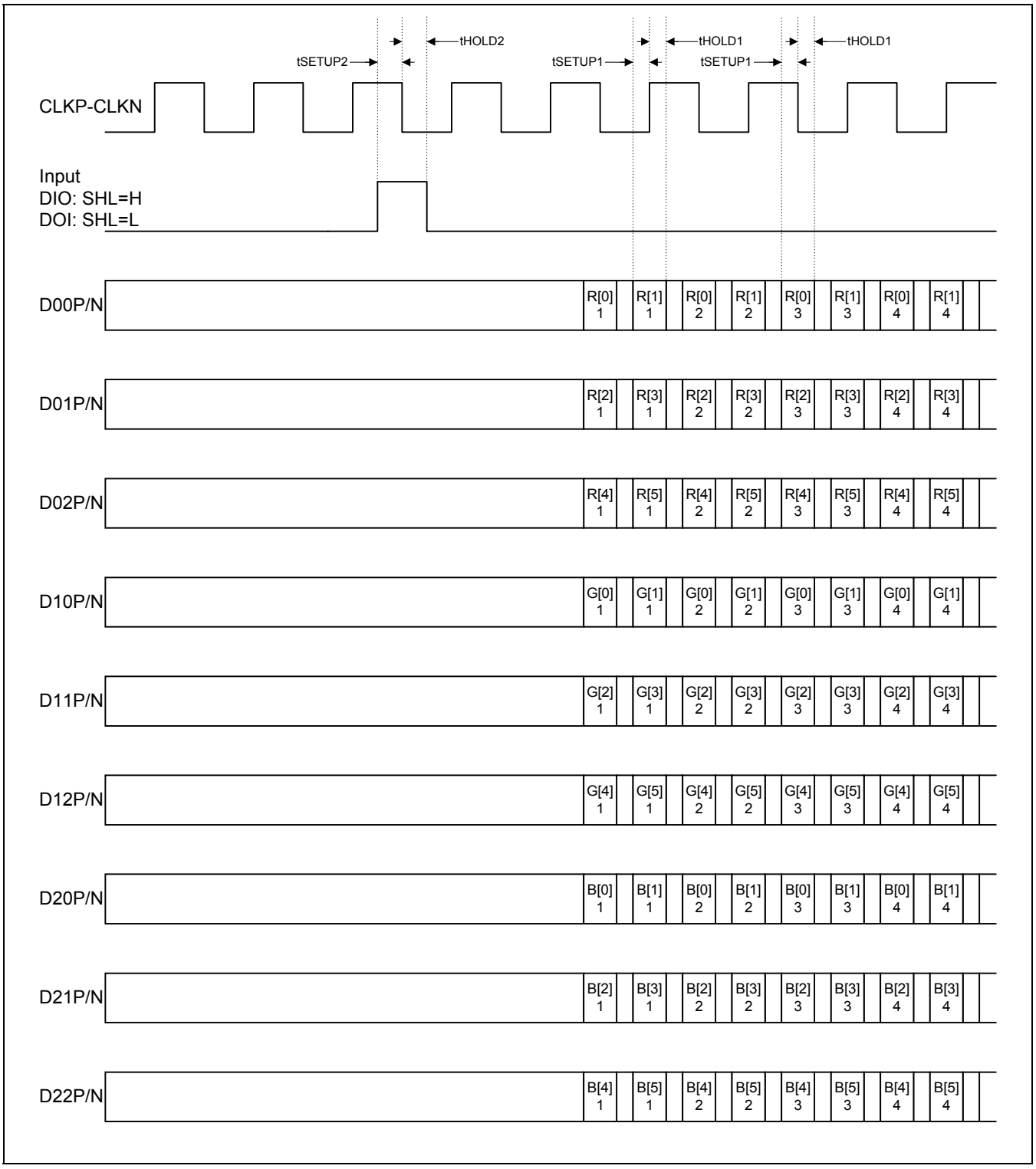


Figure 9. RSDS Data Timing Diagram