



# ISL9220, ISL9220A

## Pin Descriptions

PIN	SYMBOL	DESCRIPTION
1	STAT2	Open-drain indication pin. In conjunction with STAT1 this pin provides a unique indication for each charging state of the cycle. This pin is capable to sink 10mA minimum current to drive an LED.
2	$\overline{\text{EN}}$	IC enable input. Drive this pin to logic LO to enable the charger. Drive this pin to logic HI to disable the charger. Do not leave this pin floating.
3	AGND	Analog ground.
4	ISET1	Charge current programing pin. Connect a resistor between this pin and the GND pin to set the charge current.
5	ISET2	End-of-charge current programing pin. Connect a resistor between this pin and the GND pin to set the end-of-charge current.
6	VBAT	Battery connection pin. Connect this pin to the battery. A 10 $\mu$ F or larger X5R ceramic capacitor is recommended for decoupling and stability purposes.
7	ISNS	Output current sense pin. Connect a current sense resistor from this pin to V <sub>BAT</sub> . No decoupling capacitor is needed at this pin.
8	CISP	Input current sense positive connection pin. Connector a sense resistor from this pin the CISP.
9	CISN	Input current sense negative connection pin. Connector a sense resistor from this pin the CISN.
10, 11	VIN	Input supply voltage. Connect a 4.7 $\mu$ F ceramic capacitor from VIN to PGND.
12	VHI	High-side NMOS FET gate drive supply pin. Connect the anode of a Schottky diode to VBIAS pin and the cathode to VHI pin. Connect a 0.1 $\mu$ F capacitor from VHI pin to SW pin. See "Typical Application Diagrams" on page 6.
13, 14	SW	Switch node and inductor connection pin.
15, 16	PGND	Power ground.
17	VBIAS	Internal 5V regulator output. Connect a 0.1 $\mu$ F ~ 4.7 $\mu$ F ceramic capacitor from this pin to AGND. A typical 1 $\mu$ F ceramic capacitor is recommended.
18	RTH	Input for an external NTC thermistor for battery temperature monitoring.
19	TIME	The TIME pin sets the oscillation period by connecting a timing capacitor between this pin and GND. The oscillator also provides a time reference for the charger. The timer function can be disabled by connecting the TIME pin to GND. If the timer is disabled, there will be no timeout function for any operation mode including trickle charge and fast charge modes.
20	STAT1	Open-drain indication pin. In conjunction with STAT2 this pin provides a unique indication for each charging state of the cycle. This pin is capable to sink 10mA minimum current to drive an LED.
	EPAD	Exposed pad. Connect to GND electrically. Thermally, connect as much as possible copper to this pad either on the component layer or other layers through thermal vias to enhance the thermal performance.

## Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	NUMBER OF CELLS	TEMP. RANGE (°C)	PACKAGE Tape & Reel (Pb-free)	PKG. DWG. #
ISL9220IRTZ-T	92 20IRTZ	1	-40 to +85	20 Ld 4x4 TQFN	L20.4x4E
ISL9220IRTZ-T7A	92 20IRTZ	1	-40 to +85	20 Ld 4x4 TQFN	L20.4x4E
ISL9220AIRTZ-T	922 0AIRTZ	2	-40 to +85	20 Ld 4x4 TQFN	L20.4x4E
ISL9220AIRTZ-T7A	922 0AIRTZ	2	-40 to +85	20 Ld 4x4 TQFN	L20.4x4E
ISL9220IRTZEVAL1Z	Evaluation Board				
ISL9220AIRTZEVAL1Z	Evaluation Board				

### NOTES:

1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL9220, ISL9220A](#). For more information on MSL please see techbrief [TB363](#).

# ISL9220, ISL9220A

## Absolute Maximum Ratings

VIN, CISP, CISN	-0.3V to 18V
SW	-0.7V to 18V
VHI	-0.3V to 24V
VBAT, ISNS	-0.3V to 10V
ISET1, ISET2, RTH, VBIAS, STAT1, STAT2, EN	-0.3V to 5.5V
TIME	-0.3V to 2.75V
Input Current (VIN)	2.0A
Output Current (SW)	2.2A
<b>ESD Rating</b>	
Human Body Model (Tested per JESD22-A114F)	2500V
Machine Model (Tested per EIA/JESD22-A115-A)	175V
Charged Device Model (Tested per JES22-C101D)	1500V
<b>Latch-Up</b>	
(Tested per JESD-78B; Class 2 (+85°C), Level A)	100mA

## Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
4x4 QFN Package (Notes 4, 5)	40	4.3
Maximum Junction Temperature (Plastic Package)	+150°C	
Maximum Storage Temperature Range	-65°C to +150°C	
Pb-Free Reflow Profile	see link below	
	<a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>	

## Recommended Operating Conditions

Ambient Temperature Range	-40°C to +85°C
<b>Supply Voltage, VIN</b>	
ISL9220	4.5V to 14V
ISL9220A	9V to 14V
Programmable Charge Current	200mA to 2A
Programmable Trickle Current	20mA to 200mA

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTES:

- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- $\theta_{JC}$ , "case temperature" location is at the center of the exposed metal pad on the package underside.

## Electrical Specifications

Typical specifications are measured at the following conditions:  $T_A = +25^\circ\text{C}$ ; For ISL9220,  $V_{IN} = 5\text{V}$ ; For ISL9220A,  $V_{IN} = 12\text{V}$ .

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER-ON RESET</b>						
Rising $V_{IN}$ Threshold	$V_{POR\_R}$		3.4	3.6	3.8	V
Falling $V_{IN}$ Threshold	$V_{POR\_F}$		2.2	2.4	2.6	V
<b><math>V_{IN} - V_{BAT}</math> OFFSET VOLTAGE</b>						
Rising Offset Threshold	$V_{OS\_R}$	ISL9220	-	95	150	mV
		ISL9220A	-	170	300	mV
Falling Offset Threshold	$V_{OS\_F}$	ISL9220	10	65	-	mV
		ISL9220A	20	130	-	mV
<b>SUPPLY CURRENT</b>						
VIN Pin Supply Current	$I_{CC(VIN)}$	PGOOD = TRUE, $\overline{EN} = L$ (Note 6)		10	15	mA
		PGOOD = TRUE, $\overline{EN} = H$ (Note 6) $V_{IN} = 5\text{V to }12\text{V}$	-	-	0.5	mA
Battery Discharge Current (Total of currents flowing into VBAT, ISNS, SW pins)	$I_{DIS}$	$V_{IN} < V_{POR}$ OR $\overline{EN} = H$ $2\text{V} < V_{BAT} < 11\text{V}$	-	2	5	$\mu\text{A}$
<b>OVERVOLTAGE PROTECTION</b>						
Input OVP Rising Threshold	$V_{IN\_OVPR}$		14.5	15.0	15.5	V
Input OVP Falling Threshold	$V_{IN\_OVPF}$		14.0	14.5	15.0	V
<b>OUTPUT CURRENT</b>						
Fast Charge Current Accuracy	$I_{CHG}$	RSNS = 0.039 $\Omega$ RISET1 = 49.9k $\Omega$ (Nominal $I_{OUT} = 1000\text{mA}$ )	-10	-	10	%
Charge Termination Current Accuracy	$I_{MIN}$	RSNS = 0.039 $\Omega$ RISET2 = 300k $\Omega$ (Nominal $I_{MIN} = 100\text{mA}$ )	-35	-	35	%
Charge Termination Detection Deglitch Time			-	12	-	ms

# ISL9220, ISL9220A

## Electrical Specifications

Typical specifications are measured at the following conditions:  $T_A = +25^\circ\text{C}$ ; For ISL9220,  $V_{IN} = 5\text{V}$ ; For ISL9220A,  $V_{IN} = 12\text{V}$ . (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Level 1 Pre-Charge Current Range (Linear mode)	$I_{PCHG1}$	$V_{BAT} < V_{PCHG1}$	25	50	90	mA
Level 2 Pre-Charge Current Accuracy	$I_{PCHG2}$	$R_{SNS} = 0.039\Omega$ $R_{ISET2} = 300k\Omega$ (Nominal $I_{PCHG} = 140\text{mA}$ )	-	$\pm 20$	-	%
Level 1 Pre-Charge Threshold Voltage	$V_{PCHG1}$	ISL9220	2.42	2.5	2.56	V
		ISL9220A	4.8	5.0	5.3	V
Level 2 Pre-Charge Threshold Voltage	$V_{PCHG2}$	ISL9220	2.9	3.0	3.1	V
		ISL9220A	5.75	6.0	6.25	V
<b>RECHARGE THRESHOLD</b>						
Recharge Voltage Threshold	$V_{RECHG}$	ISL9220	3.85	4.0	4.1	V
		ISL9220A	7.75	8.0	8.25	V
<b>TEMPERATURE MONITORING</b>						
High Battery Temperature Threshold	$V_{TMIN}$	Specified as % of $V_{BIAS}$	30	35	40	%
Low Battery Temperature Threshold	$V_{TMAX}$	Specified as % of $V_{BIAS}$	70	75	80	%
Battery Removal Threshold	$V_{RMV}$	Specified as % of $V_{BIAS}$	90	95	-	%
Thermistor Disable Threshold	$V_{T\_DIS}$		-	250	-	mV
Temperature Threshold Hysteresis	$V_{T,HYS}$		-	180	-	mV
Temperature Detection Deglitch Time			-	12	-	ms
<b>THERMAL PROTECTION</b>						
Thermal Shutdown Threshold	$T_{FD}$		-	140	-	$^\circ\text{C}$
Thermal Hysteresis	$T_{HYS}$		-	30	-	$^\circ\text{C}$
<b>VBIAS OUTPUT</b>						
Output Voltage	$V_{BIAS}$	$5.3 < V_{IN} < 15\text{V}$ , $I_{VBIAS} = 5\text{mA}$	4.70	5.0	5.25	V
Output Current	$I_{BIAS}$	$5.3 < V_{IN} < 15\text{V}$	-	-	5	mA
<b>OSCILLATOR</b>						
Oscillation Period	$t_{OSC}$	$C_{TIME} = 15\text{nF}$	-	3.0	-	ms
<b>SWITCHING CHARGER AC CHARACTERISTICS</b>						
Switching Frequency	$F_{OSC}$		1.02	1.2	1.38	MHz
Maximum Duty Cycle	$D_{MAX}$		-	96	-	%
Minimum Duty Cycle	$D_{MIN}$		-	0	-	%
Cycle-By-Cycle Current Limit	$I_{LIM}$		-	3.0	-	A
<b>SWITCHING CHARGER DC CHARACTERISTICS</b>						
High-Side MOSFET ON-Resistance	$r_{DS(ON), HS1}$		-	112	-	$\text{m}\Omega$
Combined High Side ON-Resistance (Note 7)	$r_{DS(ON), HS2}$	Measured between $V_{IN}$ and SW pins	-	224	450	$\text{m}\Omega$
Low-Side MOSFET ON-Resistance	$r_{DS(ON), L}$		-	72	180	$\text{m}\Omega$
High-Side Path Reverse Leakage Current	$I_{REV}$	$V_{IN} = 0\text{V}$ , $V_{SW} = 15\text{V}$	-	1.0	5.0	$\mu\text{A}$
Charger Output Voltage	$V_{CHG}$	ISL9220, $I_{OUT} = 100\text{mA}$ , $T_A = +25^\circ\text{C}$	4.179	4.2	4.221	V
		ISL9220A, $I_{OUT} = 100\text{mA}$ , $T_A = +25^\circ\text{C}$	8.358	8.4	8.442	V
		ISL9220, $I_{OUT} = 100\text{mA}$	4.158	4.2	4.242	V
		ISL9220A, $I_{OUT} = 100\text{mA}$	8.316	8.4	8.484	V

# ISL9220, ISL9220A

**Electrical Specifications** Typical specifications are measured at the following conditions:  $T_A = +25^\circ\text{C}$ ; For ISL9220,  $V_{IN} = 5\text{V}$ ; For ISL9220A,  $V_{IN} = 12\text{V}$ . (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>INPUT CURRENT SENSE AMPLIFIER</b>						
Input Bias Current at CSIP and CSIN, Pin (Charger Enabled)	$I_{ISIP\_ON}$	$\overline{EN} = L$	-	100	200	$\mu\text{A}$
Input Current Limit Threshold	$I_{IN\_LIM}$	CSIP-CSIN	88	100	112	mV
<b>OUTPUT CURRENT SENSE AMPLIFIER</b>						
Input Bias Current at ISNS Pin, (Charger Enabled)	$I_{ISNS\_ON}$	$\overline{EN} = L$	-	100	200	$\mu\text{A}$
Input Bias Current at ISNS Pin, (Charger Disabled)	$I_{ISNS\_OFF}$	$\overline{EN} = H$	-	-	1	$\mu\text{A}$
Input Bias Current at VBAT Pin, (Charger Enabled)	$I_{VBAT\_ON}$	$\overline{EN} = L$	-	75	100	$\mu\text{A}$
Input Bias Current at VBAT Pin, (Charger Disabled)	$I_{VBAT\_OFF}$	$\overline{EN} = H$	-	-	1	$\mu\text{A}$
<b>LOGIC INPUT AND OUTPUTS</b>						
$\overline{EN}$ Pin Logic High			1.3	-	-	V
$\overline{EN}$ Pin Logic Low			-	-	0.4	V
STAT1, STAT2 Sink Current When ON		Pin Voltage = 0.4V	10	-	-	mA
STAT1, STAT2 Leakage Current When OFF		Pin Voltage = 4.2V	-	-	1	$\mu\text{A}$

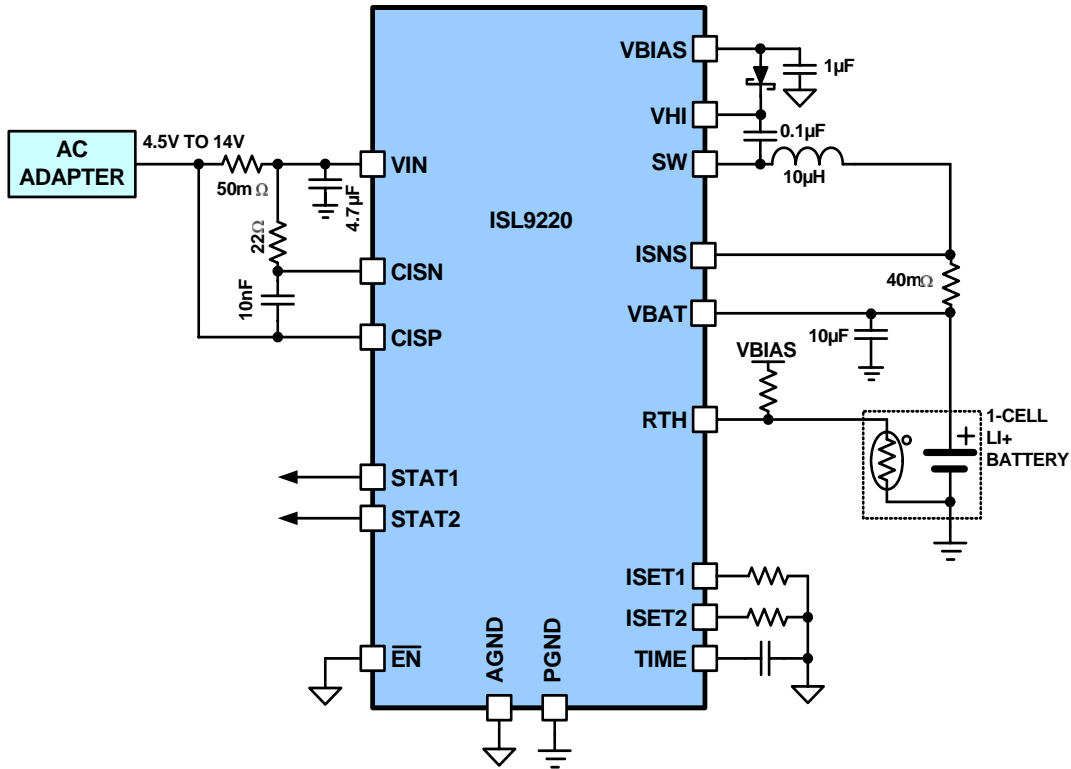
**NOTES:**

- PGOOD is defined as when  $V_{IN}$  and  $V_{BAT}$  meet all these conditions:  $V_{IN} > VPOR$ ,  $V_{IN} - V_{BAT} > VOS$ ,  $V_{IN} < V_{IN(OVP)}$ .
- Limits should be considered typical and are not production tested.

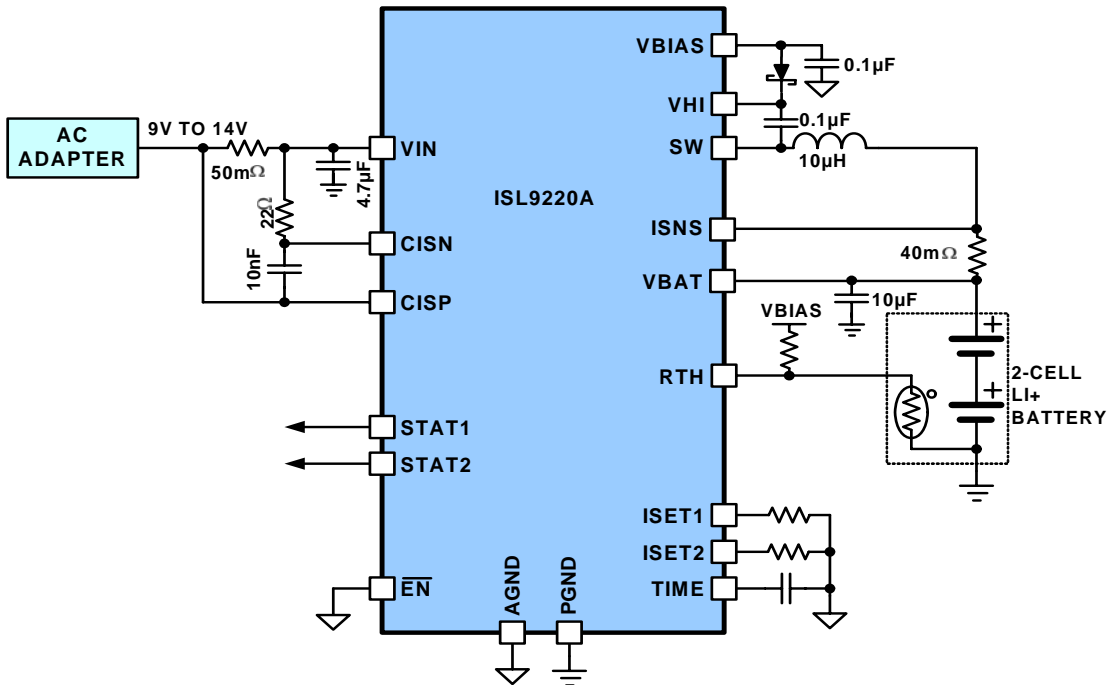
# ISL9220, ISL9220A

## Typical Application Diagrams

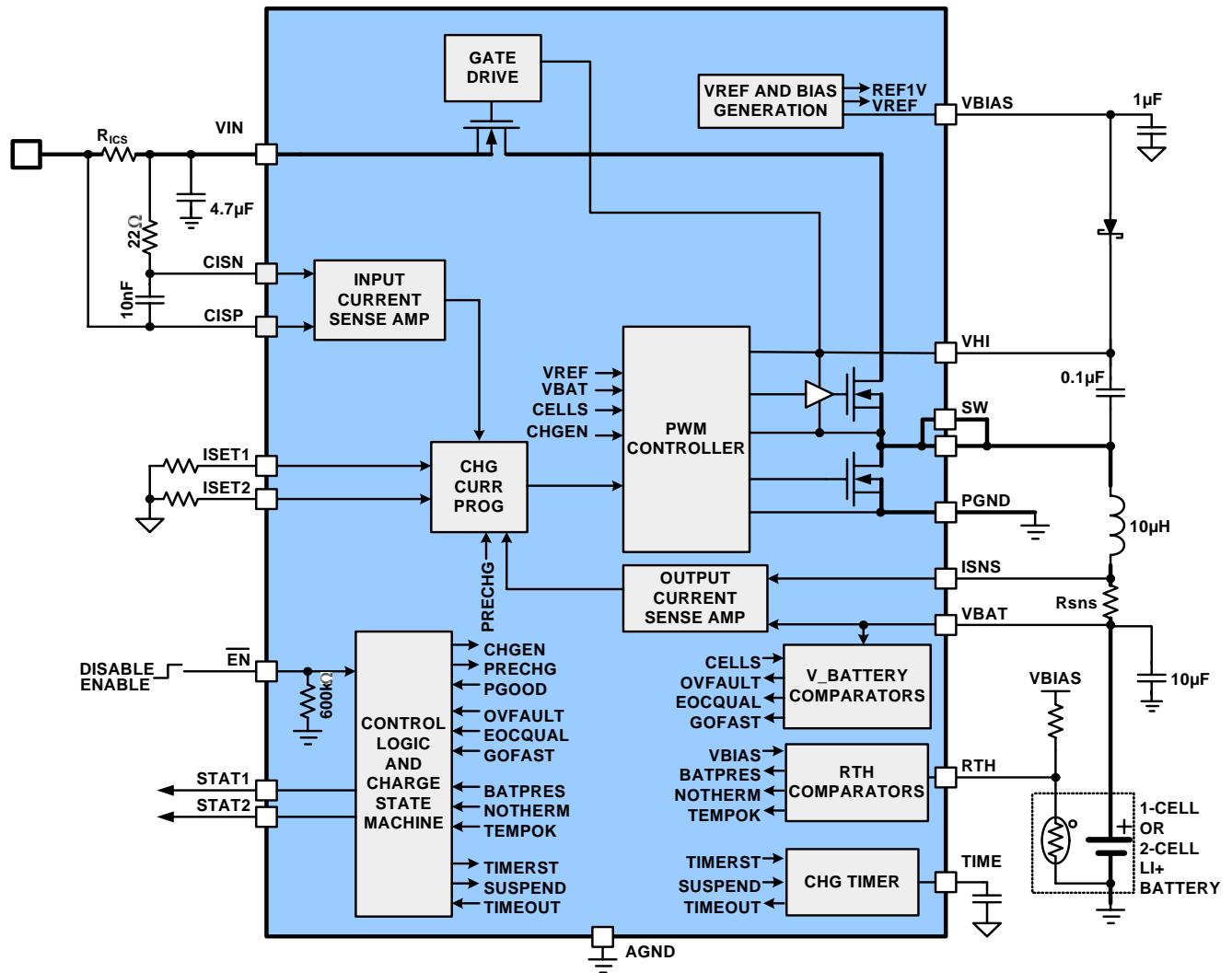
### 1-Cell Application



### 2-Cell Application



## Block Diagram



## Typical Operating Conditions

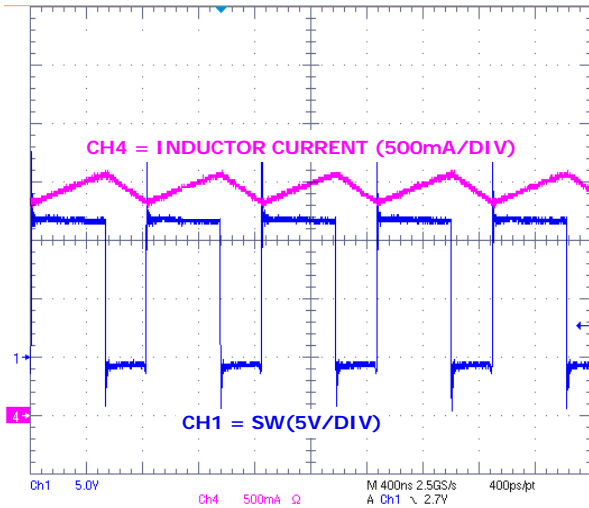


FIGURE 1. PWM WAVEFORM IN CC MODE

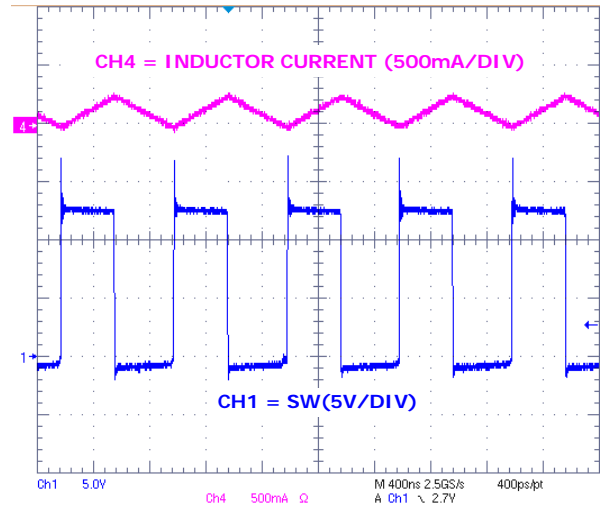


FIGURE 2. PWM WAVEFORM IN TRICKLE MODE

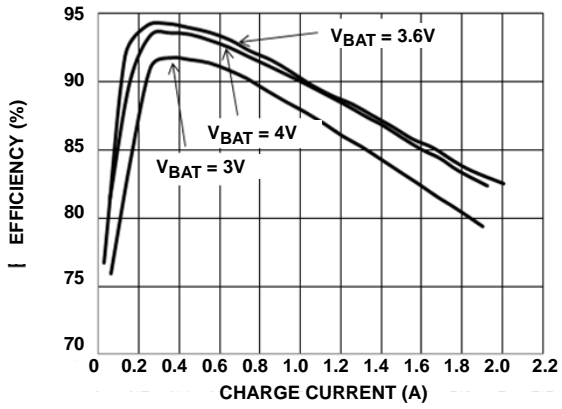


FIGURE 3. EFFICIENCY vs LOAD 1-CELL ( $V_{IN} = 5V$ ,  $L = 10\mu H$ )

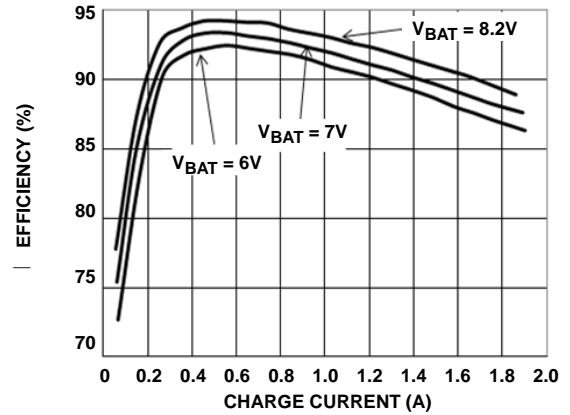


FIGURE 4. EFFICIENCY vs LOAD 2-CELL ( $V_{IN} = 12V$ ,  $L = 10\mu H$ )



## Theory of Operation

The ISL9220, ISL9220A is an integrated charger optimized for charging 1-cell and 2-cell Li-ion or Li-polymer batteries. It charges a battery with constant current (CC) and constant voltage (CV) profile. The typical charge profile is illustrated in Figure 5.

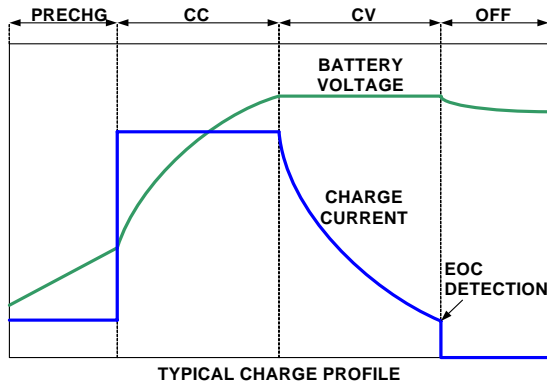


FIGURE 5. TYPICAL CHARGE PROFILE

### POR and Power-Good

The ISL9220, ISL9220A resets itself when  $V_{IN}$  undergoes transition from below  $V_{POR}$  to above  $V_{POR}$  threshold.

The ISL9220, ISL9220A has an internal PGOOD signal. Charging is prohibited if PGOOD statement is not true. See Note 6 in the "Electrical Specifications" table for the definition of PGOOD.

### Valid Charge Temperatures

An external NTC thermistor can be used to provide temperature-qualified charging. The  $V_{BIAS}$  supply is used as reference for the internal comparators. Thus, it is important that the  $V_{BIAS}$  supply also be used to bias the external voltage divider comprised of one or more fixed resistors and the thermistor. This scheme allows the use of a wide variety of thermistors. The RTH comparator block monitors the RTH pin voltage to determine if the battery temperature is within safe charging limits.

The ISL9220, ISL9220A uses two comparators (CP2 and CP3) to form a window comparator, as shown in Figure 6. When the NTC pin voltage is "out of the window," determined by the  $V_{TMIN}$  and  $V_{TMAX}$ , the ISL9220, ISL9220A stops charging and indicate a suspend condition. When the temperature returns to the set range, the charger resumes charging. The two MOSFETs, Q1 and Q2, produce hysteresis for both upper and lower thresholds. The temperature window is shown in Figure 7 for a 0°C to +50°C typical application using an industry standard type 103AT thermistor.

The temperature qualification function can be disabled by connecting the RTH pin to ground.

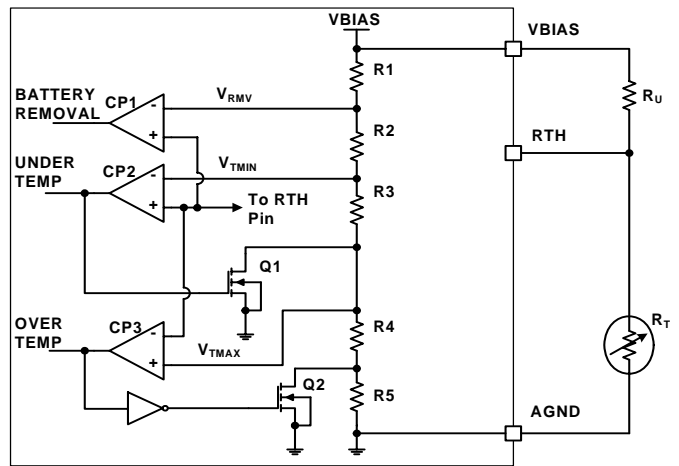


FIGURE 6. THERMISTOR INTERNAL CIRCUIT

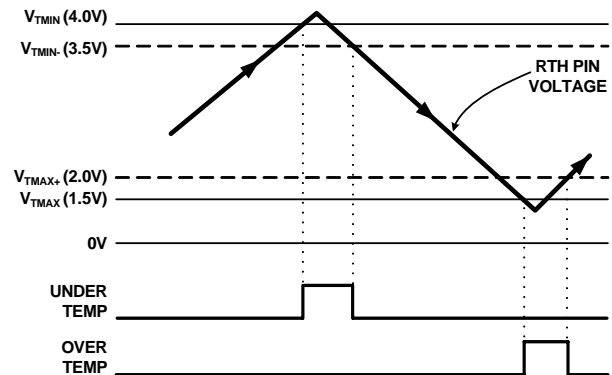


FIGURE 7. THRESHOLD VOLTAGES FOR 0°C to +50°C WINDOW ( $V_{BIAS} = 5.0V$ )

### Battery Detection

The presence or absence of the external thermistor is used to detect a battery.

When  $V_{RTH}$  is greater than  $V_{RTH,PRES}$ , i.e. when the RTH pin is not connected to ground, battery detection is provided by the RTH comparator block, as shown in Figure 6. With no battery connected, the RTH pin is pulled to  $V_{BIAS}$  by  $R_U$ , and thus  $V_{RTH}$  will exceed the  $V_{RTH,NOBAT}$  threshold. The internal battery presence signal is deglitched with a 12ms deglitcher, to avoid false indication of battery insertion or removal due to contact bounce or other noises.

### Battery Precharge

When the charger is first enabled and no fault conditions are detected, if the battery connecting to the charger is deeply discharged, the charger will charge the battery in a reduced current for the battery to recover.

If the battery voltage is less than the level 1 pre-charge voltage ( $V_{PCHG1}$ ), the charger operates in LDO mode, with an output current fixed at 50mA typical. In this mode, the output voltage can go to 0V. This provides the ability to recover a battery that has entered a safety-circuit undervoltage fault mode.

$$I_{PCHG1} = 50\text{mA} \quad (\text{EQ. 1})$$

If battery voltage is between the level 1 pre-charge voltage ( $V_{PCHG1}$ ) and level 2 pre-charge voltage ( $V_{PCHG2}$ ), the charger operates in trickle mode, and uses the precharge current limit. This precharge current is programmed by the resistor between the ISET2 pin and ground. Note that this resistor also programs the end-of-charge taper current threshold.

$$I_{PCHG2} = \frac{1638}{R_{ISET2} \times R_{SNS}} \quad (\text{mA}) \quad (\text{EQ. 2})$$

Where  $R_{ISET2}$  is in  $k\Omega$  and  $R_{SNS}$  is in  $\Omega$ .

When the battery voltage exceeds the level 2 pre-charge voltage threshold ( $V_{PCHG2}$ ), fast charging will commence. If this threshold is not reached within the precharge timer period, a TIME-OUT-FAULT condition is asserted, and the charger is disabled.

## Charge Safety Timer

An internal oscillator establishes a timing reference. The oscillation period is programmable with an external capacitor at the TIME pin,  $C_{Time}$ , as shown in the “Typical Application Diagrams” on page 6. The oscillator charges the timing capacitor to 1.5V and then discharges it to 0.5V in one period, both with 10 $\mu$ A current. The period  $t_{OSC}$  is calculated in Equation 3:

$$t_{OSC} = 0.2 \times 10^6 \times C_{Time} \quad (\text{Sec}) \quad (\text{EQ. 3})$$

Where  $C_{Time}$  is in F.

A 1nF capacitor provides 0.2ms oscillation period. The allowable range of  $C_{Time}$  value is 100pF to 1 $\mu$ F, providing a programmable charge safety-timeout range of about 1.4 minutes to almost 10 days.

Total charge time, excluding any time required for precharge, is limited to a length of TIMEOUT. This can be calculated as Equation 4:

$$\text{TIMEOUT} = 2^{22} \times t_{OSC} \quad (\text{Sec}) \quad (\text{EQ. 4})$$

Total charge time for battery precharge is limited to a length of 1/8 TIMEOUT. This can be calculated as Equation 5:

$$\text{TIMEOUT(PCHG)} = 2^{19} \times t_{OSC} \quad (\text{Sec}) \quad (\text{EQ. 5})$$

The TIME pin can be grounded to disable the safety timer functions if not needed.

## Fast Charge

The fast charge current is programmed by the resistor between the ISET1 pin and ground, and by the value of the  $R_{SNS}$  resistor (see Equation 6).

$$I_{CHG} = \frac{1946}{R_{ISET1} \times R_{SNS}} \quad (\text{mA}) \quad (\text{EQ. 6})$$

Where  $R_{ISET1}$  is in  $k\Omega$  and  $R_{SNS}$  is in  $\Omega$ .

For best accuracy, select a  $R_{SNS}$  value that provides between 40mV to 80mV differential voltage across  $R_{SNS}$  at the desired maximum peak current (DC plus ripple).

## Charge Termination

Charge current is continuously monitored. When the current falls below the taper current threshold, charging will stop, and BATFUL is asserted to indicate a successful charge completion. This taper current threshold is programmed by a single external resistor between ISET2 and ground as calculated in Equation 7.

$$I_{EOC} = \frac{1170}{R_{ISET2} \times R_{SNS}} \quad (\text{mA}) \quad (\text{EQ. 7})$$

Where  $R_{ISET2}$  is in  $k\Omega$  and  $R_{SNS}$  is in  $\Omega$ .

A secondary charge termination method is provided via the safety timer. The timeout period of this timer is programmable via a single external capacitor between the TIME pin and ground.

To disable the charge safety timer, short the TIME pin to ground.

## Charge Current Sensing

Charge current is sensed with an external current sense resistor. A low-inductance, precision resistor should be used for accurate charge current.

## Input Current Sensing

Input current is sensed with an external sense resistor. A low-inductance, precision resistor should be used for accurate input current limit.

The ISL9220, ISL9220A limits the battery charge current when the input current limit threshold is exceeded. This allows the most efficient use of AC-adaptor power without overloading the adaptor output.

An internal amplifier compares the voltage between CSIP and CSIN, and reduces the output current when this differential voltage exceeds the threshold voltage. The effective input current limit threshold is thus set by the value of the  $R_{ICS}$  resistor as calculated by Equation 8.

$$I_{IN(LIM)} = \frac{0.1}{R_{ICS}} \quad (\text{A}) \quad (\text{EQ. 8})$$

Where  $R_{ICS}$  is in  $\Omega$ .

A low pass filter is suggested to eliminate the switching noise, as shown in the “Typical Application Diagrams” on page 6.

## Status Outputs

TABLE 1. STAT1 AND STAT2 TRUE TABLE

STAT1	STAT2	CHARGING CONDITION
L	L	Precharge, or fast charge in progress
L	H	Charge Complete
H	L	Fault
H	H	Suspend

STAT1 and STAT2 are configured to indicate various charging conditions as given in Table 1.

A fault status is triggered under one of these conditions:

1.  $V_{BAT} > V_{OUT\_OVP}$  threshold
2. Timeout occurs before the EOC current has been reached

To exit the fault mode, the input power has to be recycled, or the EN pin is toggled to HI and back to LO.

## Applications Information

### Power-On Reset (POR)

The ISL9220, ISL9220A resets itself as the input voltage rises above the POR rising threshold. The internal oscillator starts to oscillate, the internal timer is reset, and the charger begins to charge the battery. The STAT1/2 pins will indicate the operating condition according to Table 1.

### Trickle Charge

If the battery voltage is below the trickle charge threshold, the ISL9220, ISL9220A delivers a small current to charge the battery until the battery voltage reaches the fast charge threshold value. There are two trickle charge thresholds. The first threshold,  $V_{PCHG1}$ , is to pre-charge a deeply discharged battery or short circuit. The second threshold,  $V_{PCHG2}$  is for batteries discharged to a voltage range from 2.5V to 3V. When  $V_{BAT}$  is below  $V_{PCHG1}$ , the ISL9220, ISL9220A operates as a linear regulator, providing a 50mA constant current to output. When  $V_{BAT}$  reaches  $V_{PCHG2}$ , the ISL9220, ISL9220A starts to operate as a switching charger. The trickle charge current is programmable by Riset2.

### Charge Cycle

A charge cycle consists of three charge modes: trickle mode, constant current (CC) mode, and constant voltage (CV) mode. The charge cycle always starts with the trickle mode until the battery voltage stays above  $V_{MIN}$  (3.0V typical). If the battery voltage stays below  $V_{MIN}$ , the charger stays in the trickle mode. The charger operates in CC mode after the battery voltage is above  $V_{MIN}$ . As the battery-pack terminal voltage rises to the final charge voltage, the CV mode operation begins. Since the battery terminal voltage is regulated at the constant output voltage in the CV mode, the charge current begins to drop. After the charge current drops below the end-of-charge level, which is programmed by Riset2. The ISL9220, ISL9220A indicates the end-of-charge (EOC) with STAT1 and STAT2 and terminates the charge. The following events initiate a new charge cycle:

- POR
- A new battery being inserted (detected by RTH pin)
- Recovery from an battery over-temperature fault
- The  $\overline{EN}$  pin is toggled from HI-to-LO

### Recharge

After a charge cycle completes at a timeout event, charging is prohibited until the recharge condition ( $V_{BAT} < V_{RECHG}$ ) is met, then the charging restarts with the timer reset to zero.

## Inductor and Output Capacitor Selection

To achieve better steady state and transient response, ISL9220, ISL9220A typically uses a 10 $\mu$ H inductor. The peak-to-peak inductor current ripple can be expressed in Equation 9:

$$\Delta I = \frac{V_{BAT} \cdot \left(1 - \frac{V_{BAT}}{V_{IN}}\right)}{L \cdot f_s} \quad (\text{EQ. 9})$$

In Equation 9, usually the typical values can be used but to have a more conservative estimation, the inductance should consider the value with worst case tolerance; and for switching frequency  $f_s$ , the minimum  $f_s$  from the "Electrical Specifications" table on page 3 can be used. A worst case for charge current ripple is when battery voltage is half of the input voltage.

To select the inductor, its saturation current rating should be at least higher than the sum of the maximum output current and half of the delta calculated from Equation 9. Another more conservative approach is to select the inductor with the current rating higher than the peak current limit.

Another consideration is the inductor DC resistance since it directly affects the efficiency of the converter. Ideally, the inductor with the lower DC resistance should be considered to achieve higher efficiency.

Inductor specifications could be different from different manufacturers so please check with each manufacturer if additional information is needed.

For the output capacitor, a ceramic capacitor can be used because of the low ESR values, which helps to minimize the output voltage ripple. A typical value of 10 $\mu$ F/10V ceramic capacitor should be enough for most of the applications and the capacitor should be X5R or X7R.

## Board Layout Recommendations

The ISL9220, ISL9220A is a high frequency switching charger and hence the PCB layout is a very important design practice to ensure a satisfactory performance.

The power loop is composed of the output inductor L, the output capacitor  $C_{OUT}$ , the SW pin and the PGND pin. It is important to make the power loop as small as possible and the connecting traces among them should be direct, short and wide; the same practice should be applied to the connection of the VIN pin, the input capacitor  $C_{IN}$  and PGND.

The switching node of the converter, the SW pin, and the traces connected to this node are very noisy, so keep the voltage feedback trace and other noise sensitive traces away from these noisy traces.

The input capacitor should be placed as close as possible to the VIN pin. The ground of the input and output capacitors should be connected as close as possible as well. In addition, a solid ground plane is helpful for a good EMI performance.

The ISL9220, ISL9220A employs a thermal enhanced QFN package with an exposed pad. In order to maximize the current capability, it is very important that the exposed pad under the package is properly soldered to the board and is connected to other layers through thermal vias. More thermal vias and more

copper attached to the exposed pad usually results in better thermal performance. The exposed pad is big enough for 5 vias as shown in Figure 8.

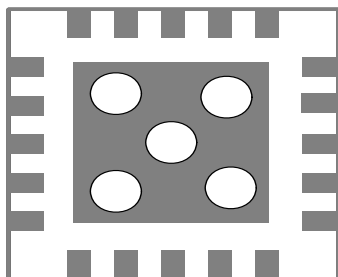


FIGURE 8. EXPOSED PAD

## Charging Flow Chart

The charging flow chart is shown in Figure 9. The charging starts with the trickle mode, the ISL9220, ISL9220A charges the battery in a trickle current. If  $V_{BAT}$  reaches  $V_{PCHG2}$  before the trickle charge timeout interval, the operation will change to CC mode. When the output voltage reaches the 4.2V final voltage, the operation will change to CV mode, where the battery is charged at a constant voltage. If the end-of-charge current is reached before the timeout interval is elapsed, the operation will come to charge complete state. The charging is terminated. After the termination, if the output voltage drops below the recharge threshold, a recharge starts and the timer is reset to zero.

In the event that the timeout condition is reached before EOC, the fault mode is entered. The fault mode can also be triggered by a  $V_{BAT}$  OVP event. To exit the fault mode, the input power has to be removed and re-applied, or the  $\overline{EN}$  pin is toggled to HI and back to LO, then a new cycle starts.

# ISL9220, ISL9220A

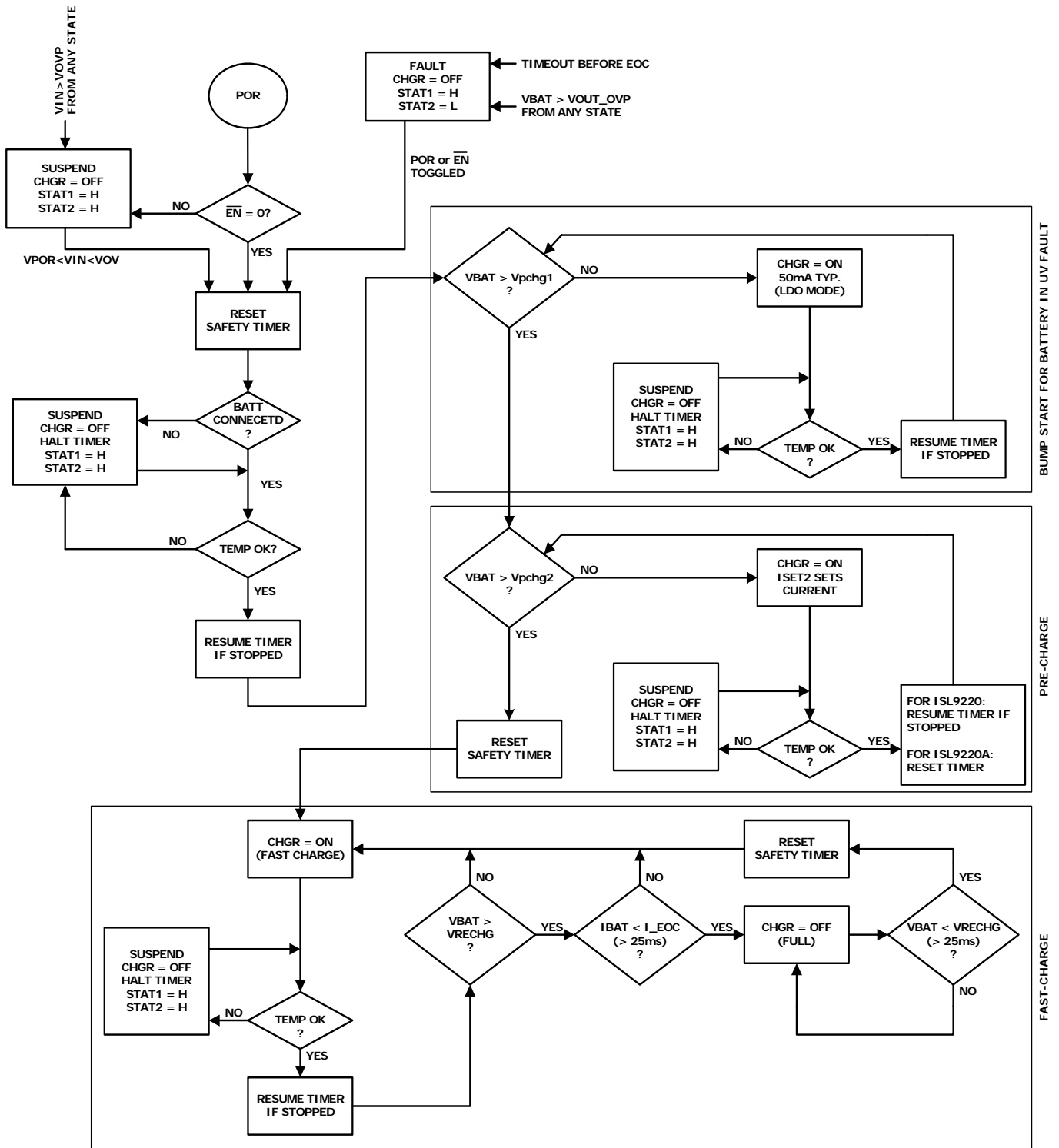


FIGURE 9. CHARGING FLOW CHART

# ISL9220, ISL9220A

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
December 16, 2011	FN6936.3	Moved the 10 $\mu$ F capacitor at the SW to the VBAT pin in "1-Cell Application" and "2-Cell Application" on page 6.
October 3, 2011		Added AN1589 to "Related Literature" on page 1. Changed Eval board names in "Ordering information" on page 2 from ISL9220EVAL1Z, ISL9220AEVAL1Z TO ISL9220IRTZEVAL1Z, ISL9220AIRTZEVAL1Z. In the "Pin Descriptions" on page 2: Pin 12, VHI. Changed "Connect a Schottky diode from VBIAS to this pin, and a 0.1mF capacitor to AGND, as shown in the Typical Application Circuits." to "Connect the anode of a Schottky diode to VBIAS pin and the cathode to VHI pin. Connect a 0.1 $\mu$ F capacitor from VHI pin to SW pin. See "Typical Application Diagrams" on page 6. Pin 17, VBIAS. Changed "Connect a 1 $\mu$ F ceramic capacitor from this pin to AGND." to "Connect a 0.1 $\mu$ F ~ 4.7 $\mu$ F ceramic capacitor from this pin to AGND. A typical 1 $\mu$ F ceramic capacitor is recommended"
August 11, 2010	FN6936.2	Added "Number of Cells" column to "Ordering Information" on page 2. Corrected input voltage in "2-Cell Application" on page 6 from "4.5V to 14V" to "9V to 14V"
July 1, 2010	FN6936.1	Changed minimum limit for "IPCHG1" on page 4 from 30 to 25mA. On page 4, changed "Minimum On-Time" with typical 20ns to "Minimum Duty Cycle" with typical of 0%. Changed minimum limit for "VPCHG1" on page 4 from 4.85 to 4.80V for only the "A option" Changed maximum limit for "VPCHG1" on page 4 from 5.25 to 5.3V for only the "A option" Changed minimum limit for "VPCHG2" on page 4 from 5.80V to 5.75V for only the "A option" Changed maximum limit for "VPCHG2" on page 4 from 6.2V to 6.25V for only the "A option" Changed minimum limit for "VRECHG" on page 4 from 7.80V to 7.75V for only the "A option" Changed maximum limit for "VRECHG" on page 4 from 8.20 to 8.25V for only the "A option"
June 30, 2010	FN6936.0	Initial Release.

## Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to [www.intersil.com/products](http://www.intersil.com/products) for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on [intersil.com](http://www.intersil.com): [ISL9220](http://www.intersil.com/ISL9220), [ISL9220A](http://www.intersil.com/ISL9220A)

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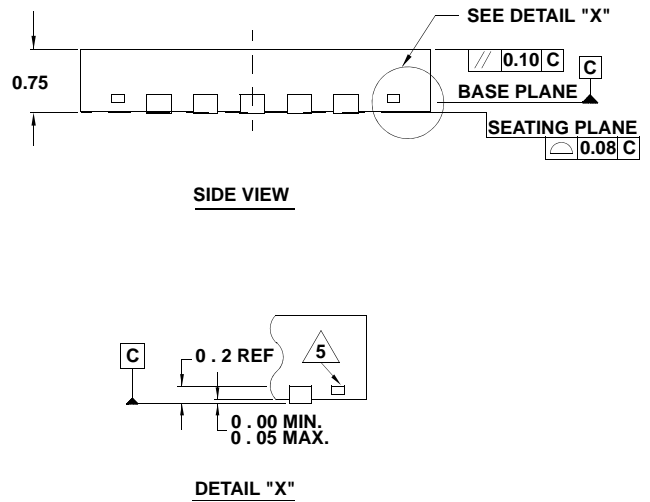
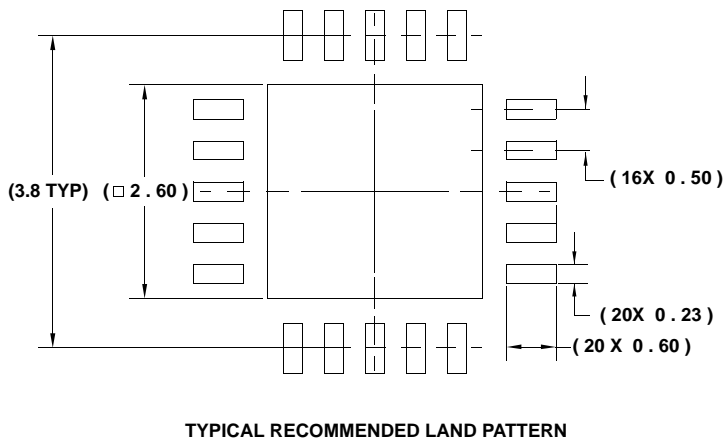
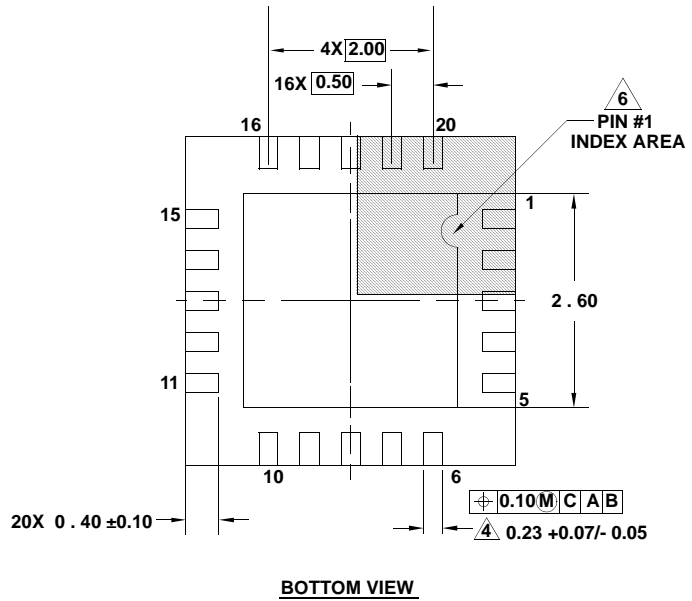
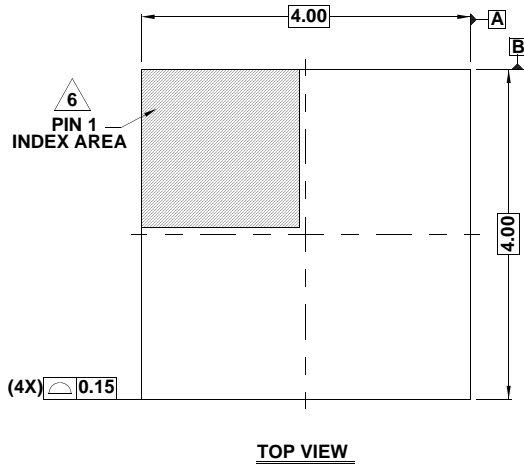
# ISL9220, ISL9220A

## Package Outline Drawing

### L20.4x4E

20 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

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#### NOTES:

1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal  $\pm 0.05$
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-229.