EMC1001

±1.5°C SMBus Temperature Sensor in Miniature TSOT

Features

- Self-Contained Internal Temperature Sensor
  - +0.25°C resolution
  - ±1.5°C Accuracy +40°C to +85°C
- SMBus Address Selected by External Resistor:
  - Select 1 of 4 per package, 8 addresses available
- Maskable Interrupt using $\overline{\text{ALERT}}$ pin
- One-shot Command during Standby
- Low Power, 3.0V to 3.6V Supply
- 47 µA at 0.0625 Conversions per Second (Typical)
- 4.8 µA in Standby (Typical)
- SMBus 2.0 Compliant interface
- Programmable Temperature Conversion Rate
- Small 6-lead TSOT package

Applications

- Desktop and Notebook Computers
- Thermostats
- Smart batteries
- Industrial/Automotive
- Other Electronic Systems

General Description

The EMC1001 is a tiny SMBus temperature sensor with ±1.5°C accuracy and two interrupts. Packaged in a SOT23-6, the EMC1001 provides an accurate, low-cost, low-current solution for critical temperature monitoring in a PC or in embedded applications.

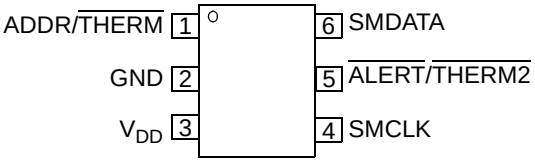
The EMC1001 generates two separate interrupts with programmable thermal trip points. The $\overline{\text{THERM}}$ output operates as a thermostat with programmable threshold and hysteresis. The $\overline{\text{ALERT}}$ output can be configured as a maskable SMBus alert with programmable window comparator limits, or as a second $\overline{\text{THERM}}$ output. An efficient fan control system can be created since this output may be used to control a fan.

A power-down mode extends battery life in portable applications.

Each part number may be configured to respond to one of four separate SMBus addresses.

Package Types

EMC1001
6-Lead TSOT



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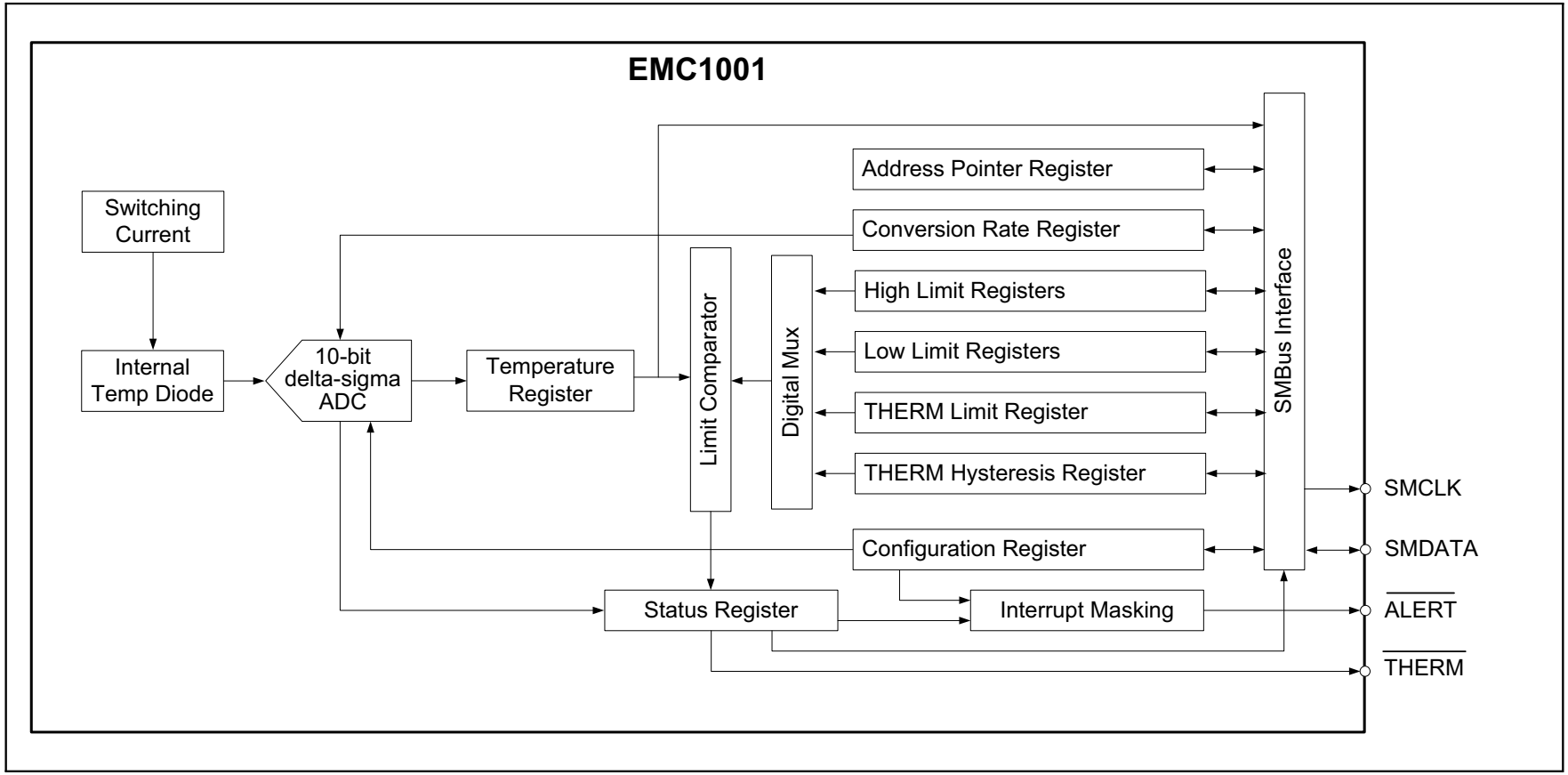
Simplified Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage VDD.....-0.3 to 5.0V
Voltage on ALERT/THERM2, SMDATA and SMCLK pins .....
.....-0.3 to 5.5V
Voltage on any other pin .....-0.3 to V_{DD}+0.3V
Lead Temperature Range .....
..... Refer to JEDEC Spec. J-STD-020
ESD Rating, All Pins (Human Body Model) 2000V

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise noted, V_{DD} = 3.0V to 3.6V, T_A= -25°C to +125°C, Typical values at T_A = +27°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Power						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Average Operating Current	I_{DD}	—	36	—	mA	0.0625 conversion/s, see Table 4-4
	I_{PD}	—	4.8	10	µA	Standby mode
Temperature Measurement						
Accuracy		—	±0.5	±1.5	°C	+40°C ≤ T_A ≤ +85°C
		—	±1	±3	°C	-25°C ≤ T_A ≤ +125°C
Resolution		—	0.25	—	°C	
Conversion Time		—	26	—	ms	
Voltage Tolerance						
Voltage at pin (ADDR/$\overline{\text{THERM}}$)	V_{TOL}	-0.3	—	3.6	V	
Voltage at pin ($\overline{\text{ALERT}}$/THERM2, SMDATA,SMCLK)	V_{TOL}	-0.3	—	5.5	V	
Digital Outputs (ADDR/THERM, ALERT/THERM2)						
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OUT} = -4 mA
High Level Leakage Current	I_{OH}	—	0.1	1	mA	V_{OUT} = V_{DD}
SMBus Interface (SMDATA,SMCLK)						
Input High Level	V_{IH}	2.0	—	—	V	
Input Low Level	V_{IL}		—	0.8	V	
Input High/Low Current	I_{IH}/I_{IL}	-1	—	1	mA	
Hysteresis		—	500	—	mV	
Input Capacitance		—	5	—	pF	
Output Low Sink Current		6		—	mA	SMDATA = 0.6V
SMBus Timing						
Clock Frequency	F_{SMB}	10	—	400	kHz	
Spike Suppression		—	—	50	ns	
Bus Free Time Start to Stop	T_{BUF}	1.3	—	—	µs	
Hold Time Start	THD:STA	0.6	—	—	µs	

Note 1: 300 ns rise time maximum is required for 400 kHz bus operation. For lower clock frequencies, the maximum rise time is (0.1/F_{SMB}) + 50 ns.

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ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise noted, V_{DD} = 3.0V to 3.6V, T_A= -25°C to +125°C, Typical values at T_A = +27°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Setup Time Start	TSU:STA	0.6	—	—	µs	
Setup Time Stop	TSU:STO	0.6	—	—	µs	
Data Hold Time	THD:DAT	0.3	—	—	µs	
Data Setup Time	TSU:DAT	100	—	—	ns	
Clock Low Period	T_{LOW}	1.3	—	—	µs	
Clock High Period	T_{HIGH}	0.6	—	—	µs	
Clock/Data Fall Time	T_F	20 + 0.1C_b	—	300	ns	
Clock/Data Rise Time	T_R	20 + 0.1C_b	—	300(1)	ns	
Capacitive Load (each bus line)	Cb	0.6	—	400	pF	

Note 1: 300 ns rise time maximum is required for 400 kHz bus operation. For lower clock frequencies, the maximum rise time is (0.1/F_{SMB}) + 50 ns.

TABLE 1-1: SMBUS ADDRESS CONFIGURATION INFORMATION

Part Number	ADDR/$\overline{\text{THERM}}$ Pull-up Resistor	SMBus Address	Package Description
EMC1001	7.5 kΩ ±5% **(Note 1, Note 2)**	100 1000b	6-Lead TSOT
	12 kΩ ±5% **(Note 2)**	100 1001b	6-Lead TSOT
	20 kΩ ±5% **(Note 2)**	011 1000b	6-Lead TSOT
	33 kΩ ±5% **(Note 2)**	011 1001b	6-Lead TSOT
EMC1001-1	7.5 kΩ ±5% **(Note 1, Note 2)**	100 1010b	6-Lead TSOT
	12 kΩ ±5% **(Note 2)**	100 1011b	6-Lead TSOT
	20 kΩ ±5% **(Note 2)**	011 1010b	6-Lead TSOT
	33 kΩ ±5% **(Note 2)**	011 1011b	6-Lead TSOT

Note 1: This value must be greater than 1 kΩ ±5% and less than or equal to 7.5 kΩ ±5%.

2: The pull-up resistor must be connected to V_{DD} (pin 1), and the total capacitance on this pin must be less than 100 pF.

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise noted, V_{DD} = 3.0V to 3.6V, T_A= -25°C to +125°C, Typical values at T_A = +27°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Ambient Temperature Range	T_A	-25	—	+125	°C	
Storage Temperature Range	T_A	-55	—	+150	°C	
Maximum Junction Temperature	T_J	-40	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 6L-TSOT	θ_{JA}	—	112	—	°C/W	

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2.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

TSOT	Pin Number	Description
1	ADDR/$\overline{\text{THERM}}$	Logic output pin that can be used to turn on/off a fan or throttle a CPU clock in the event of an overtemperature condition. This is an open-drain output. This pin is sampled following power-up and the value of the pull-up resistor determines the SMBus slave address (see Table 1-1). Total capacitance on this pin must not exceed 100 pF, and the pull-up resistor must be connected to the same supply voltage as V_{DD}.
2	GND	Ground pin
3	V_{DD}	Supply Voltage pin, 3.0V to 3.6V
4	SMCLK	SMBus Clock Input pin
5	$\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$	Logic Output pin used as interrupt, SMBus alert or as a second $\overline{\text{THERM}}$ output. This is an open-drain output.
6	SMDATA	SMBus Data Input/Output pin, open-drain output

3.0 SYSTEM MANAGEMENT BUS INTERFACE PROTOCOL

A host controller, such as an I/O controller, communicates with the EMC1001 via the two-wire serial interface named SMBus. The SMBus interface is used to read and write registers in the EMC1001, which is a slave-only device. A detailed timing diagram is shown in Figure 3-1.

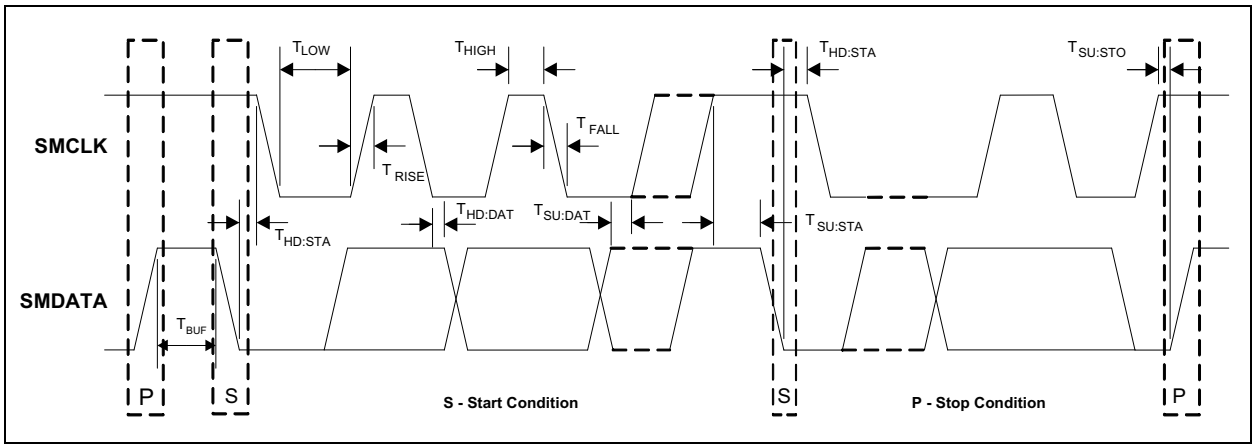

FIGURE 3-1: *System Management Bus Timing Diagram.*

The EMC1001 implements a subset of the SMBus specification and supports Write Byte, Read Byte, Send Byte, Receive Byte and Alert Response Address protocols, as shown in the following sections.

All protocols in these sections use the convention in Table 3-1.

TABLE 3-1: PROTOCOL FORMAT

Data Sent to Device	Data Sent to the Host
Data sent	Data sent

3.1 SMBus Write Byte

The Write Byte is used to write one byte of data to a specific register as shown in Table 3-2.

TABLE 3-2: WRITE BYTE PROTOCOL

START	Slave Address	WR	ACK	Command	ACK	Data	ACK	STOP
1	7	1	1	8	1	8	1	1

3.2 SMBus Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 3-3.

TABLE 3-3: READ BYTE PROTOCOL

START	Slave Address	WR	ACK	Command	ACK	START	Slave Address	RD	ACK	Data	NACK	STOP
1	7	1	1	8	1	1	7	1	1	8	1	1

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3.3 SMBus Send Byte

The Send Byte protocol is used to set the Internal Address Register to the correct Address. The Send Byte can be followed by the Receive Byte protocol (**Section 3.4 "SMBus Receive Byte"**) in order to read data from the register. The send byte protocol cannot be used to write data; if data is to be written to a register, then the Write Byte protocol must be used (see **Section 3.1 "SMBus Write Byte"**). The Send Byte protocol is shown in Table 3-4.

TABLE 3-4: SEND BYTE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	STOP
1	7	1	1	8	1	1

3.4 SMBus Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g., set via Send Byte). This is used for consecutive reads of the same register as shown in Table 3-5.

TABLE 3-5: RECEIVE BYTE PROTOCOL

START	Slave Address	RD	ACK	Register Data	NACK	STOP
1	7	1	1	8	1	1

3.5 Alert Response Address

The $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ output can be used as an SMBALERT# as described in **Section 4.3 "ALERT/THERM2 Output"** The Alert Response Address is polled by the Host whenever it detects an SMBALERT#, i.e. when the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin is asserted. The EMC1001 will acknowledge the Alert Response Address and respond with its device address as shown in Table 3-6.

TABLE 3-6: MODIFIED SMBUS RECEIVE BYTE PROTOCOL RESPONSE TO ARA

START	Alert Response Address	RD	ACK	EMC1001 Slave Address	NACK	STOP
1	7	1	1	8	1	1

3.6 SMBus Addresses

The EMC1001 is available in two versions (EMC1001 and EMC1001-1), each of which has four 7-bit slave addresses that are enabled based on the pull-up resistor on the ADDR/$\overline{\text{THERM}}$ pin. The value of this pull-up resistor determines the slave address per Table 1-1. Attempting to communicate with the EMC1001 SMBus interface with an invalid slave address or invalid protocol results in no response from the device and does not affect its register contents.

The EMC1001 supports stretching of the SMCLK signal by other devices on the SMBus but will not perform this operation itself. The EMC1001 has an SMBus timeout feature. Bit 7 of the SMBus Timeout Enable register enables this function when set to 1 (the default setting is 0). When this feature is enabled, the SMBus will timeout after approximately 25 ms of inactivity.

4.0 PRODUCT DESCRIPTION

The EMC1001 is an SMBus temperature sensor that monitors a single temperature zone. Thermal management is performed in cooperation with a host device. The host reads the temperature data from the EMC1001 and takes appropriate action such as controlling fan speed or processor clock frequency. The EMC1001 has programmable temperature-limit registers that define a safe operating window. After the host has configured the temperature limits, the EMC1001 can operate as a free-running independent watchdog to warn the host of temperature hot-spots, without requiring the host to poll the device. The ADDR/THERM output can be used to control a fan without host intervention.

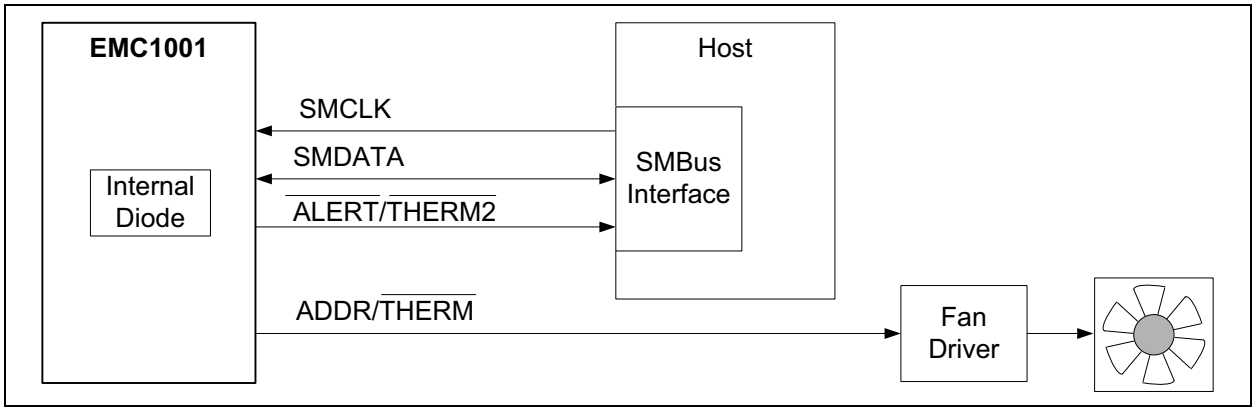

FIGURE 4-1: *Controlling a Fan without Host Intervention.*

The EMC1001 has two basic modes of operation:

- **Run Mode:** In this mode, the EMC1001 continuously converts temperature data and updates its registers. The rate of temperature conversion is configured as shown in **Section 4.9 "Conversion Rate Register"**.
- **Standby Mode:** In this mode, the EMC1001 is placed in Standby to conserve power, as described in **Section 4.5 "Standby Mode"**.

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4.1 Temperature Monitors

Thermal diode temperature measurements are based on the change in forward bias voltage (ΔV_{BE}) of a diode when operated at two different currents:

EQUATION 4-1:

$$\Delta V_{BE} = V_{BE_HIGH} - V_{BE_LOW} = \frac{\eta k T}{q} ln\left(\frac{I_{HIGH}}{I_{LOW}}\right)$$

Where:

k = Boltzmann's Constant
T = Absolute Temperature in Kelvin
q = Electron Charge
η = Diode Ideality Factor

The change in ΔV_{BE} voltage is proportional to absolute temperature T.

Figure 4-2 shows a detailed block diagram of the temperature measurement circuit. The EMC1001 incorporates switched capacitor technology that integrates the temperature diode ΔV_{BE} from different bias currents. The negative terminal (DN) for the temperature diode is internally biased with a forward diode voltage referenced to ground.

The advantages of this architecture over Nyquist rate direct-conversion ADC (FLASH) or successive approximation register (SAR) converters are superb linearity and inherent noise immunity. The linearity can be directly attributed to the delta-sigma ADC single-bit comparator, while the noise immunity is achieved by the ~20 ms integration time which translates to 50 Hz input noise bandwidth.

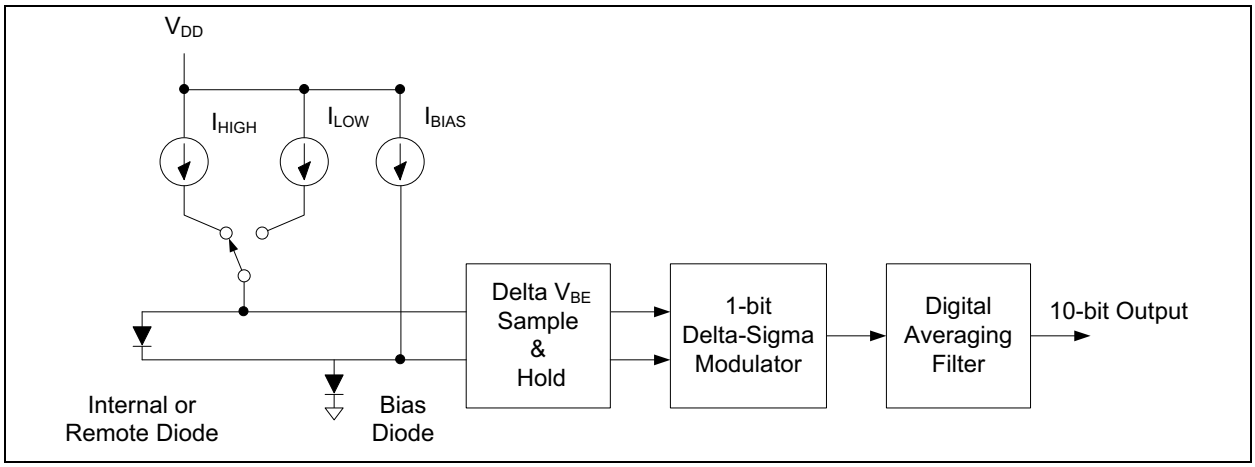

FIGURE 4-2: *Detailed Block Diagram.*

4.2 Temperature Measurement Results and Data

The 10-bit temperature measurement results are stored in temperature value registers. Table 4-1 shows the two's complement temperature data format with an LSB equivalent to 0.25°C.

TABLE 4-1: TEMPERATURE DATA FORMAT

Temperature	Valid Range -40°C to +125°C
	Two's Complement
-0.25°C	1111 1111 11 (1)
0.0°C	0000 0000 00

Note 1: Temperature measurement returns 1100 0000 00 for all temperatures ≤-64.00°C.

2: Temperature measurement returns 0111 1111 11 for all temperatures ≥+127.75°C.

TABLE 4-1: TEMPERATURE DATA FORMAT (CONTINUED)

Temperature	Valid Range -40°C to +125°C
	Two's Complement
+0.25°C	0000 0000 01
+0.50°C	0000 0000 10
+0.75°C	0000 0000 11
+1°C	0000 0001 00
...	...
+125°C	0111 1101 00 (2)

Note 1: Temperature measurement returns 1100 0000 00 for all temperatures ≤-64.00°C.

2: Temperature measurement returns 0111 1111 11 for all temperatures ≥+127.75°C.

The eight most significant bits are stored in the Temperature Value High Byte register and the two least significant bits stored in the Temperature Value Low Byte register as outlined in Table 4-2. The six LSB positions of the Temperature Value Low Byte register always read zero. In Table 4-2, the upper case “B” shows the bit position of a 16-bit word created by concatenating the High Byte and Low Byte, and the lower case “b” shows the bit position in the 10-bit value.

TABLE 4-2: BIT POSITION OF TWO BYTE VALUES

High Byte								Low Byte							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	0	0	0	0	0	0

4.3 $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ Output

The $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ output asserts if an out-of-limit measurement is detected ($T_A \leq$ low limit or $T_A >$ high limit). The $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin is an open-drain output and requires a pull-up resistor to V_{DD}. The $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin can be used as an SMBALERT#, or may be configured as a second $\overline{\text{THERM}}$ output.

As described in the SMBus specification, an SMBus slave may inform the SMBus master that it wants to talk by asserting the SMBALERT# signal. One or more $\overline{\text{ALERT}}$ outputs can be hardwired together as a wired-OR bus to a common input.

The $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin resets when the EMC1001 responds to an alert response address (ARA = `0001 100`) sent by the host, and if the out-of-limit condition no longer exists, but it does not reset if the error condition remains. The $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin can be masked so that it will not assert in the event of an out-of-limit temperature measurement, except when it is configured as a second $\overline{\text{THERM}}$ pin.

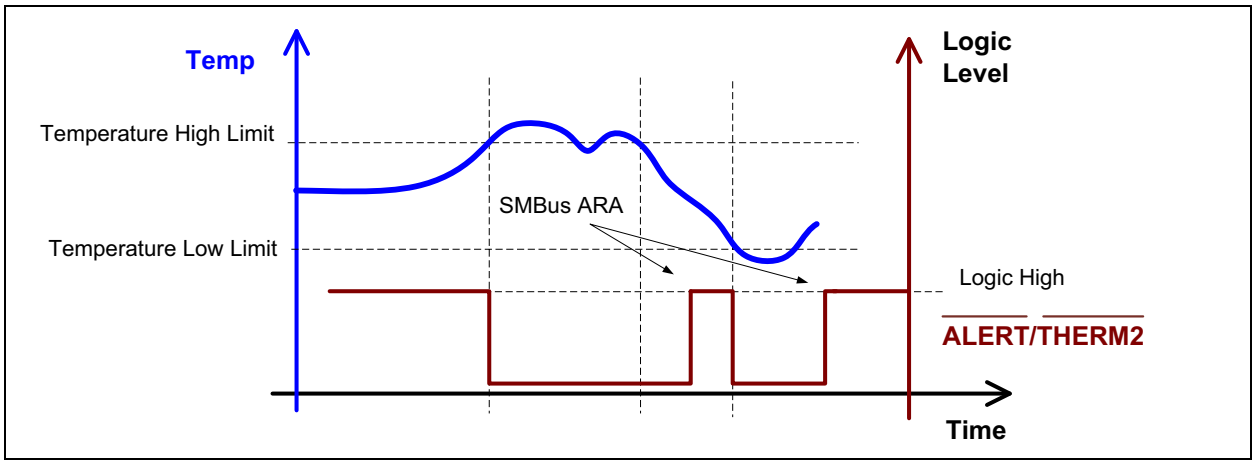

FIGURE 4-3: *ALERT Response to Temperature Limits Exceeded.*

The $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin can be configured as a second $\overline{\text{THERM}}$ pin that asserts when the temperature measurement exceeds the Temperature High Limit value. The output will not de-assert until the temperature drops below the Temperature High Limit, minus the THERM Hysteresis value.

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4.4 ADDR/$\overline{\text{THERM}}$ Output

The ADDR/$\overline{\text{THERM}}$ output asserts if the temperature measurement exceeds the programmable THERM limit. It can be used to drive a fan or other failsafe devices. The ADDR/$\overline{\text{THERM}}$ pin is open drain and requires a pull-up resistor to V_{DD}. The value of this pull-up resistor determines the slave address per Table 1-1. The ADDR/$\overline{\text{THERM}}$ pin cannot be masked.

When the ADDR/$\overline{\text{THERM}}$ pin is asserted, it will not de-assert until the temperature drops below the THERM limit, minus the THERM Hysteresis value.

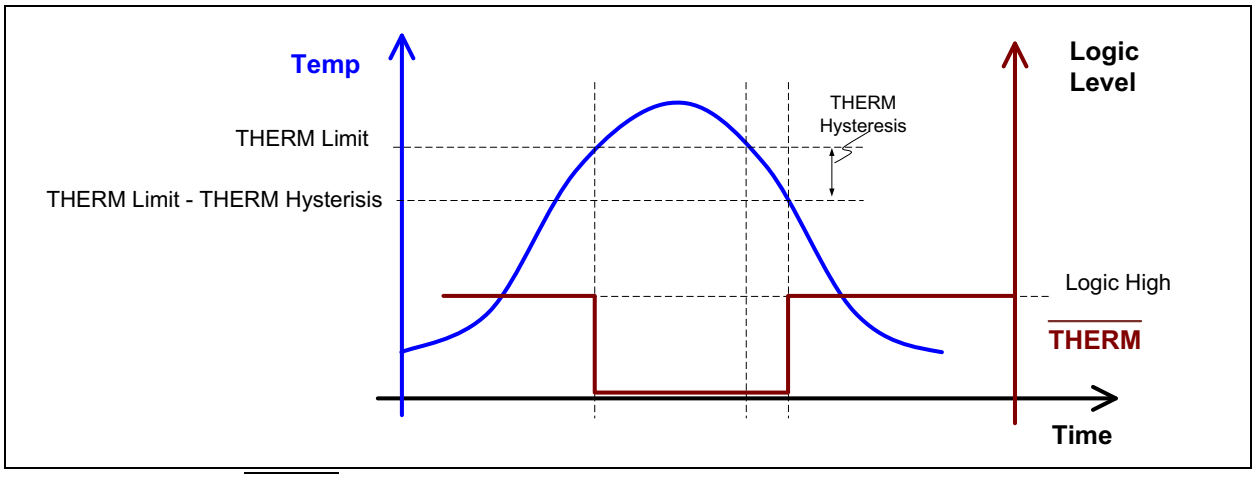

FIGURE 4-4: *$\overline{\text{THERM}}$ Response to THERM Limit Exceeded.*

4.5 Standby Mode

The EMC1001 can be set to Standby mode (low power) by setting a bit in the Configuration Register as described in **Section 4.8 "Configuration Register"**. This shuts down all internal analog functions while the SMBus remains enabled. When the EMC1001 is in Standby mode, a `One-Shot` command measurement can be initiated. The user may also write new values to the limit registers described in **Section 4.10 "Limit Registers"** while in Standby. If the previously stored temperature is outside any of the new limits, the ALERT/$\overline{\text{THERM2}}$ output will respond as described in **Section 4.3 "ALERT/THERM2 Output"** and the ADDR/$\overline{\text{THERM}}$ output will respond as described in **Section 4.4 "ADDR/THERM Output"**.

4.6 Register Allocation

The registers shown in Table 4-3 are accessible through the SMBus.

TABLE 4-3: REGISTER MAP

Register Address (HEX)	Read/Write	Register Name	Power-On Default
00	R	Temperature Value High Byte	0000 0000
01	RC	Status	undefined
02	R	Temperature Value Low Byte	0000 0000
03	R/W	Configuration	0000 0000
04	R/W	Conversion Rate	0000 0100
05	R/W	Temperature High Limit High Byte	0101 0101 (+85°C)
06	R/W	Temperature High Limit Low Byte	0000 0000
07	R/W	Temperature Low Limit High Byte	0000 0000 (0°C)
08	R/W	Temperature Low Limit Low Byte	0000 0000
0F	W	One-Shot	N/A
20	R/W	THERM Limit	0101 0101 (+85°C)
21	R/W	THERM Hysteresis	0000 1010 (+10°C)
22	R/W	SMBus Timeout Enable	1000 0000
FD	R	Product ID Register	0000 0000 (**EMC1001**)
			0000 0001 (**EMC1001-1**)
FE	R	Manufacture ID	0101 1101
FF	R	Revision Number	0000 0011 **(Note 1)**

Note 1: The revision number may change. Please obtain the latest version of this document from the Microchip web site (www.microchip.com).

At device power-up, the default values are stored in all registers. A Power-on Reset (POR) is initiated when power is first applied to the part and the V_{DD} supply exceeds the POR threshold. Reads of undefined registers will return 00h, and writes to undefined registers will be ignored.

The EMC1001 uses an interlock mechanism that locks the low-byte value when the high byte register is read. This prevents updates to the low byte register between high-byte and low-byte reads. This interlock mechanism requires that the high byte register always be read prior to reading the low byte register.

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4.7 Status Register

The Status register is a read-only register that stores the operational status of the part. When either T_{LOW} or T_{HIGH} are set ($T_A \leq$ low limit or $T_A >$ high limit) and the $\overline{ALERT}/\overline{THERM2}$ pin is not masked, the $\overline{ALERT}/\overline{THERM2}$ pin will assert. See **Section 4.3 "ALERT/THERM2 Output"** for more details on the ALERT function.

REGISTER 4-1: STATUS REGISTER

RC-0	RC-0	RC-0	U-0	U-0	U-0	U-0	RC-0
BUSY	THIGH	TLOW	—	—	—	—	THRM
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
RC = Read then Clear			

bit 7 **BUSY:** ADC is busy converting a value
- 1 = ADC is converting
- 0 = ADC is not converting

bit 6 **THIGH:** Temperature High Limit bit
- 1 = Temperature High Limit is exceeded
- 0 = Temperature High Limit is within the limits

bit 5 **TLOW:** Temperature Low Limit bit
- 1 = Temperature Low Limit is exceeded
- 0 = Temperature Low Limit is within the limits

bit 3-1 **Reserved:** Unimplemented bit, read as '0'.

bit 0 **THRM:** THERM limit bit
- 1 = THERM limit is exceeded, ADDR/$\overline{THERM}$ output will be asserted
- 0 = THERM limit is in the limits

Each bit is cleared individually when the Status register is read, provided that the error condition for that bit no longer exists. The $\overline{ALERT}/\overline{THERM2}$ output is latched and will not be reset until the host has responded with an alert response address (ARA = 0001 100). The $\overline{ALERT}/\overline{THERM2}$ output will not reset if the Status register has not been cleared.

4.8 Configuration Register

The Configuration register controls the functionality of the temperature measurements.

REGISTER 4-2: CONFIGURATION REGISTER

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
MASK1	RUN/STOP	ALERT/THERM2	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **MASK1:** Masks the $\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$ signal (Note 1).
- 1 = $\overline{\text{ALERT}}$ is disabled; any out-of-limit condition will not assert the signaled pin
- 0 = $\overline{\text{ALERT}}$ is enabled; any out-of-limit condition will assert the signaled pin (**default**)

bit 6 **RUN/STOP:** Initiates ADC conversions
- 1 = Standby mode, thus reducing supply current significantly, though the SMBus will still be active (Note 2)
- 0 = Active mode (continuously running); the ADC will convert temperatures in a continuous mode (**default**)

bit 5 **ALERT/THERM2:** sets the $\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$ pin to act as either an SMBALERT# signal or as the $\overline{\text{THERM2}}$ signal.
- 1 = the $\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$ pin acts as the $\overline{\text{THERM2}}$ signal and Bit 7 is ignored
- 0 = the $\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$ pin acts as the $\overline{\text{ALERT}}$ (SMBALERT#) signal (**default**)

bit 3-0 **Reserved:** Unimplemented bit, read as '0'.

Note 1: This bit is ignored if the $\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$ pin is configured as $\overline{\text{THERM2}}$ signal by Bit 5.

2: If this bit is high and the One-shot register is written to, the ADC will execute a temperature measurement and then return to Standby mode.

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4.9 Conversion Rate Register

The Conversion Rate register determines how many times the temperature value will be updated per second. The lowest 4 bits configure a programmable delay that waits between consecutive conversion cycles to obtain the desired conversion rate. Table 4-4 shows the conversion rate and the associated quiescent current.

TABLE 4-4: CONVERSION RATES

Conversion Rate Value	Conversions/ Second	Typical Quiescent Current (µA)
00h	0.0625	36
01h	0.125	37
02h	0.25	38
03h	0.5	40
04h (**default**)	1	44
05h	2	54
06h	4	71
07h	8	109
08h	16	182
09h	32	326
0Ah to FFh	Reserved	—

4.10 Limit Registers

The user can configure high and low temperature limits and an independent THERM limit. The temperature high limit (T_H) is a 10-bit value that is set by the Temperature High Limit High Byte register and the Temperature High Limit Low Byte register. The Temperature High Limit Low Byte register contains the two least significant bits, as shown in Table 4-2. The two least significant bits are stored in the upper two bits of the register, and the six LSB positions of this register always read zero.

The temperature low limit (T_L) is a 10-bit value that is set by the Temperature Low Limit High Byte register and the Temperature Low Limit Low Byte register, as shown in Table 4-2.

The limits are compared to the temperature measurement results (T_{INT}) and have been exceeded if ($T_{INT} \leq T_L$ or $T_{INT} > T_H$). If either limit is exceeded then the appropriate bit is set high in the Status register and the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ output will respond as described in **Section 4.3 "ALERT/THERM2 Output"**.

The THERM limit (T_{TH}) is a single byte value set by the THERM Limit register. Exceeding the THERM limit asserts the ADDR/$\overline{\text{THERM}}$ signal as described in **Section 4.4 "ADDR/THERM Output"**. When the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin is configured as $\overline{\text{THERM2}}$, then exceeding the high limit asserts this pin.

4.11 THERM Hysteresis Register

The THERM Hysteresis register holds a hysteresis value that determines the de-assertion of $\overline{\text{THERM}}$, as shown in Figure 4-4. It defaults to 10°C and can be set by the user at any time after power-up. When the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin is configured as $\overline{\text{THERM2}}$, the hysteresis value also impacts the de-assertion of $\overline{\text{THERM2}}$.

4.12 One-Shot Register

Writing to the One-shot register while in Standby mode initiates a conversion and comparison cycle. The EMC1001 will execute a temperature measurement, compare the data to the limit registers and return to the Standby mode. A write to the One-shot register will be ignored if it occurs while the EMC1001 is in Run mode.

4.13 SMBus Timeout Enable

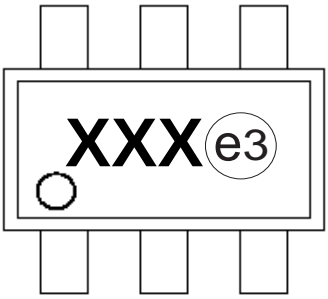
The EMC1001 has an SMBus timeout feature. Bit 7 of the SMBus Timeout Enable register enables this function when set to `1` (the default setting is `0`). When this feature is enabled, the SMBus will timeout after approximately 25 ms of inactivity.

5.0 PACKAGING INFORMATION

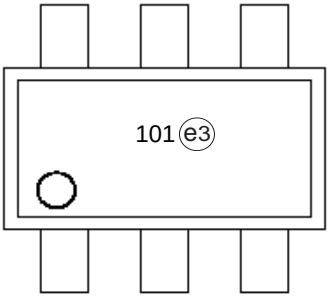
5.1 Package Marking Information

6-Lead TSOT

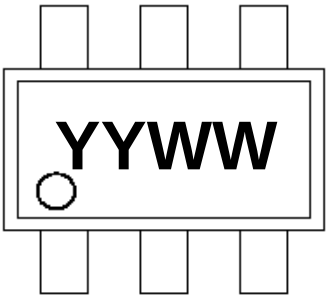
Top Marking

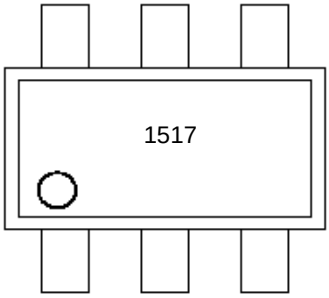


Example



Bottom Marking





Legend:	X	Device version
	NNNNNNN	Last 7 digits of Lot Number
	R	Revision
	<COO>	Country of origin
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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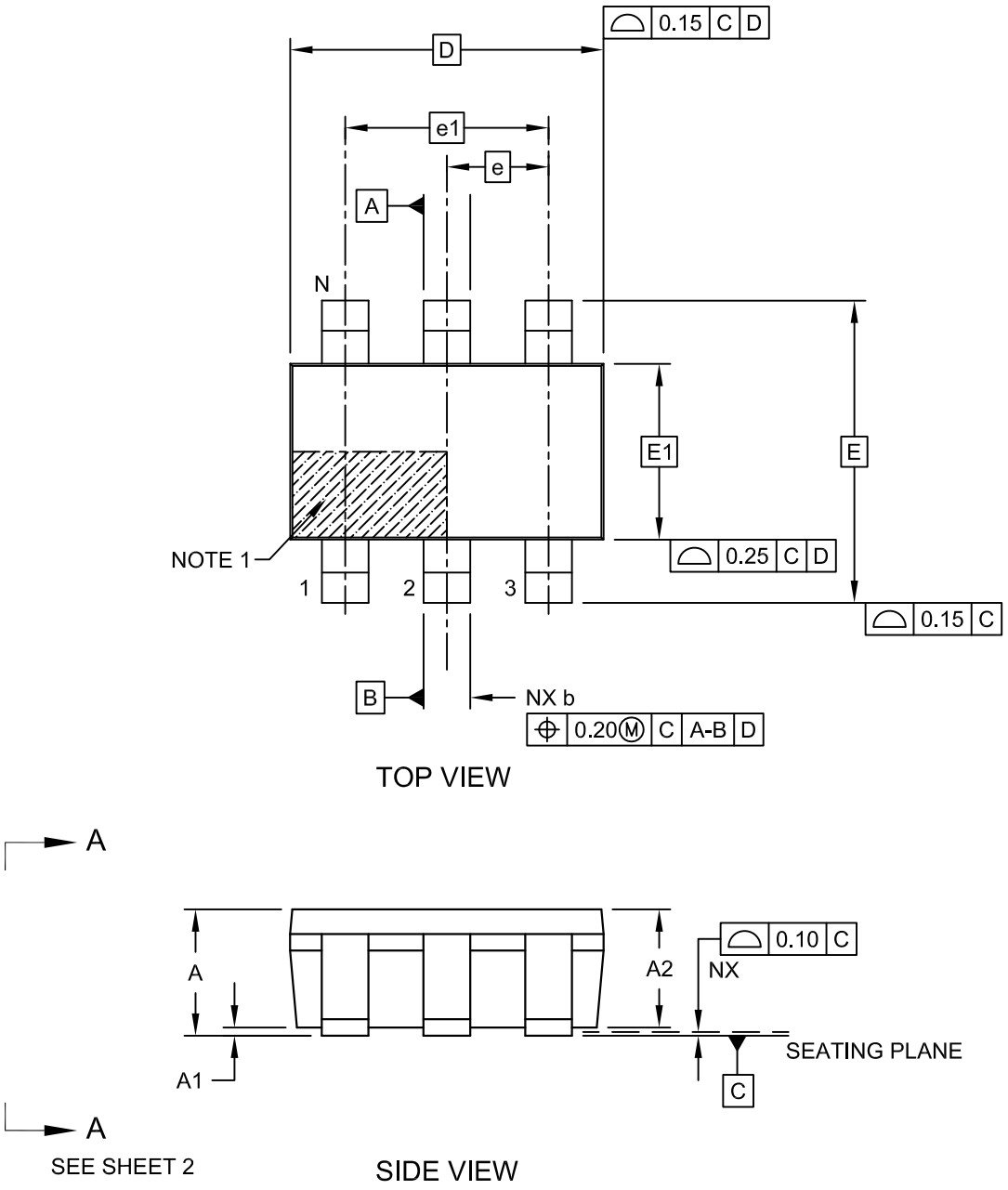
6-Lead Thin Small Outline Transistor (OS) [TSOT]

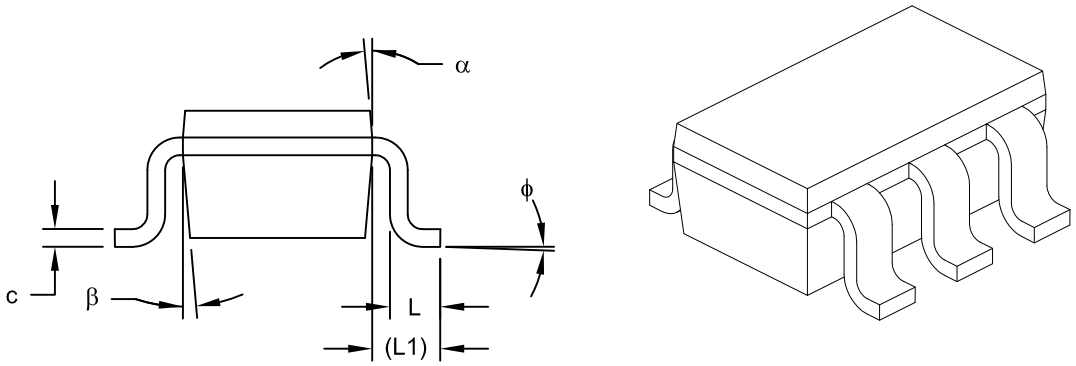
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-141A Sheet 1 of 2

6-Lead Thin Small Outline Transistor (OS) [TSOT]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A

	Units	MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Number of Leads	N		6	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.70	0.90	1.00
Standoff	A1	0.00	-	0.10
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	0.45	0.60
Footprint	L1		0.60 REF	
Foot Angle	ϕ	0°	4°	8°
Lead Thickness	c	0.08	-	0.20
Lead Width	θ	0.30	-	0.50
Mold Draft Angle Top	α	4°	10°	12°
Mold Draft Angle Botton	β	4°	10°	12°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-141A Sheet 2 of 2

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APPENDIX A: REVISION HISTORY

Revision A (May 2015)

- Original Release of this Document.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	[-X](1)
Device	Package	Tape and Reel Option

Device:	EMC1001:	Tiny SMBus Temperature Sensor
	EMC1001-1:	Tiny SMBus Temperature Sensor with Alternate SMBus Address (see Table 1-1)
Package:	AFZQ=	6-pin, Thin Small Outline Transistor Package, Green, Lead Free
Tape and Reel Option:	Blank =	Standard packaging (tube or tray)
	TR =	Tape and Reel(1)

Examples:

a) EMC1001-AFZQ-TR: 6-pin TSOT package, Tape and Reel

b) EMC1001-1-AFZQ-TR: Alternate SMBus Address, 6-pin TSOT package, Tape and Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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