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## USER GUIDE FOR IR3629 EVALUATION BOARD

( $V_{in}=12V$ ,  $V_o=1.8V$ ,  $I_o=20A$ )

### DESCRIPTION

The IR3629 is a synchronous buck controller, providing a compact, high performance and flexible solution in a small 3mmx4mm MLPD package.

Key features offered by the IR3629 include programmable soft-start ramp, precision 0.6V reference voltage, thermal protection, fixed 600kHz switching frequency requiring no external component, input under-voltage lockout for proper start-up, and pre-bias start-up.

An output over-current protection function is implemented by sensing the voltage developed across the on-resistance of the synchronous rectifier MOSFET for optimum cost and performance.

This user guide contains the schematic and bill of materials for the IR3629 evaluation board. The guide describes operation and use of the evaluation board itself. Detailed application information for the IR3629 integrated circuit is available in the IR3629 data sheet.

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### BOARD FEATURES

- $V_{in} = +12V$  (13.2V Max)
- $V_{out} = +1.8V$  @ 0-20A
- IRF6712 as Controller MOSFET
- IRF6715 as Synchronous MOSFET
- $L = 0.36\mu H$
- $C_{in}=33\mu F$  (SP cap) + 2x10 $\mu F$  (ceramic 1206)
- $C_{out}=6x22\mu F$ (ceramic 1206)
- Optional external supply connection for  $V_c$
- Optional Power-good output connection

## CONNECTIONS and OPERATING INSTRUCTIONS

A well regulated +12V input supply should be connected to VIN+ and VIN-. A maximum of 20A load can be connected to VOUT+ and VOUT-. The connection diagram is shown in Fig. 1

IR3629 demo board can also be powered by two separate power supplies, one is the input voltage ( $V_{in}$ ) between VIN+ and VIN-, the other is bias voltage ( $V_{cc}$ ) between Vc-ext and PGND. In this case, a well regulated 5V~12V power supply should be connected to Vc-ext and PGND and R14 should be removed.

Inputs and outputs of the board are listed in Table I.

**Table I. Connections**

Connection	Signal Name
VIN+	$V_{in}$ (+12V)
VIN-	Ground of $V_{in}$
Vc-ext	Optional Vcc input
PGND	Ground for optional Vcc input
VOUT-	Ground of $V_{out}$
VOUT+	$V_{out}$ (+1.8V)
GND	Bias Voltage Ground

## LAYOUT

The PCB is a 6-layer board. All of layers are 2 Oz. copper. Power supply decoupling capacitors, the charge-pump capacitor and feedback components are located close to the IR3629. The feedback resistors are connected to the output voltage at the point of regulation and are located close to the IC.

The input and output energy storage capacitors and the power inductor are located on bottom side of the board, to improve efficiency, the circuit board is designed to minimize the length of the on-board power ground current path.

## IR3629 Demo Board



Fig. 1 Connection diagram of the evaluation board for IR3629 (Top view)

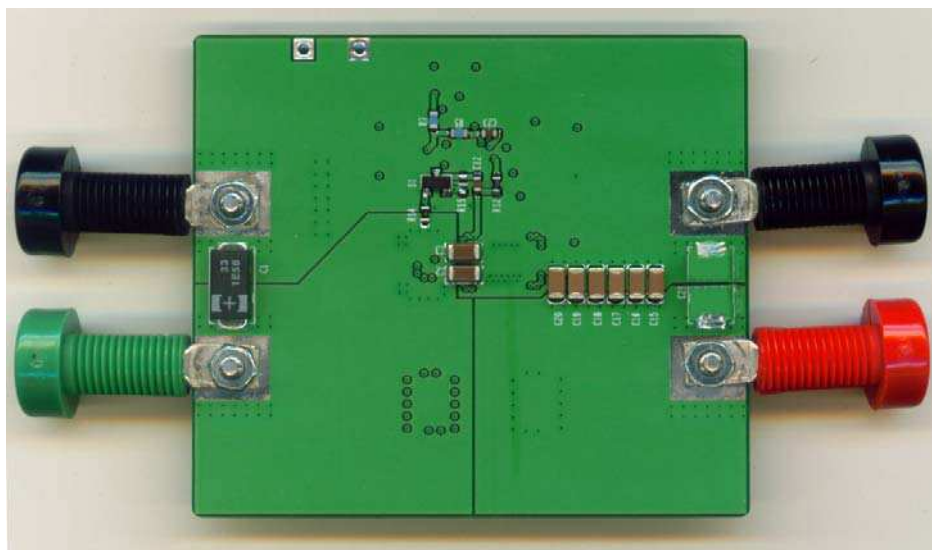
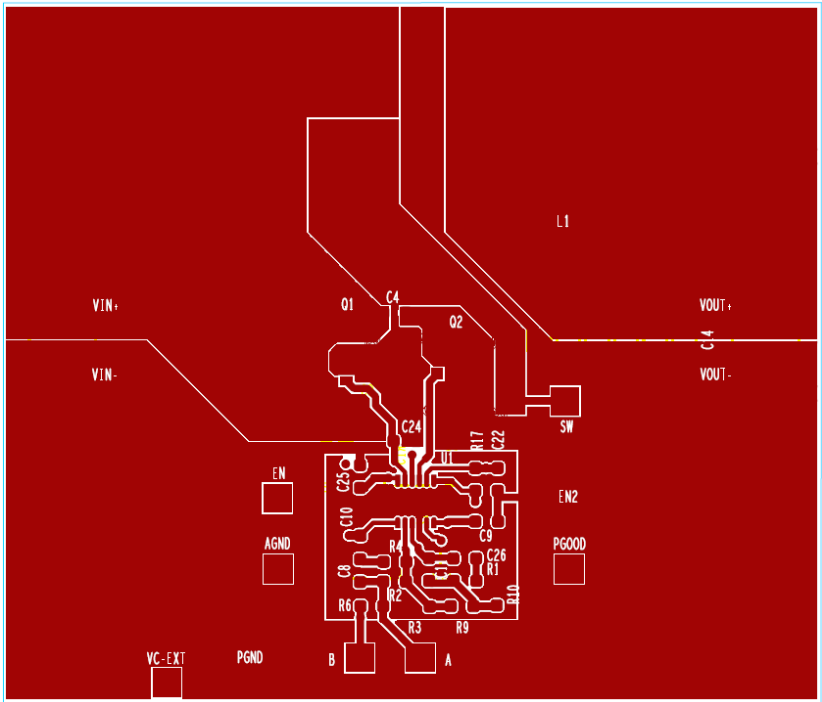
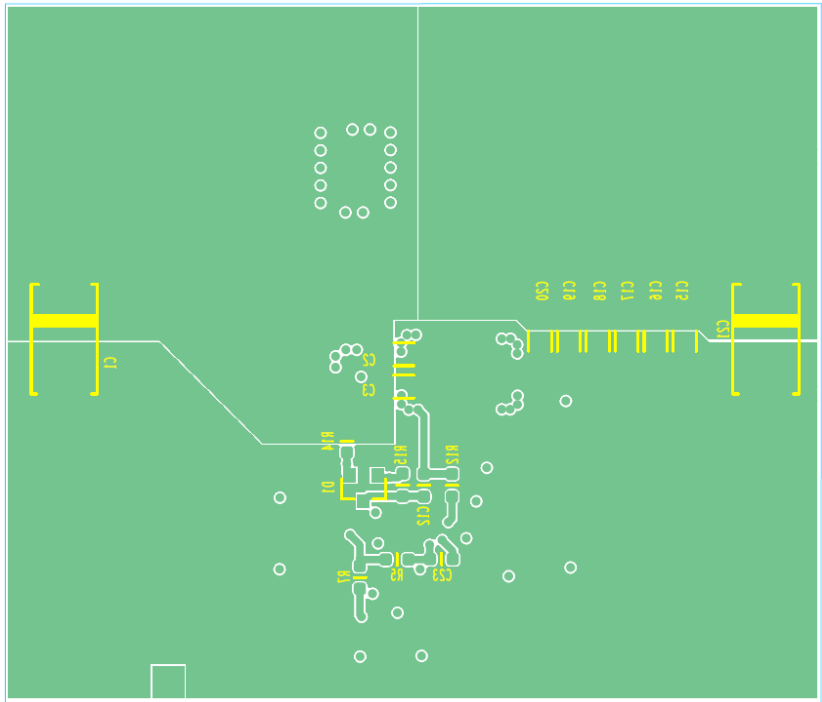


Fig. 2 Bottom view of the evaluation board for IR3629

IR3629 PCB Layers

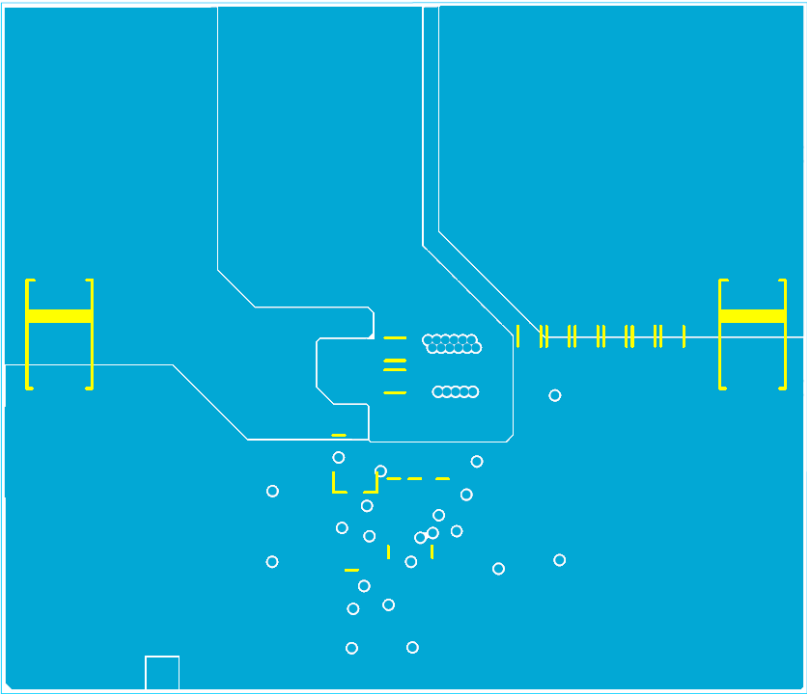
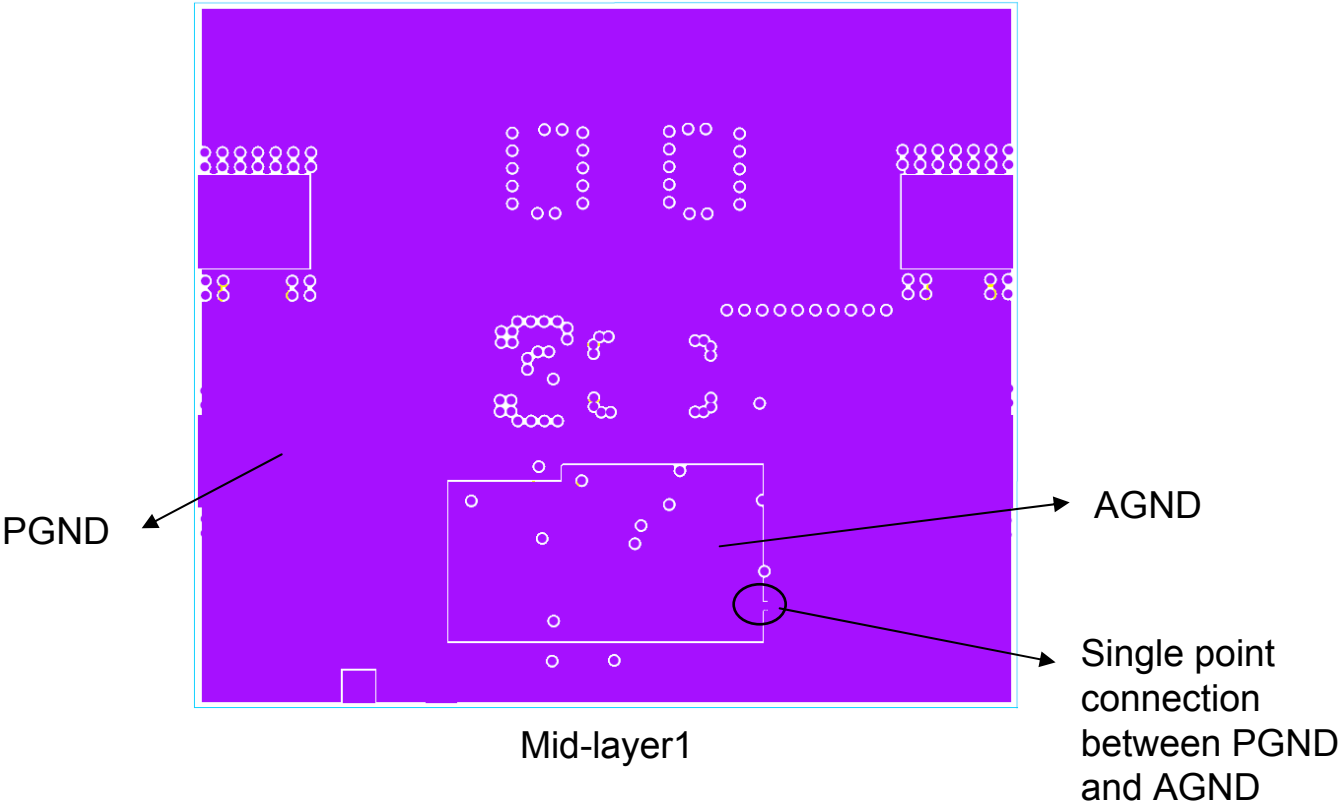


Top Layer



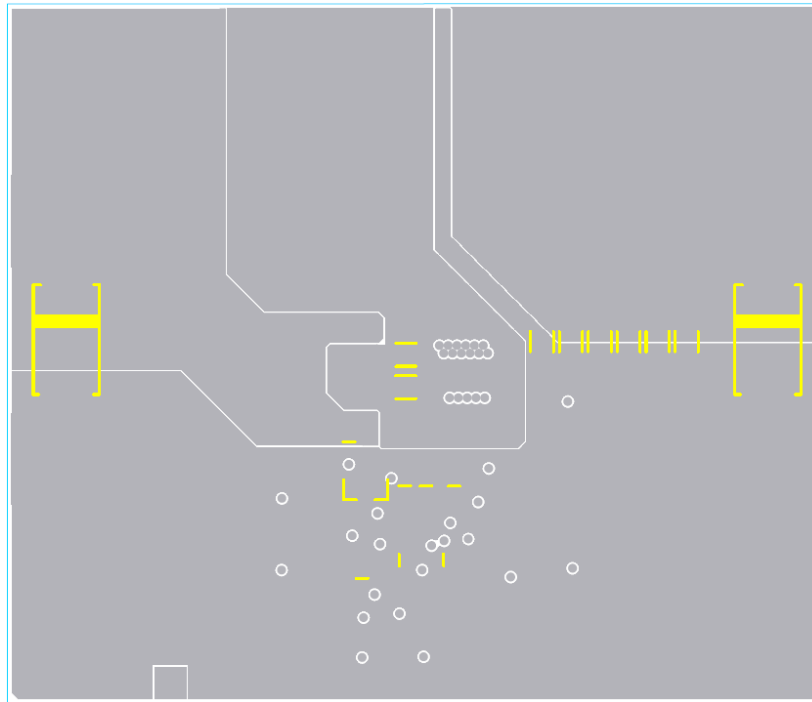
Bottom Layer

IR3629 PCB Layers

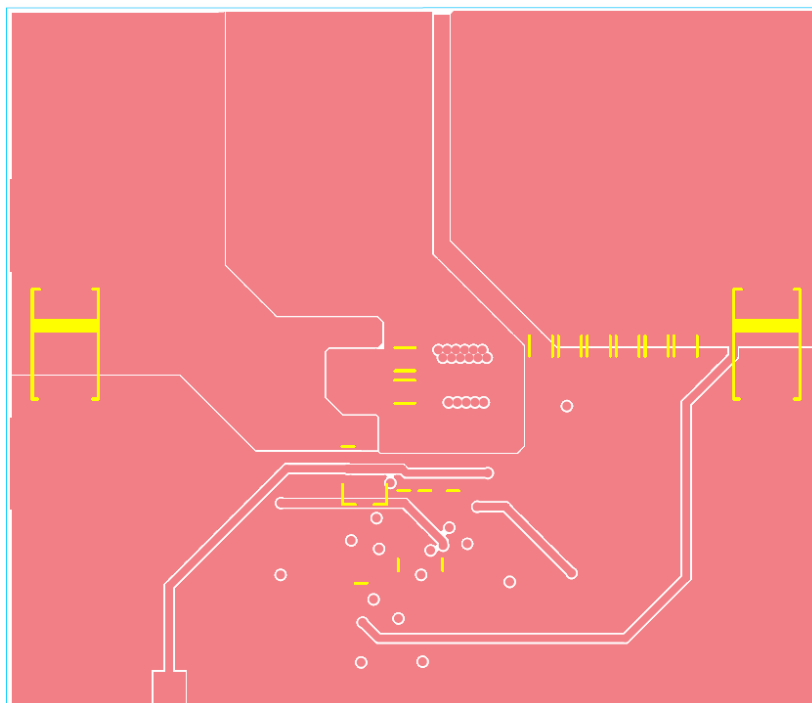


Mid-layer2

## IR3629 PCB Layers



Mid-layer3



Mid-layer4

## IR3629 Demo Board Schematic

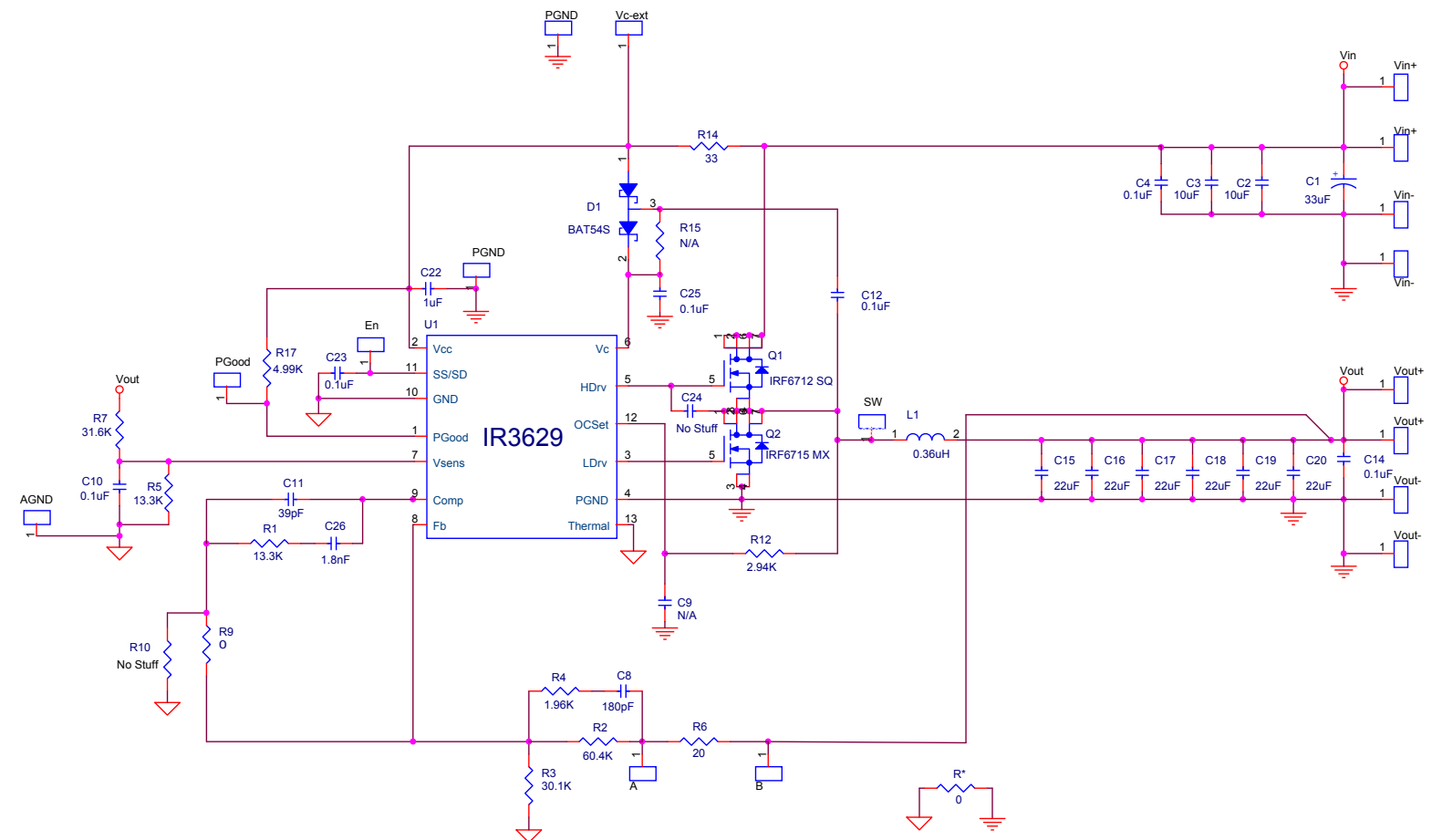


Fig. 3 Schematic of the IR3629 evaluation board with 12Vin and 1.8V output voltage

## BILL OF MATERIALS

Item	Quantity	Reference	Value	Description	Size	Manufacturer	Part Number
1	1	C1	33uF	POSCAP, 25V, 20%	-	Sanyo	25TQC33M
2	2	C2,C3	10uF	Ceramic, 25V, X7R, 10%	1206	Murata	GRM31CR61C106KA88
3	6	C4,C10,C12 C14,C23, C25	0.1uF	Ceramic, 25V, X7R, 10%	603	TDK	C1608X7R1H104K
4	1	C8	180pF	Ceramic, 50V, C0G, 5%	603	Murata	GRM1885C1H181JA01D
5	1	C11	39pF	Ceramic, 50V, C0G, 5%	603	Murata	GRM1885C1H390JA01D
6	6	C15,C16, C17,C18, C19,C20	22uF	Ceramic, 6.3V, X5R, 20%	1206	Panasonic	ECJDV50J226M
7	1	C22	1uF	Ceramic, 16V, X5R, 10%	603	TDK	C1608X5R1C105K
8	1	C26	1.8nF	Ceramic, 50V, C0G, 5%	603	Murata	GRM1885C1H182JA01D
9	1	D1	BAT54S	Dual Schottky Diode	SOT-23	Vishay	BAT54S
10	1	L1	0.36uH	1.1mOhm	-	Panasonic	ETQP4LR36WFC
11	1	Q1	IRF6712 SQ	NFET, 25V, 3.8mOhm, 12nC	DirectFET SQ	IR	IRF6712SPbF
12	1	Q2	IRF6715 MX	NFET, 25V, 1.3mOhm, 40nC	DirectFET MX	IR	IRF6715MPbF
13	1	R9	0	Thick film, 1%, 1/10W	603	any	any
14	1	R1	13.3K	Thick film, 1%, 1/10W	603	any	any
15	1	R2	60.4K	Thick film, 1%, 1/10W	603	any	any
16	1	R7	31.6K	Thick film, 1%, 1/10W	603	any	any
17	1	R3	30.1K	Thick film, 1%, 1/10W	603	any	any
18	1	R4	1.96K	Thick film, 1%, 1/10W	603	any	any
19	1	R5	13.3K	Thick film, 1%, 1/10W	603	any	any
20	1	R6	20	Thick film, 1%, 1/10W	603	any	any
21	1	R12	2.94K	Thick film, 1%, 1/10W	603	any	any
22	1	R17	4.99K	Thick film, 1%, 1/10W	603	any	any



## BILL OF MATERIALS (cont.)

Item	Quantity	Reference	Value	Description	Size	Manufacturer	Part Number
23	1	R14	33	Thick film, 1%, 1/4W	1206	any	any
24	1	U1	IR3629	PWM Controller	MLPD 3x4	IR	IR3629MPbF
25	2	C9, C24	No Stuff		603		
26	1	C21	No Stuff		-		
27	2	R10,R15	No Stuff		603		
28	2	-	-	Banana Jack, Insulated, Solder Terminal, Black	-	Johnson Components	105-0853-001
29	1	-	-	Banana Jack, Insulated, Solder Terminal, Red	-	Johnson Components	105-0852-001
30	1	-	-	Banana Jack, Insulated, Solder Terminal, Green	-	Johnson Components	105-0854-001

## TRACKING OPERATING PERFORMANCE

$V_{in}=12.0V$ ,  $V_o=1.8V$ ,  $F_s=600kHz$ , Room Temperature, No Air Flow

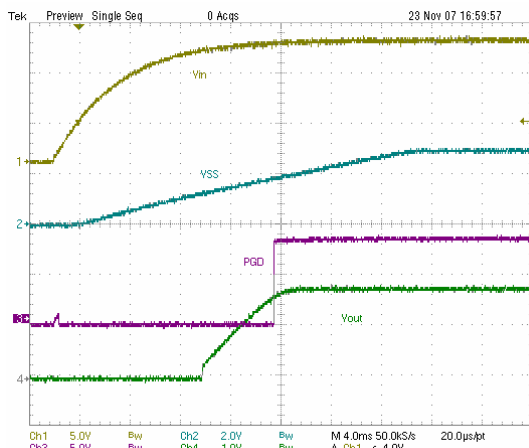


Fig. 4 Start Up at 20A

Ch1:Vin, Ch2:Vss, Ch3:PGood, Ch4:Vout

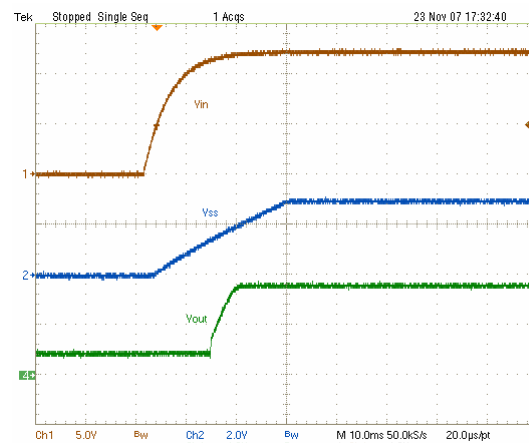


Fig. 5 Prebias Start Up

Ch1:Vin, Ch2:Vss, Ch4:Vout



Fig. 6 Output Voltage Ripple at 20A Load

Ch1:Vout, Ch3:SW

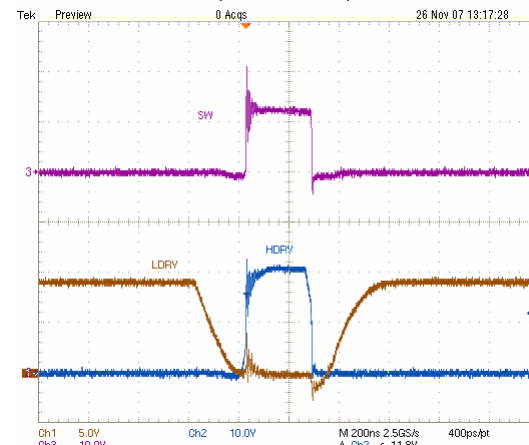


Fig. 7 Gate Signals at 20A Load

Ch1:LDRV, Ch2:HDRV, Ch3:SW

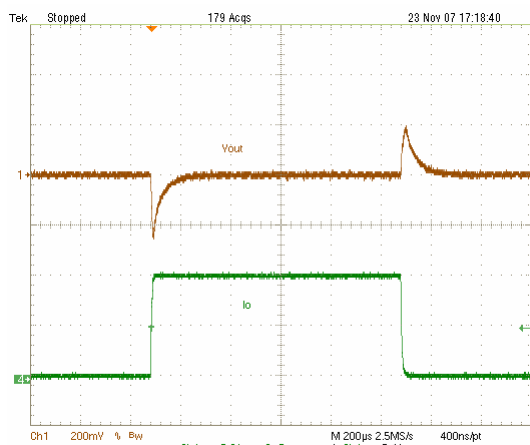


Fig. 8 Transient Response

Ch1:Vout, Ch2:Io(0-10A)



Fig. 9 Shorted Hiccup Condition Recovery

Ch2:Vout, Ch3:Vss, Ch4:Io

**TYPICAL OPERATING PERFORMANCE**  
**Vin=12.0V, Vo=1.8V, Io=0-20A, Fs=600kHz, Air Flow=200LFM**

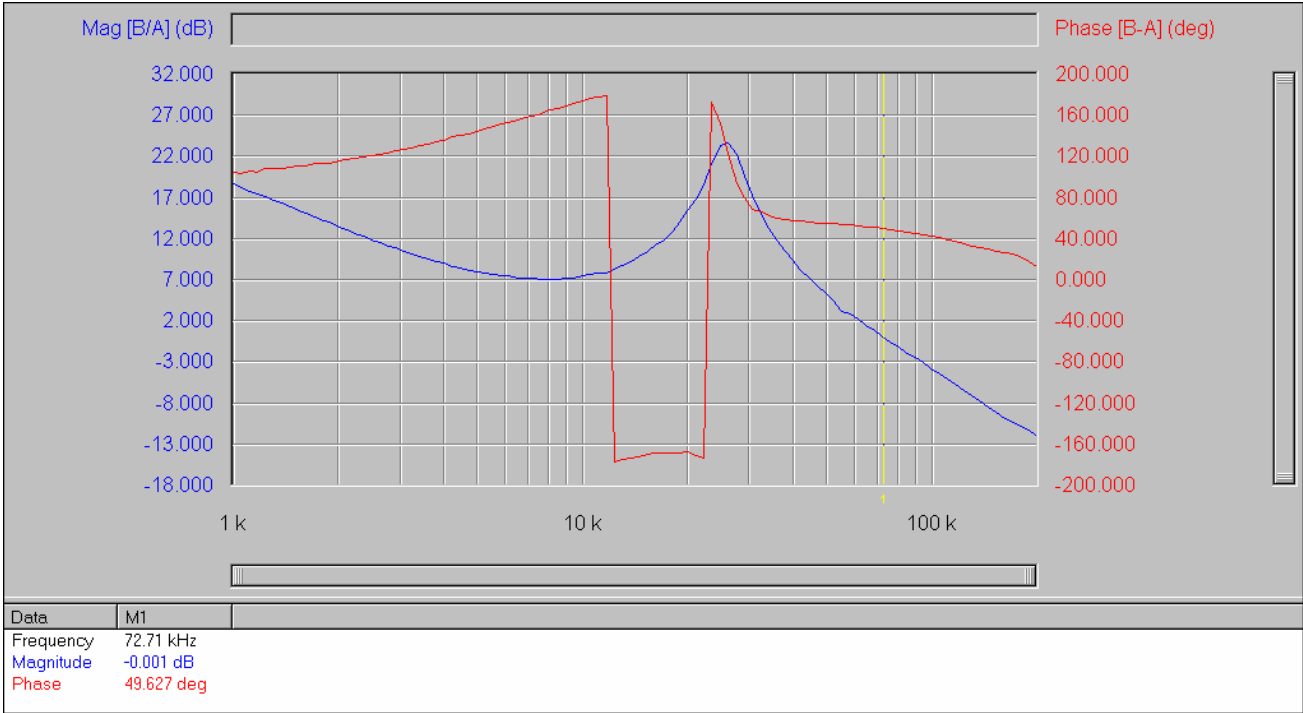


Fig. 10 Bode Plot of Control Loop

**TYPICAL OPERATING PERFORMANCE**

$V_{in}=12.0V$ ,  $V_o=1.8V$ ,  $F_s=600kHz$ , Room Temp, No Air Flow

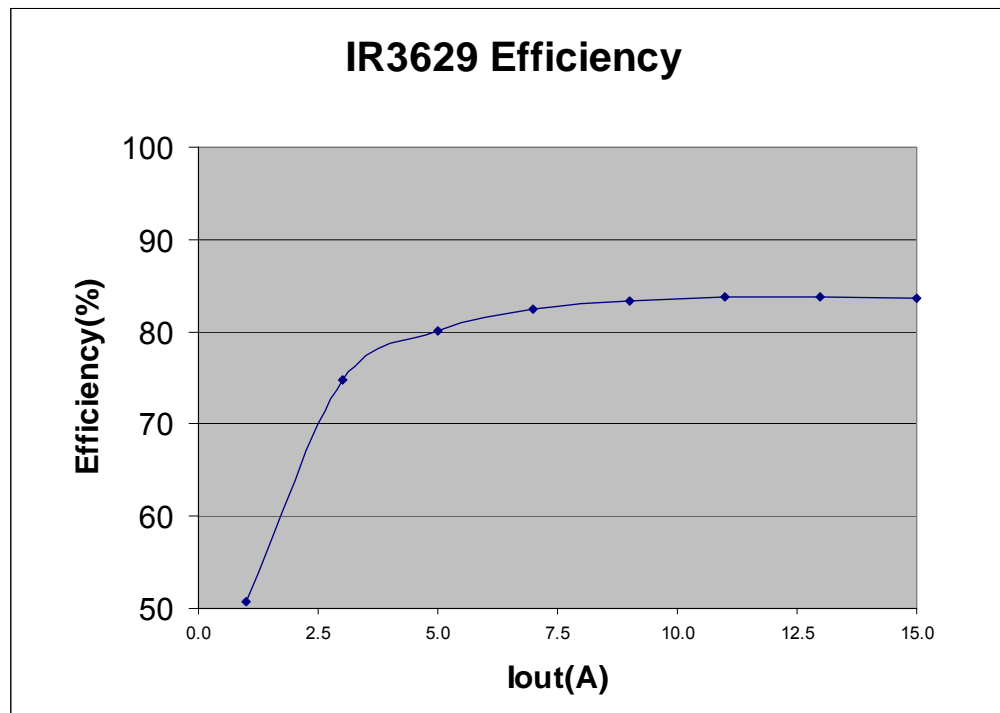


Fig. 11 Efficiency vs. Load

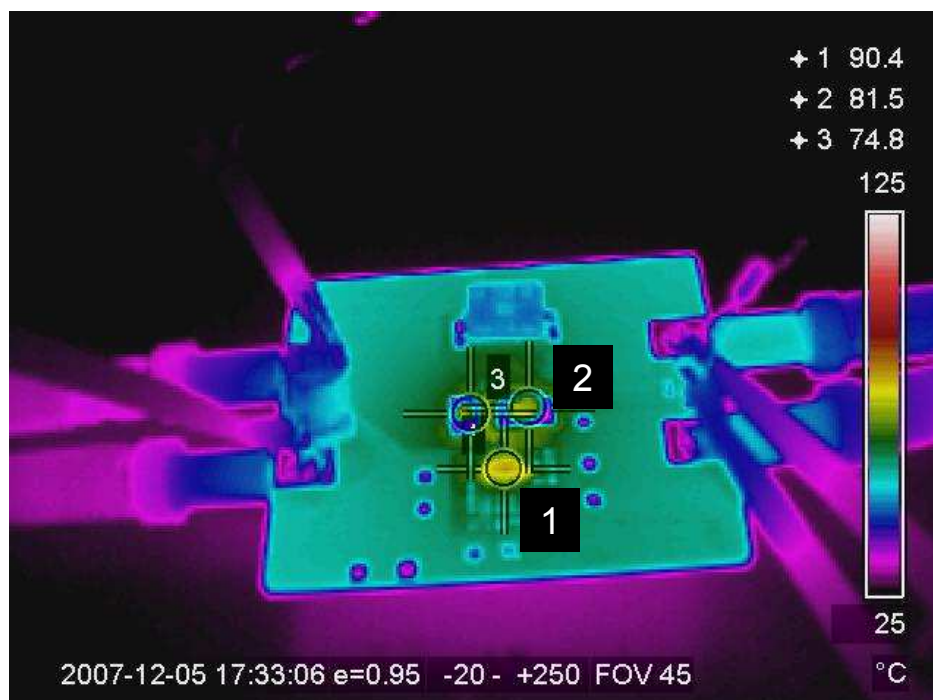
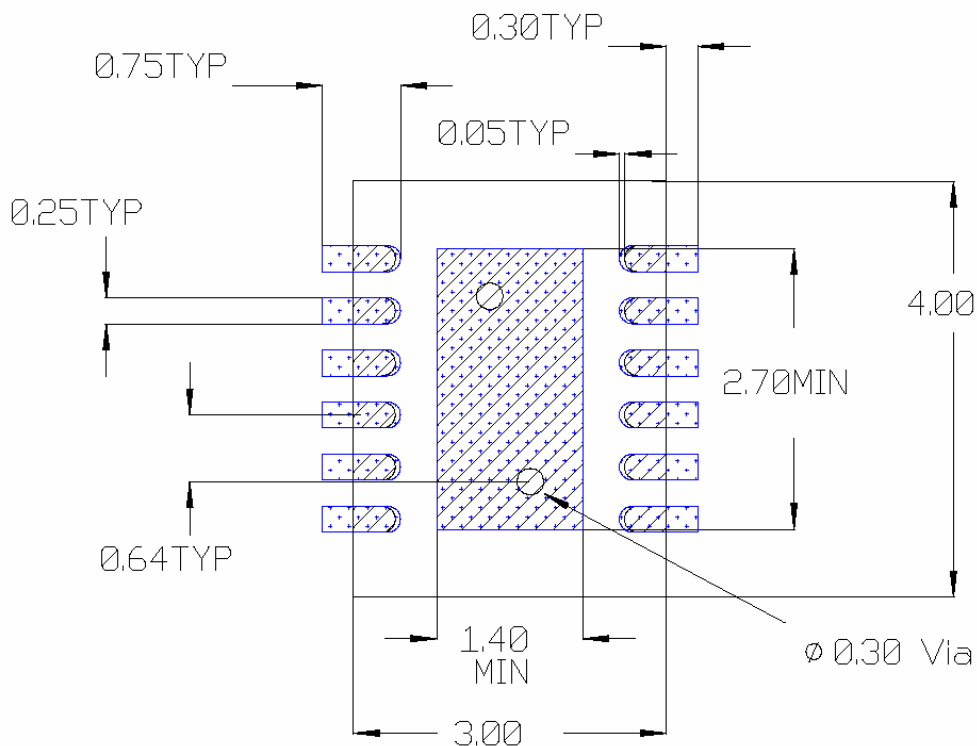


Fig. 12 Thermal Image of IR3629 Demo Board at  $I_o=15A$

(1: IR3629, 2: IRF6715, 3: IRF6712)

### PCB Metal and Components Placement

- The lead land width should be equal to the nominal part lead width. The minimum lead to lead spacing should be  $\geq 0.2\text{mm}$  to minimize shorting.
- The lead land length should be equal to maximum part lead length + 0.3 mm outboard extension + 0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- The center pad land length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be  $\geq 0.17\text{mm}$  for 2 oz. Copper ( $\geq 0.1\text{mm}$  for 1 oz. Copper and  $\geq 0.23\text{mm}$  for 3 oz. Copper).
- Two 0.30mm diameter via should be placed in the center of the pad land and connected to ground to minimize the noise effect on the IC.

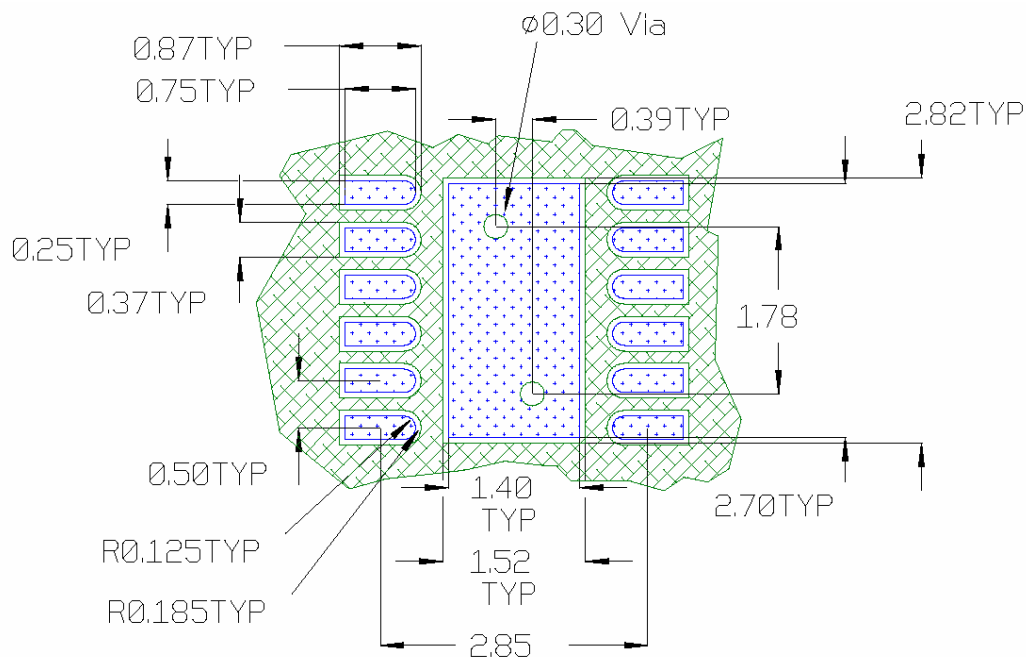


All Dimensions in mm

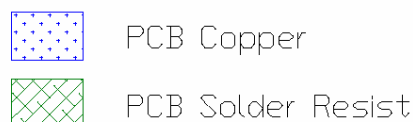


## Solder Resist

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist misalignment is a maximum of 0.05mm and it is recommended that the lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm.  
At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of  $\geq 0.17\text{mm}$  remains.
- The land pad should be Non Solder Mask Defined (NSMD), with a minimum pullback of the solder resist off the copper of 0.06mm to accommodate solder resist mis-alignment.
- Ensure that the solder resist in-between the lead lands and the pad land is  $\geq 0.15\text{mm}$  due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.
- Each via in the land pad should be tented or plugged from bottom boardside with solder resist.

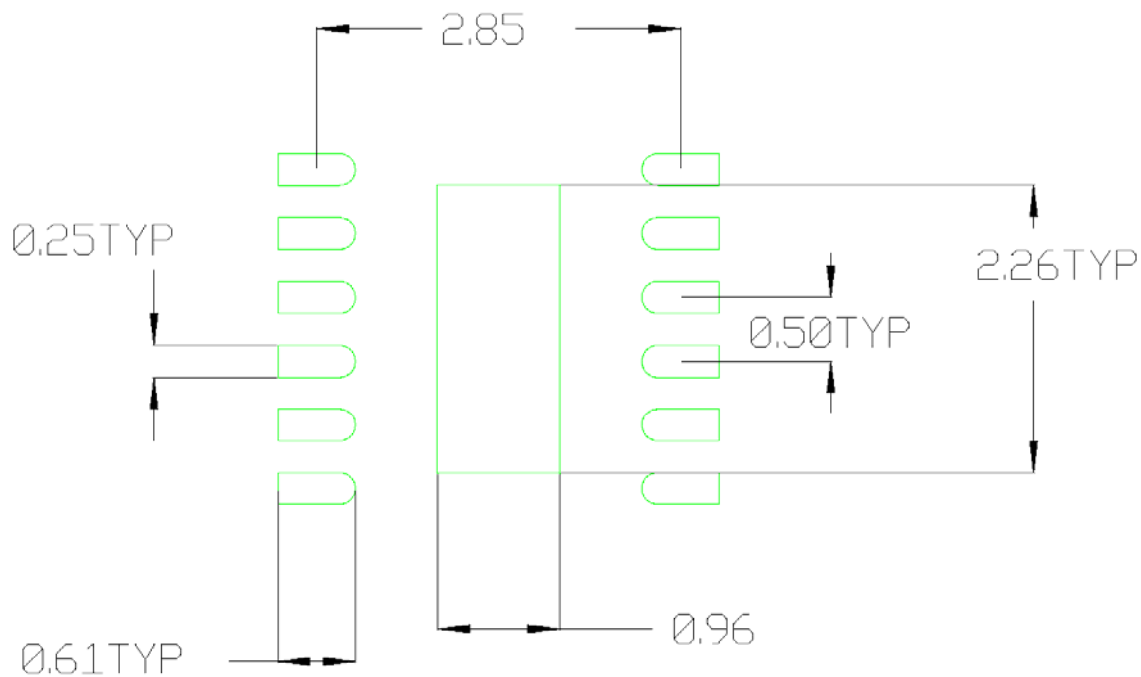


All Dimensions in mm



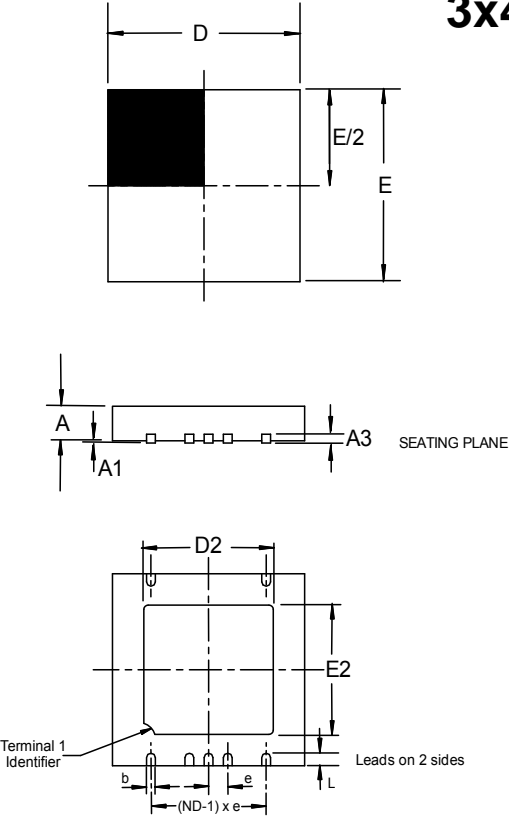
### Stencil Design

- The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.
- The land pad aperture should deposit approximately 50% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture  
All Dimensions in mm

IR3629 MLPD Package  
3x4-12Lead



SYMBOL	VGED-4					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	.032	.035	.039
A1	0.00	0.02	0.05	.000	.0008	.0019
A3	0.20 REF			.008 REF		
b	0.18	0.25	0.30	.0071	.0096	.0118
D2	3.0	—	3.70	.118	—	.145
D	4.00 BSC			.157 BSC		
E	3.00 BSC			.118 BSC		
E2	1.40	—	1.80	.055	—	.070
L	0.30	0.40	0.50	.012	.016	.019
e	0.50 PITCH			.020 PITCH		
N	12			10		
ND	6			6		

TAPE & REEL ORIENTATION

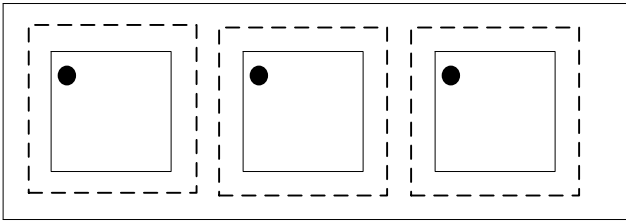


Figure A