1200V High Voltage High & Low-side, Gate Driver

BM60210FV-C

General Description

The BM60210FV-C is a monolithic high and low side gate drive IC, which can be drive high speed power MOSFET and IGBT driver with bootstrap operation.
The floating channel can be used to driven an N-channel power MOSFET or IGBT in the high side configuration which operates up to 1200V.
It incorporates the fault signal output functions, Under-voltage Lockout (UVLO) function and Miller clamp function.

Key Specifications

■ High-side floating supply voltage:	1200V
■ Output voltage range:	10V to 24V
■ Min Output Current:	3A
■ Turn ON/Off time:	75ns(Max)
■ Delay Matching:	25ns(Max)
■ Minimum input pulse width:	60ns(Max)
■ Operating temperature range:	-40°C to 125°C

Features

- Floating Channels for Bootstrap Operation to +1200V.
- Gate drive supply range from 10V to24V
- Built-in Under Voltage Lockout for Both Channels
- 3.3V and 5.0V Input Logic Compatible
- Active Miller Clamping
- AEC-Q100 Qualified (Note 1)
  (Note 1:Grade1)

Package

	W(Typ) x D(Typ) x H(Max)
SSOP-B20W	6.50mm x 8.10mm x 2.01mm

Applications

- MOSFET gate driver
- IGBT gate driver

Typical Application Circuits

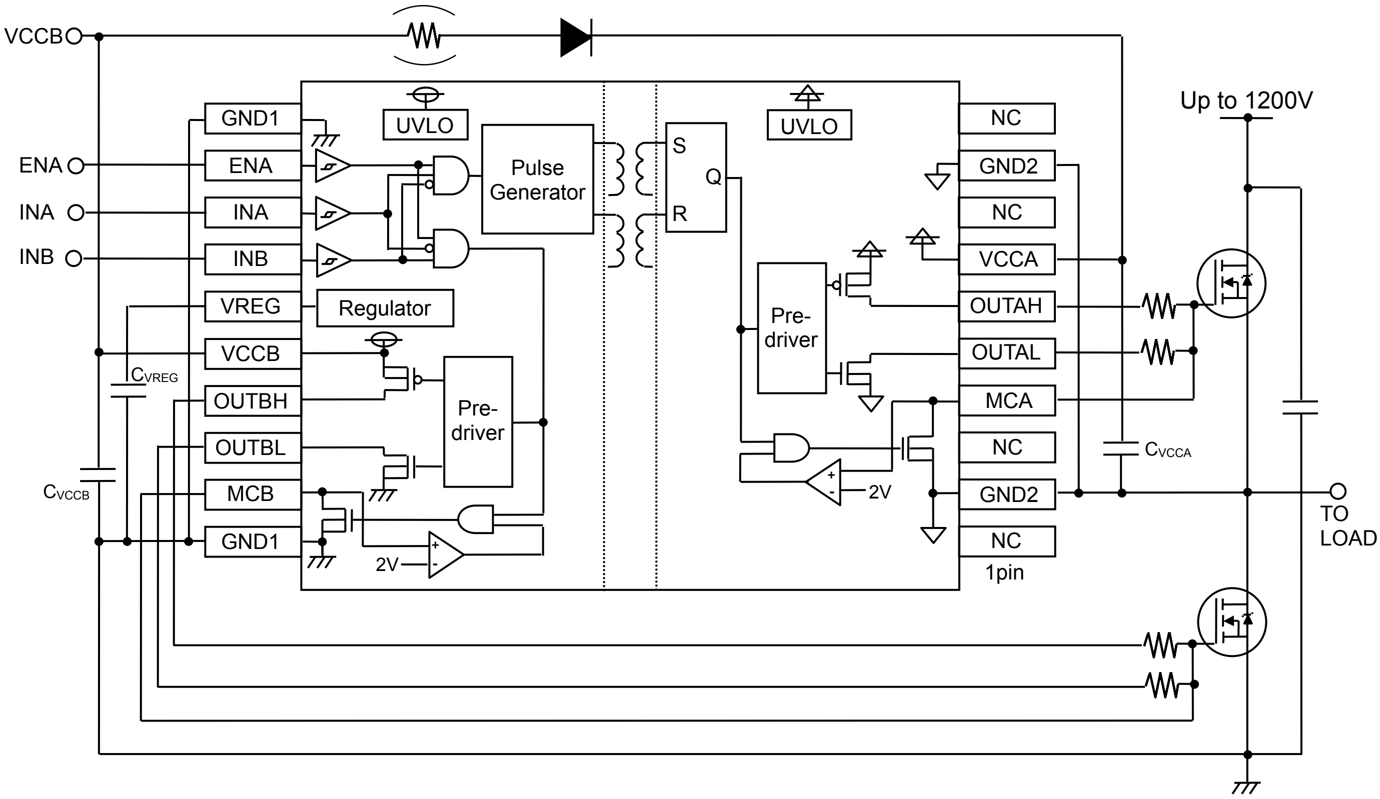


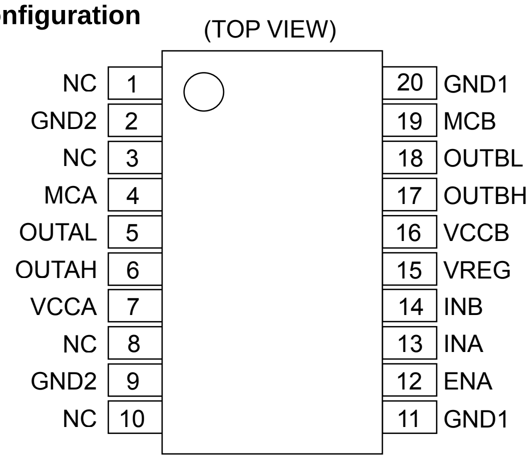
Figure 1. Typical Application Circuits

Contents

Recommended Range of External Constants

Pin Name	Symbol	Recommended Value			Unit
		Min.	Typ.	Max.	
VCCA	C_{VCCA}	0.1	1.0	-	μF
VCCB	C_{VCCB}	0.1	1.0	-	μF
VREG	C_{VREG}	0.1	3.3	10.0	μF

Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Function
1	NC	Non -connection
2	GND2	High -side ground pin
3	NC	Non -connection
4	MCA	High-side Output pin for Miller Clamp
5	OUTAL	High-side Output pin (Sink)
6	OUTAH	High-side Output pin (Source)
7	VCCA	High-side power supply pin
8	NC	Non -connection
9	GND2	High -side ground pin
10	NC	Non -connection
11	GND1	Low -side and input-side ground pin
12	ENA	Input enabling signal input pin
13	INA	Logic input for low side gate driver output
14	INB	Logic input for low side gate driver output
15	VREG	Power supply pin for input circuit
16	VCCB	Low -side and input-side power supply pin
17	OUTBH	low-side Output pin (Source)
18	OUTBL	low-side Output pin (Sink)
19	MCB	low-side Output pin for Miller Clamp
20	GND1	Low -side and input-side ground pin

Description of pins and cautions on layout of board

1) VCCA (High-side power supply pin)
The VCCA pin is a power supply pin on the high-side output. To reduce voltage fluctuations due to OUT pin output current, connect a bypass capacitor between the VCCA and the GND2 pins.

2) GND2 (High -side ground pin)
The GND2 pin is a ground pin on the high-side. Connect the GND2 pin to the emitter / source of a high-side power device.

3) VCCB (Low -side and input-side power supply pin)
The VCCB pin is a power supply pin on the low-side output. To reduce voltage fluctuations due to OUT pin output current, connect a bypass capacitor between the VCCB and the GND2 pins.

4) GND1 (Low -side and input-side ground pin)
The GND1 pin is a ground pin on the low-side and the input side.

5) VREG (Power supply pin for input circuit)
The VCC1 pin is a power supply pin for the input circuit. To suppress voltage fluctuations due to the current to drive internal transformers, connect a bypass capacitor between the VREG and the GND1 pins.

6) INA, INB, ENA (Control input terminal)
The INA, INB and ENA pins are used to determine output logic.

ENA	INA	INB	OUTA	OUTB
L	X	X	L	L
H	L	L	L	L
H	L	H	L	H
H	H	L	H	L
H	H	H	L	L

7) OUTAH, OUTAL, OUTBH, OUTBL (Output pin)
The OUTAH pin and the OUTBH pin are source side pins used to drive the gate of a power device, and the OUTAL pin and the OUTBL pin are sink side pins used to drive the gate of a power device.

8) MCA, MCB (Output pin for Miller Clamp)
The MC pin is for preventing the increase in gate voltage due to the Miller current of the power device connected to the OUT pin. If the Miller Clamp function is not used, short-circuit the MCA pin to the GND2 pin and the MCB pin to the GND1 pin.

Description of functions and examples of constant setting

1) Miller Clamp function
When INA=L and OUT pin voltage < V_{MCON} (typ 2V), the internal MOSFET of the MC pin is turned ON.

INA	MC	Internal MOSFET of the MC pin
L	less than V_{MCON}	ON
H	X	OFF

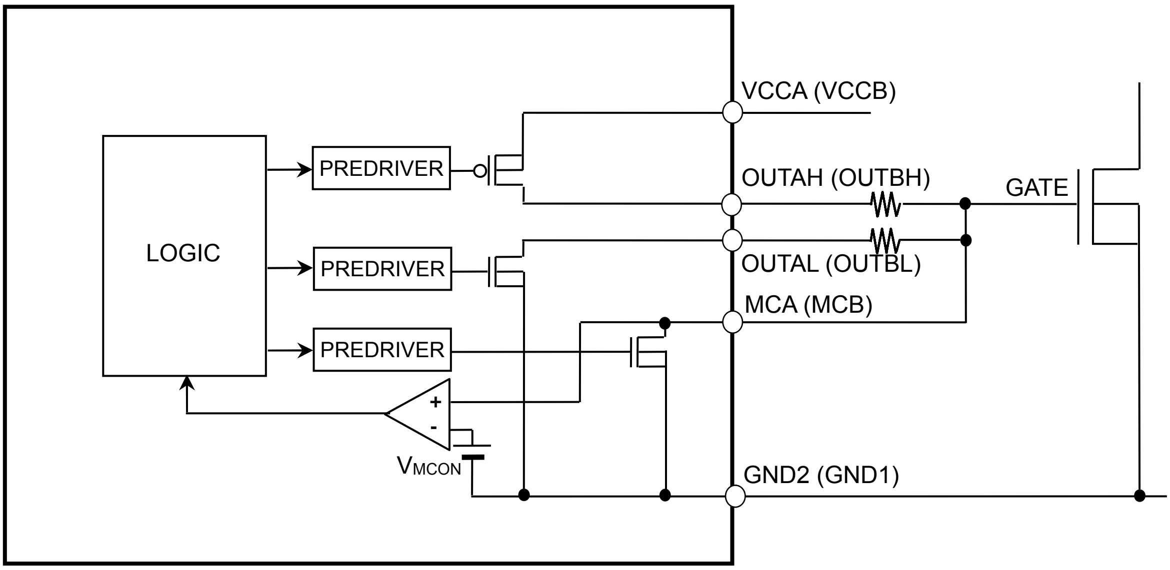


Figure 2. Block diagram of Miller Clamp function.

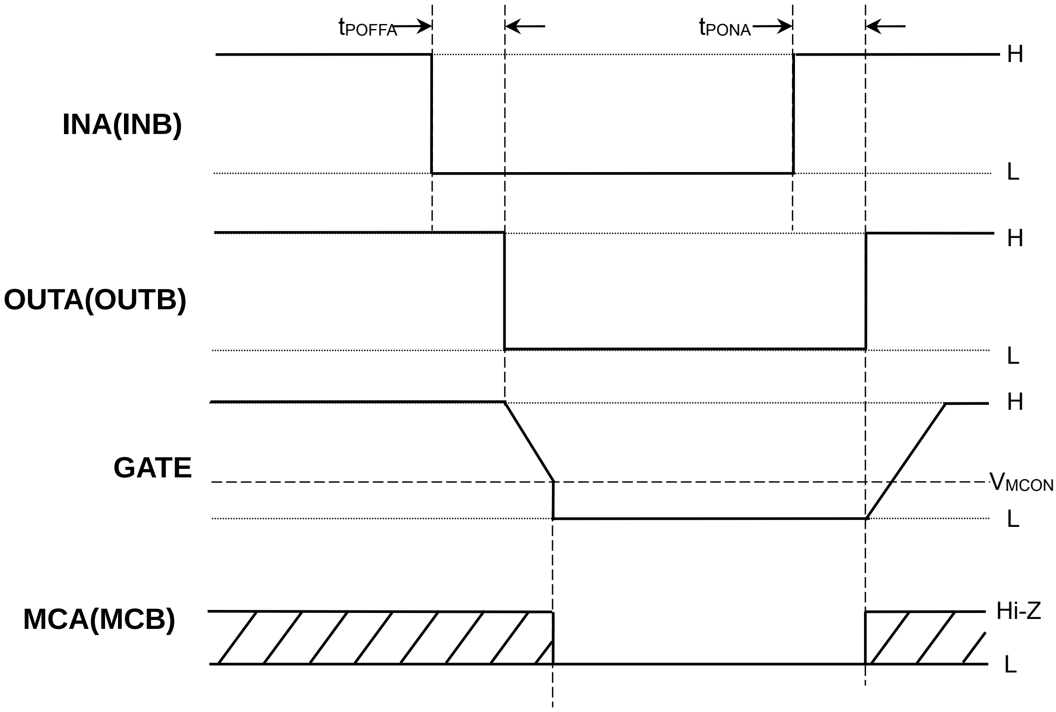


Figure 3. Timing chart of Miller Clamp function

2) Under-voltage Lockout (UVLO) function

The BM60210FV-C incorporates the Under-voltage Lockout (UVLO) function both of VCCA and VCCB. When the power supply voltage drops to the UVLO ON voltage (typ 8.5V), the OUT pin will output the “L” signal. In addition, to prevent malfunctions due to noises, a mask time of $t_{UVLOMSK}$ (typ 2.5μs) is set on both the low and the high voltage sides.

This IC does not have a function which feeds back the high voltage side state to the low voltage side. After the high voltage side UVLO is released, the input signal will take effect from the time after the input signal switches.

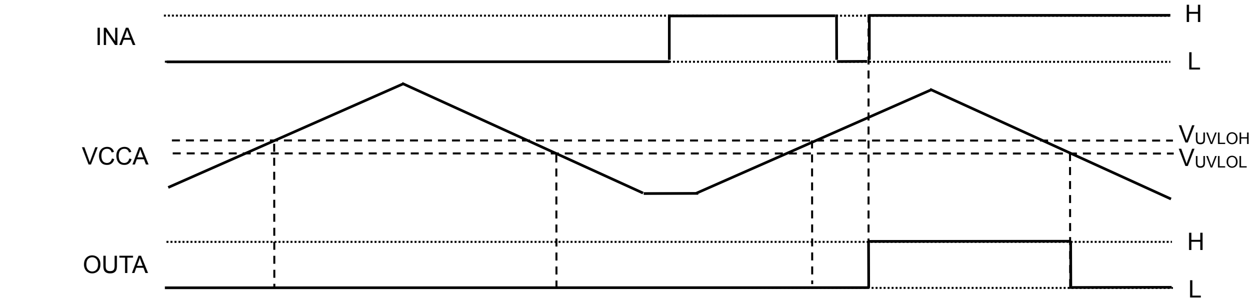


Figure 4. Input-side UVLO Function Operation Timing Chart

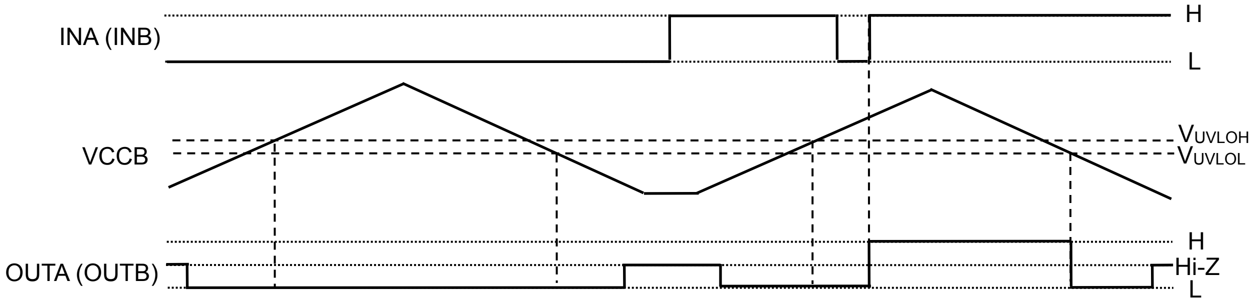


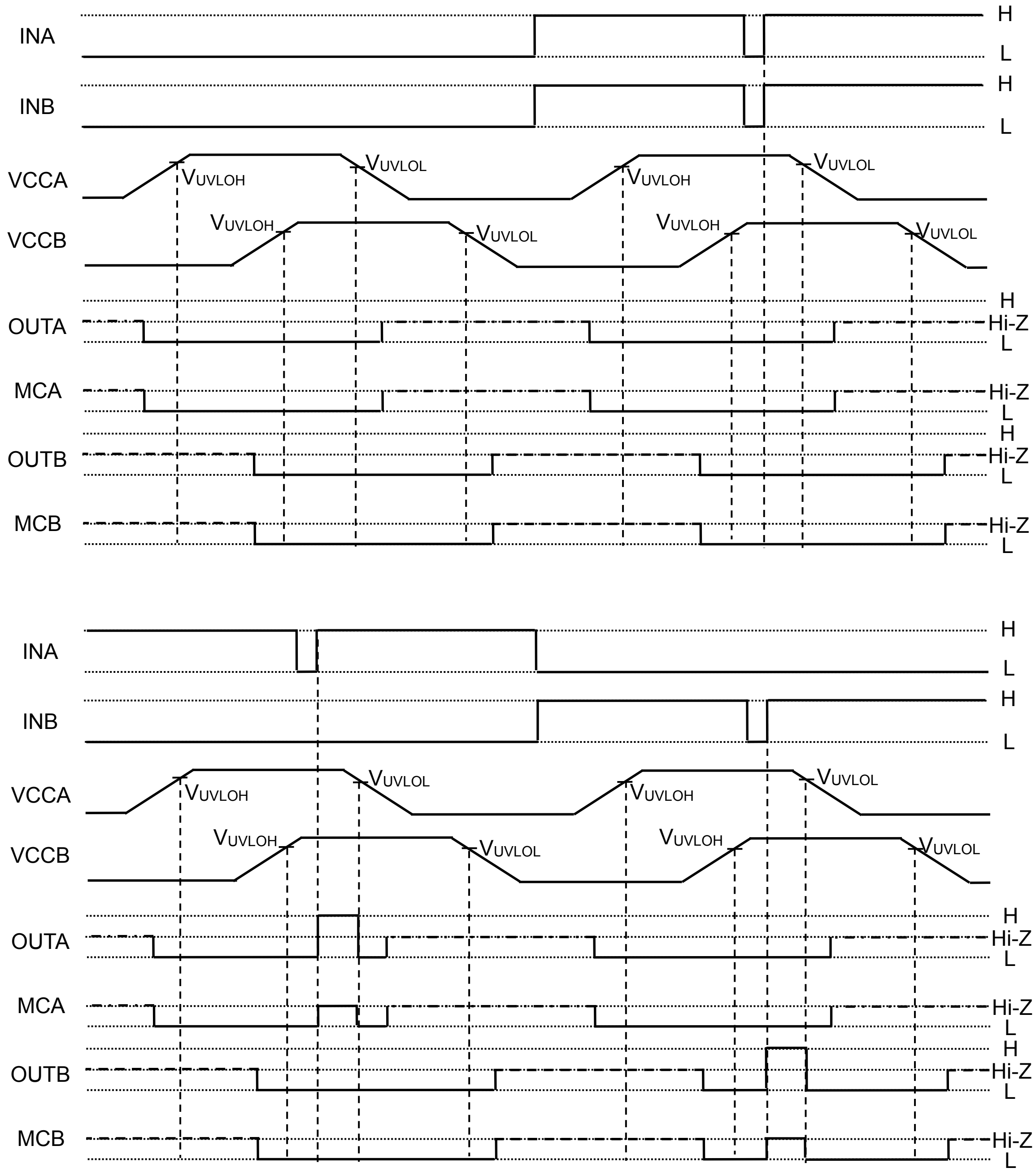
Figure 5. Output-side UVLO Function Operation Timing Char

3）I/O condition table

No.	Status	Input					Output			
		VCCB	VCCA	ENA	INB	INA	OUTB	MCB	OUTA	MCA
1	VCCB UVLO	UVLO	X	X	X	X	L	L	L	L
2	VCCA UVLO	○	UVLO	L	X	X	L	L	L	L
3		○	UVLO	H	L	X	L	L	L	L
4		○	UVLO	H	H	X	H	Hi-Z	L	L
5	Disable	○	○	L	X	X	L	L	L	L
6	Normal operation	○	○	H	L	L	L	L	L	L
7		○	○	H	L	H	L	L	H	Hi-Z
8		○	○	H	H	L	H	H	L	L
9		○	○	H	H	H	L	L	L	L

○ : VCCA or VCCB > UVLO, X : Don't care

4) Power supply startup / shutoff sequence



–·–·–·– : Since the VCCA to GND2 pin voltage is low and the output MOS does not turn ON, the output pins become Hi-Z.

- - - - - - : Since the VCCB to GND1 pin voltage is low and the output MOS does not turn ON, the output pins become Hi-Z.

Figure 6. Power Supply Startup / Shutoff Sequence

Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
High side floating supply voltage	V_{CCA}	-0.3～+1230(Note 1)	V
High side offset voltage	GND2	VCCA-30～VCCA+0.3	V
High side floating output voltage OUTA	V_{OUTA}	GND2-0.3～VCCA+0.3	V
Low side and logic fixed supply voltage	V_{CCB}	-0.3～+30.0(Note 1)	V
Low side output voltage OUTB	V_{OUTB}	-0.3～+VCCB+0.3 or +30.0(Note 1)	V
Logic input voltage (INA, INB)	V_{IN}	-0.3～+VCCB+0.3 or +30.0(Note 1)	V
OUTA pin output current (Peak 1μs)	$I_{OUTAPEAK}$	5.0(Note 2)	A
OUTB pin output current (Peak 1μs)	$I_{OUTBPEAK}$	5.0(Note 2)	A
MCA pin output current (Peak 1μs)	$I_{MCAPEAK}$	5.0(Note 2)	A
MCB pin output current (Peak 1μs)	$I_{MCBPEAK}$	5.0(Note 2)	A
Power dissipation	P_d	1.19(Note 3)	W
Operating temperature range	T_{opr}	-40～+125	°C
Storage temperature range	T_{stg}	-55～+150	°C
Junction temperature	T_{jmax}	+150	°C

(Note 1) Relative to GND1.
(Note 2) Should not exceed Pd and Tj=150°C
(Note 3) Derate by 9.5mW/°C when operating above Ta=25°C. Mounted on a glass epoxy of 70mm ×70mm ×1.6mm.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Ratings

Parameter	Symbol	Min.	Max.	Units
High side floating supply voltage	V_{CCA}	GND2+10	GND2+24	V
High side floating supply offset voltage	GND2	-	1200	V
High side (OUTA) output voltage	V_{OUTA}	GND2	VCCA	V
High side (OUTB) output voltage	V_{OUTB}	GND1	VCCB	V
Logic input voltage (INA, INB)	V_{IN}	GND1	VCCB	V
Low side supply voltage	V_{CCB}	10	24	V
Ambient temperature	Ta	-40	+125	°C

Electrical Characteristics

(Unless otherwise specified T_a=-40°C to 125°C、V_{CCA}=10V to 24V、V_{CCB}=10V to 24V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
General						
VCCB circuit current 1	I_{CC11}	0.31	0.47	0.84	mA	OUTB=L
VCCB circuit current 2	I_{CC12}	0.28	0.40	0.79	mA	OUTB=H
VCCB circuit current 3	I_{CC12}	0.36	0.53	0.92	mA	INA =10kHz, Duty=50%
VCCB circuit current 4	I_{CC13}	0.41	0.61	1.07	mA	INA =20kHz, Duty=50%
VCCA circuit current 1	I_{CC21}	0.26	0.47	0.72	mA	OUTA=L
VCCA circuit current 2	I_{CC22}	0.22	0.45	0.66	mA	OUTA=H
Logic block						
Logic high level input voltage	V_{INH}	2.0	-	V_{CCB}	V	INA, INB, ENA
Logic low level input voltage	V_{INL}	0	-	0.8	V	INA, INB, ENA
Logic pull-down resistance	R_{IND}	25	50	100	kΩ	INA, INB, ENA < 3V
Logic pull-down current	I_{IND}	20	50	150	µA	INA, INB, ENA ≥ 3V
Logic input minimum pulse width	t_{INMIN}	-	-	60	ns	INA, INB
ENA input mask time	t_{ENAMSK}	0.6	1	1.4	µs	ENA
Output						
OUT ON resistance (Source)	R_{ONH}	0.4	0.9	2.0	Ω	I_{OUT}=-40mA, OUTA, OUTB
OUT ON resistance (Sink)	R_{ONL}	0.2	0.6	1.3	Ω	I_{OUT}=40mA, OUTA, OUTB
OUT maximum current (Source)	$I_{OUTMAXH}$	3.0	4.5	-	A	Guaranteed by design, OUTA, OUTB
OUT maximum current (Sink)	$I_{OUTMAXL}$	3.0	3.9	-	A	Guaranteed by design, OUTA, OUTB
OUT Turn ON time	t_{PON}	35	55	75	ns	OUTA, OUTB
OUT Turn OFF time	t_{POFF}	35	55	75	ns	OUTA, OUTB
OUT Propagation distortion	t_{PDISTA}	-25	0	25	ns	$t_{POFF} – t_{PON}$, OUTA, OUTB
Delay matching, HS&LS turn ON/OFF	t_{DM}	-	-	25	ns	
OUT Rise time	t_{RISE}	-	50	-	ns	OUT-GND 間 10nF, OUTA, OUTB
OUT Fall time	t_{FALL}	-	50	-	ns	OUT-GND 間 10nF, OUTA, OUTB
MC ON resistance	R_{ONMC}	0.20	0.65	1.40	Ω	I_{MC}=40mA, MCA, MCB
MC ON threshold voltage	V_{MCON}	1.8	2	2.2	V	MCA, MCB
VREG output voltage	V_{VREG}	4.2	4.7	5.2	V	
Common Mode Transient Immunity	CM	100	-	-	kV/µs	Guaranteed by design
Protection functions						
UVLO OFF voltage	V_{UVLOH}	9.0	9.5	10.0	V	VCCA, VCCB
UVLO ON voltage	V_{UVLOL}	8.0	8.5	9.0	V	VCCA, VCCB
UVLO mask time	$t_{UVLOAMSK}$	1.0	2.5	5.0	µs	VCCA, VCCB

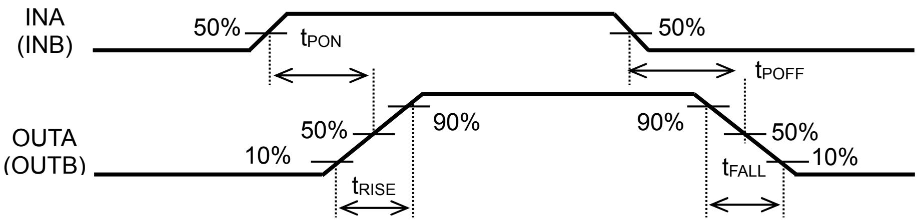


Figure 7. IN-OUT Timing Chart

Typical Performance Curves

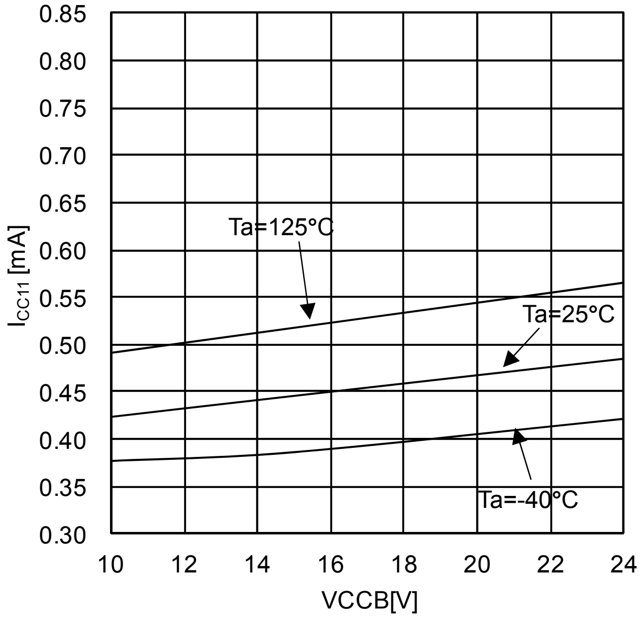


Figure 8. VCCB circuit current 1
(OUTB=L)

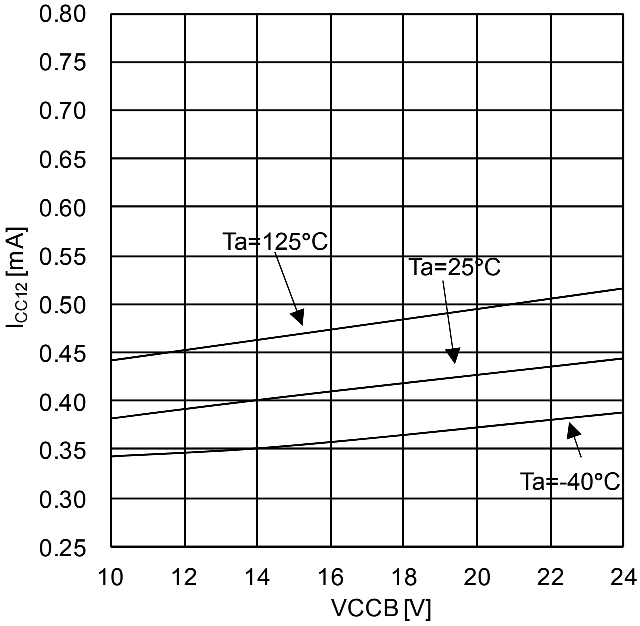


Figure 9. VCCB circuit current 2
(OUTB=H)

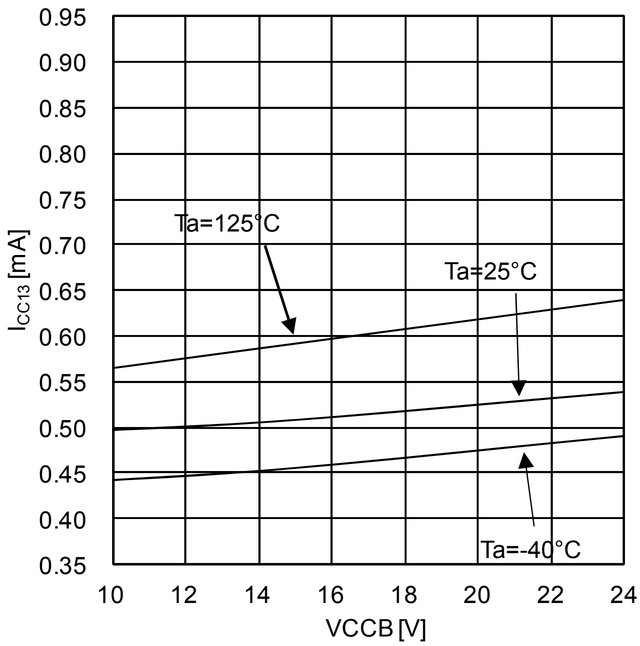


Figure 10. VCCB circuit current 3
（INA=10kHz, Duty=50%）

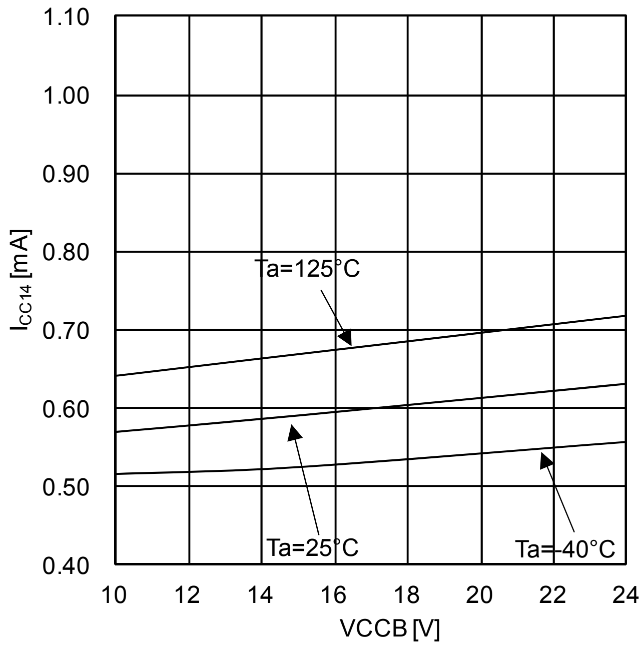


Figure 11. VCCB circuit current 4
(INA=20kHz, Duty=50%）

Typical Performance Curves - continued

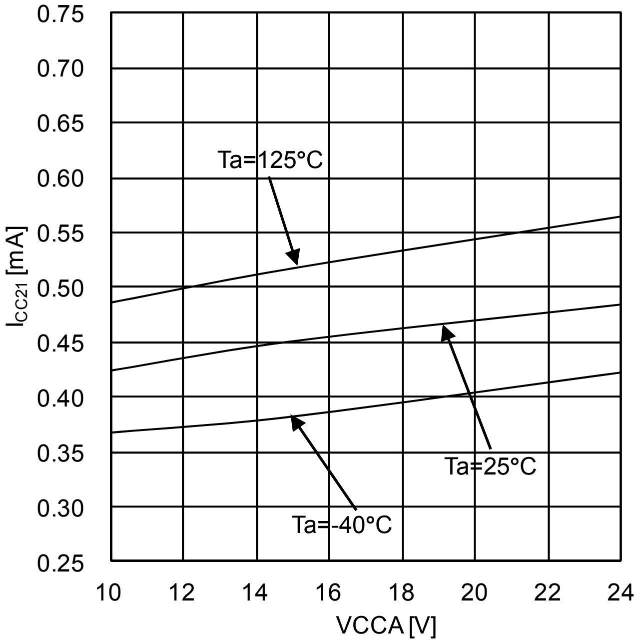


Figure 12. VCCA circuit current 1
(OUTA=L)

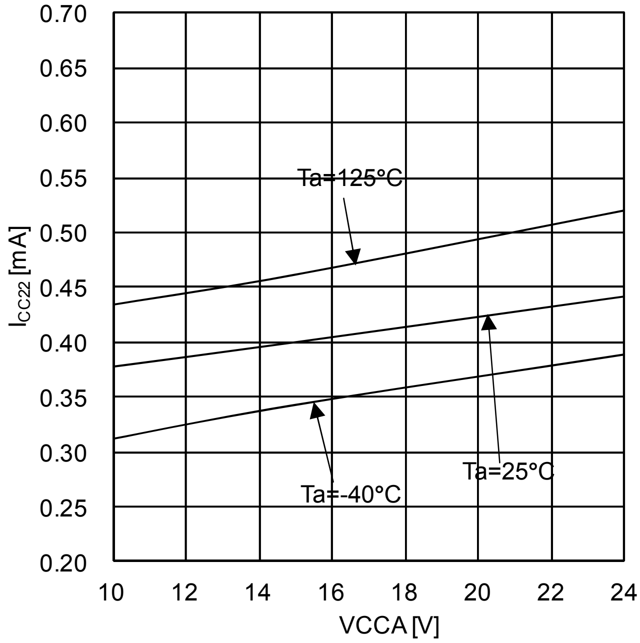


Figure 13. VCCA circuit current 2
(OUTA=H)

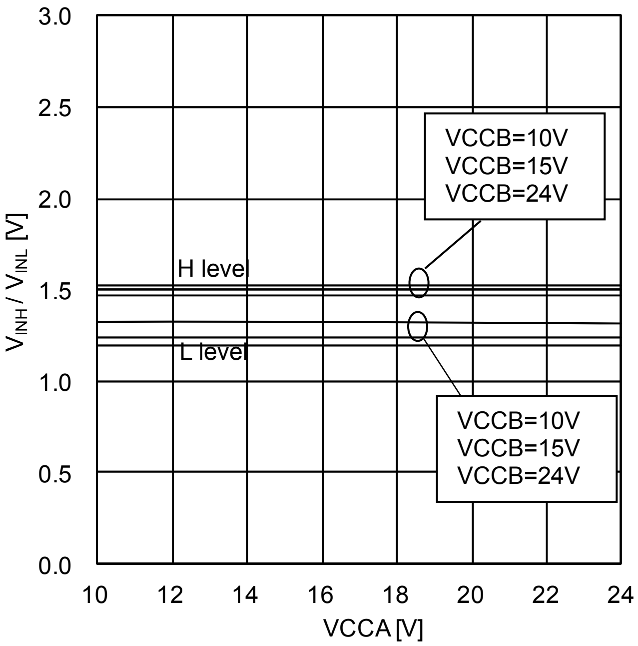


Figure 14. logic(INA/INB)H/L level
input voltage

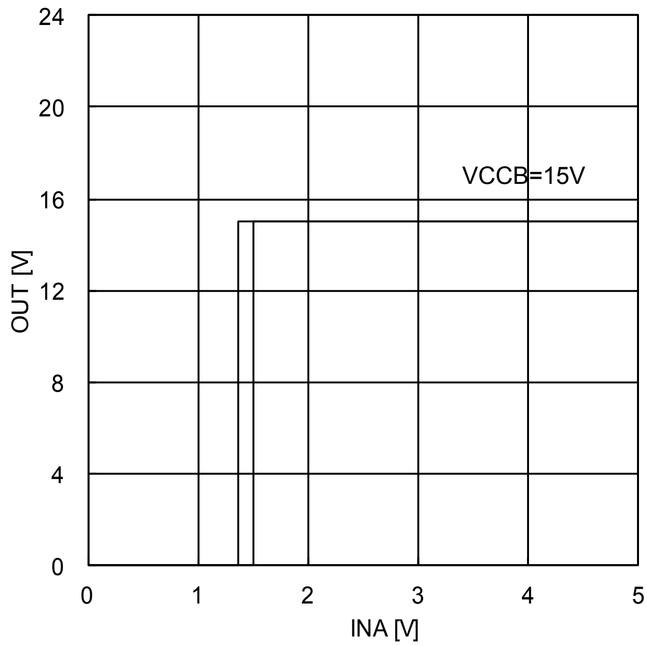


Figure 15. OUTA output voltage vs INA input voltage
(VCCB=15V, VCCA=15V, Ta=25°C)

Typical Performance Curves - continued

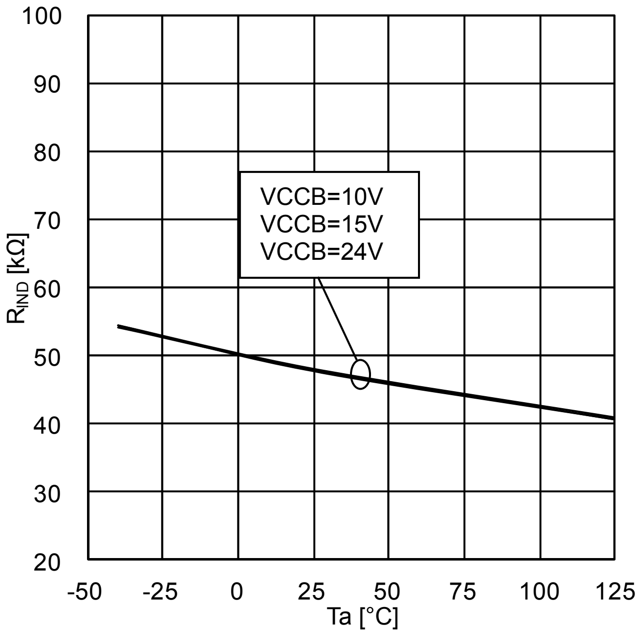


Figure 16. logic pull-down resistance

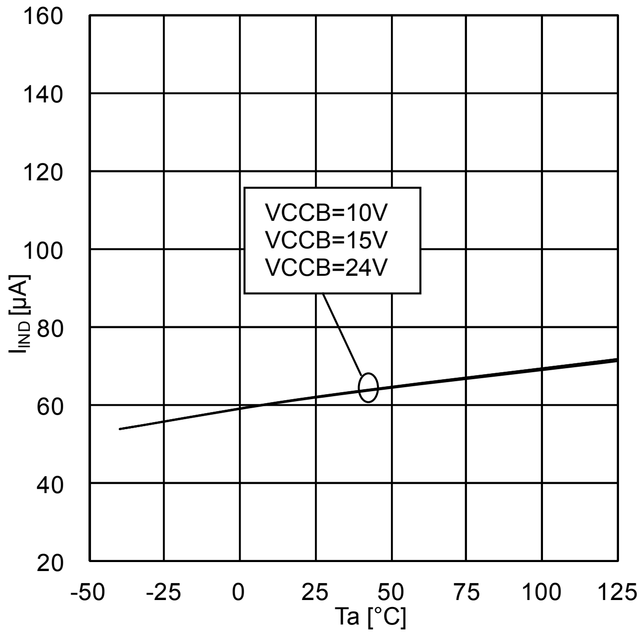


Figure 17. logic pull-down current

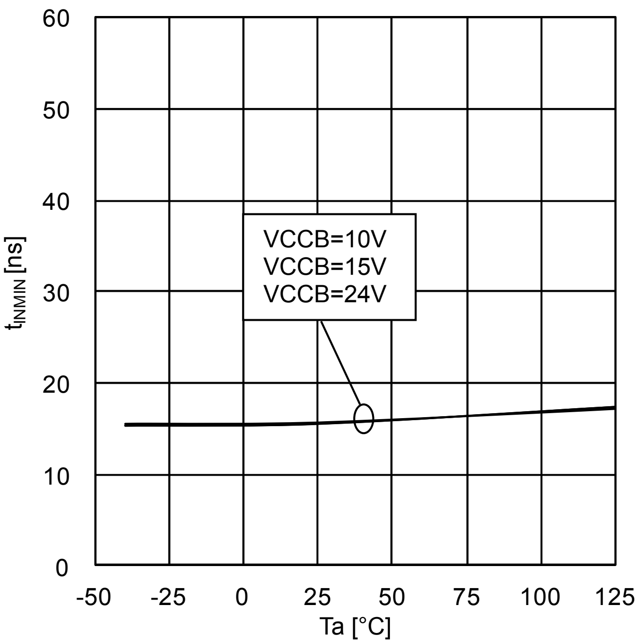


Figure 18. logic(INA)input mask time

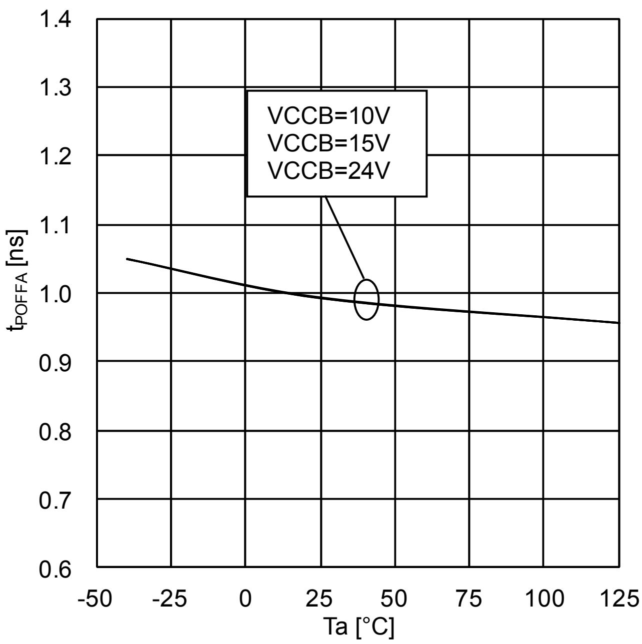


Figure 19. ENA input mask time

Typical Performance Curves - continued

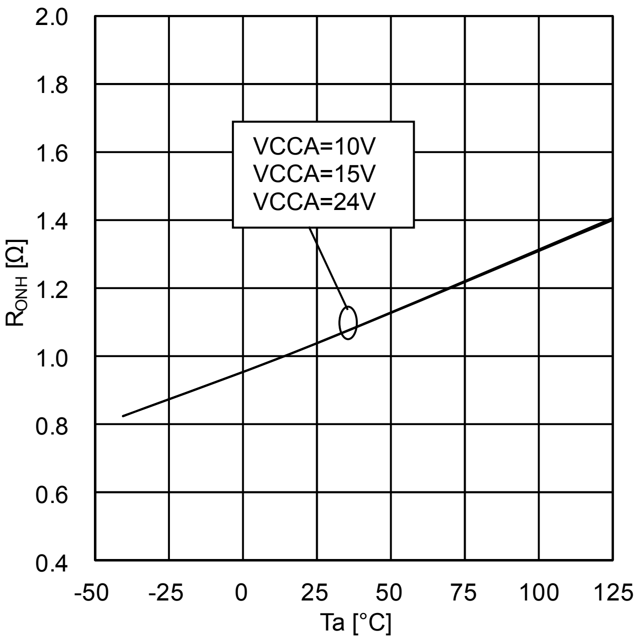


Figure 20. OUTA ON resistance (Source)

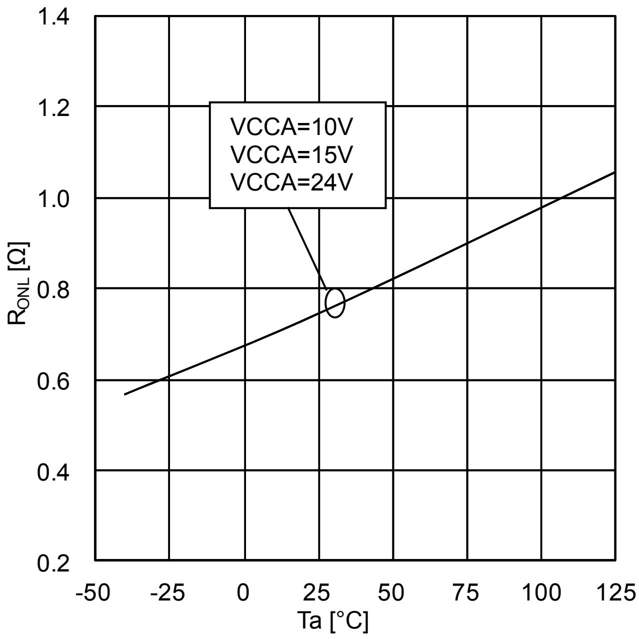


Figure 21. OUTA ON resistance (Sink)

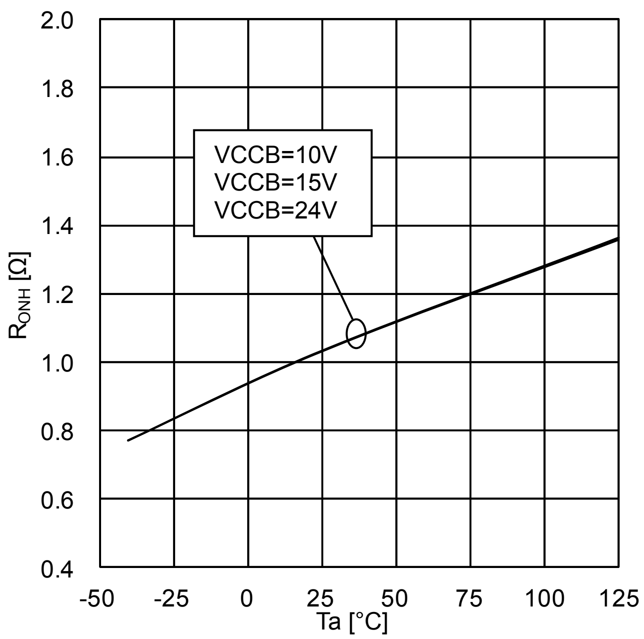


Figure 22. OUTB ON resistance (Source)

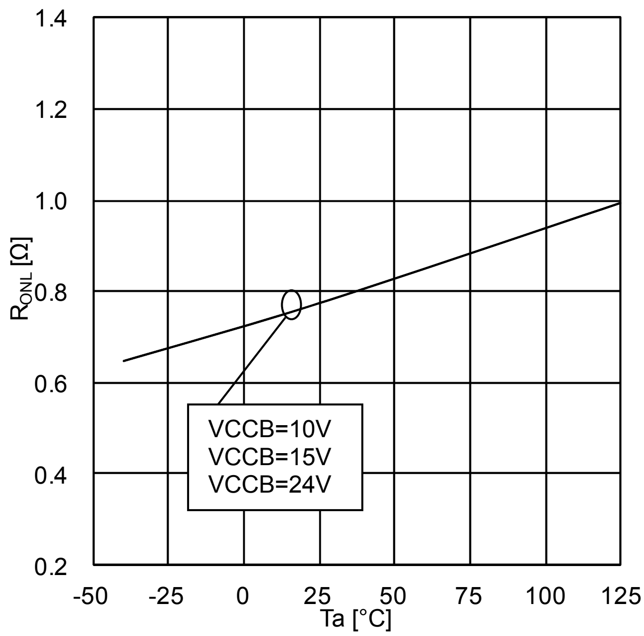


Figure 23. OUTB ON resistance (Sink)

Typical Performance Curves - continued

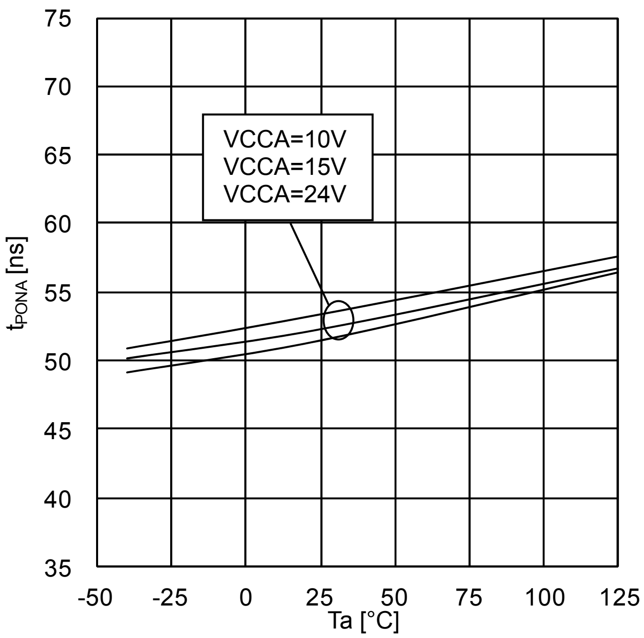


Figure 24. Turn ON Time
(INA=PWM, INB=L)

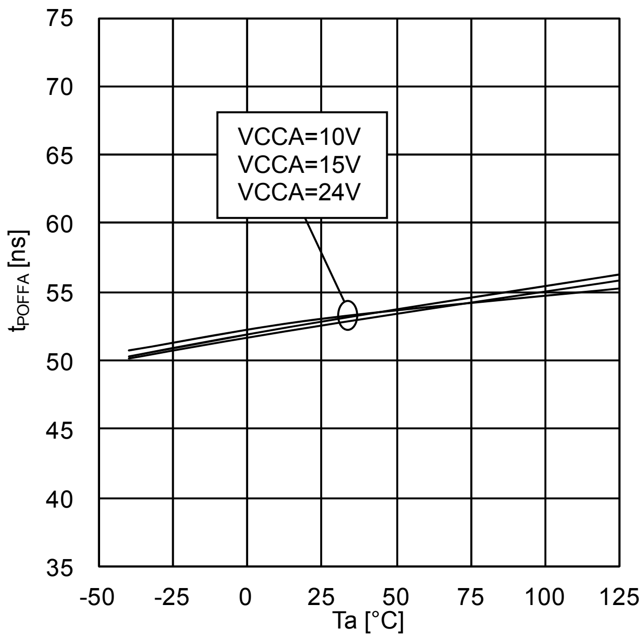


Figure 25. Turn OFF Time
(INA=PWM, INB=L)

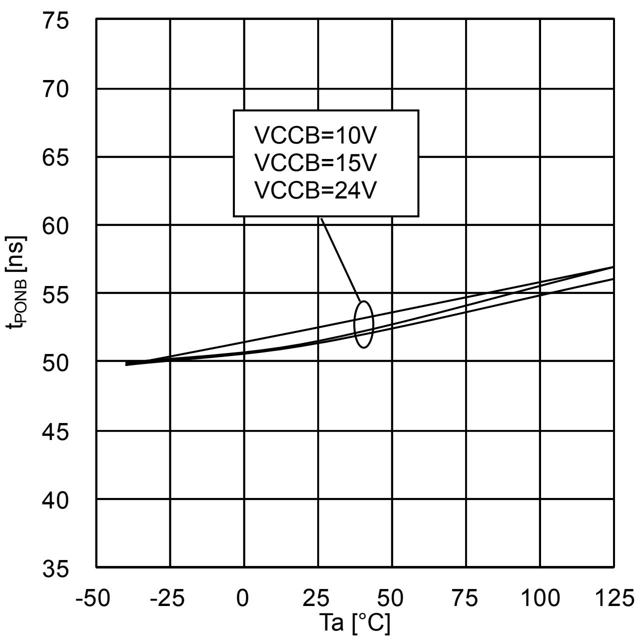


Figure 26. Turn ON Time
(INA=L, INB=PWM)

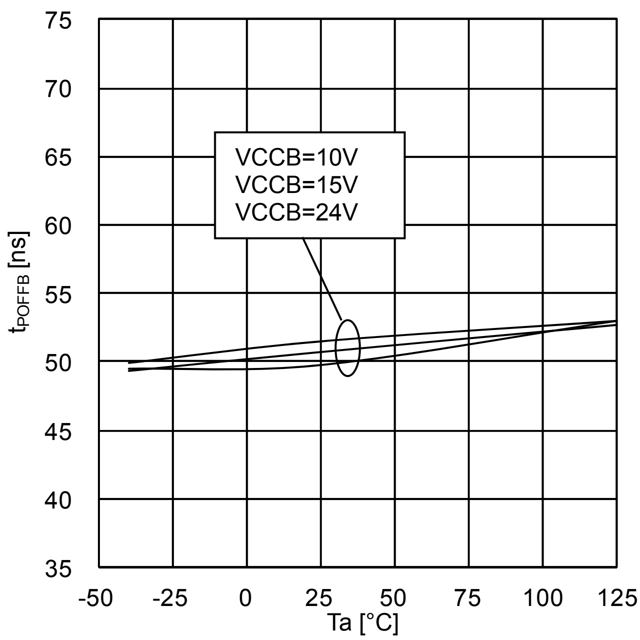


Figure 27. Turn OFF Time
(INA=L, INB=PWM)

Typical Performance Curves - continued

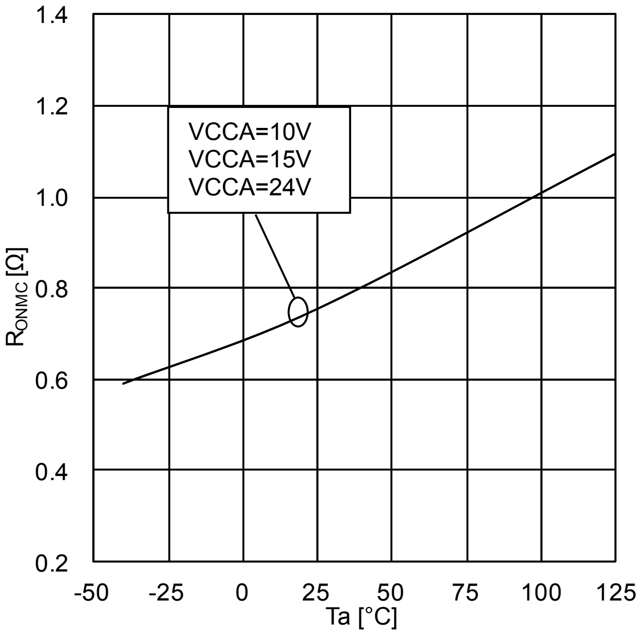


Figure 28. MCA ON resistance

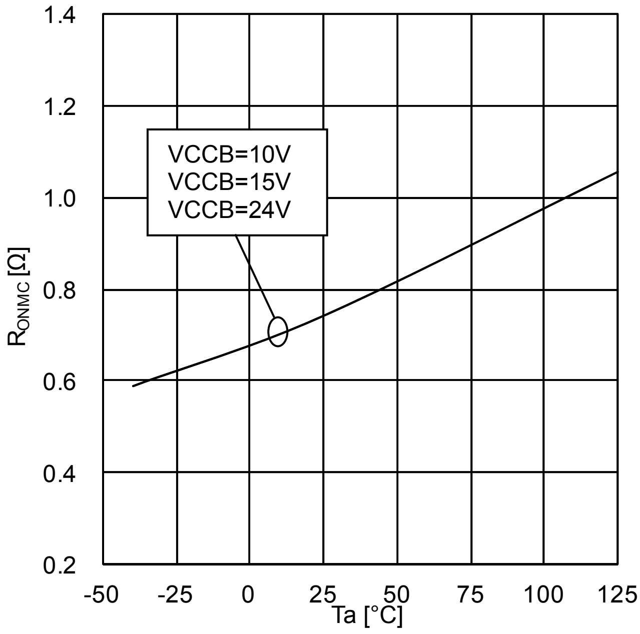


Figure 29. MCB ON resistance

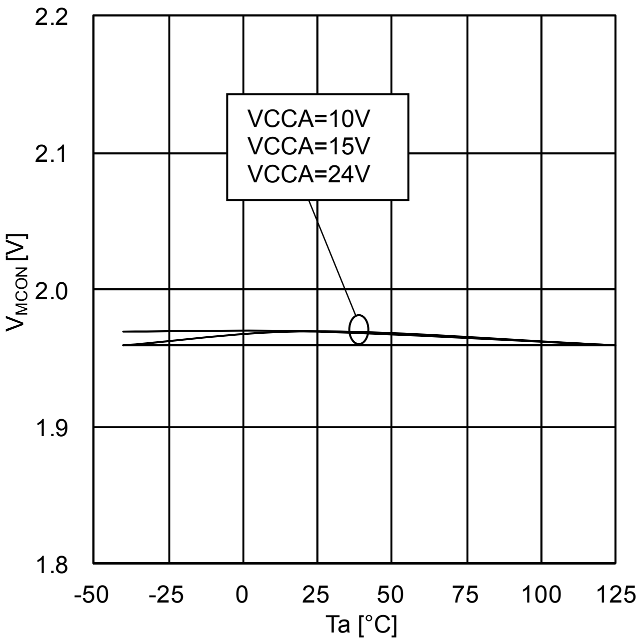


Figure 30. MCA ON threshold

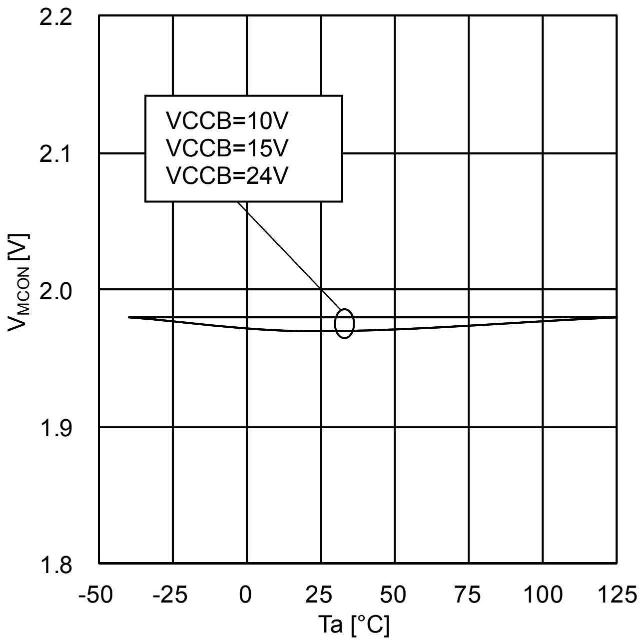


Figure 31. MCB ON threshold

Typical Performance Curves - continued

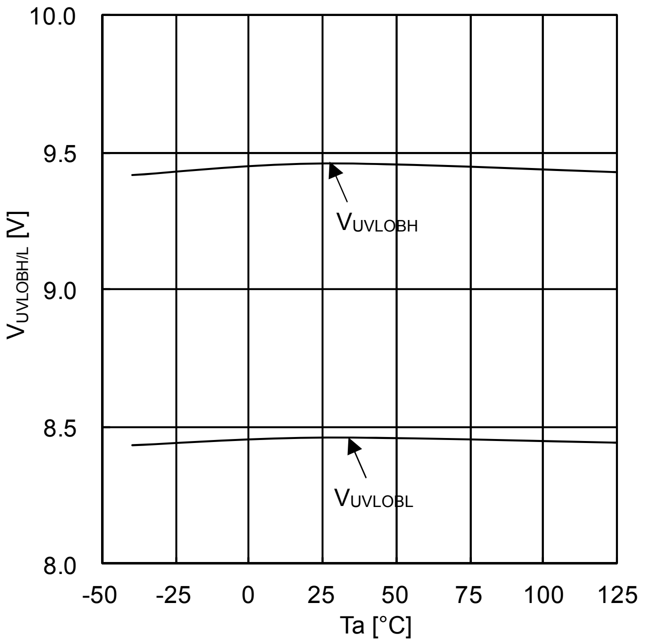


Figure 32. VCCB UVLO ON/OFF voltage

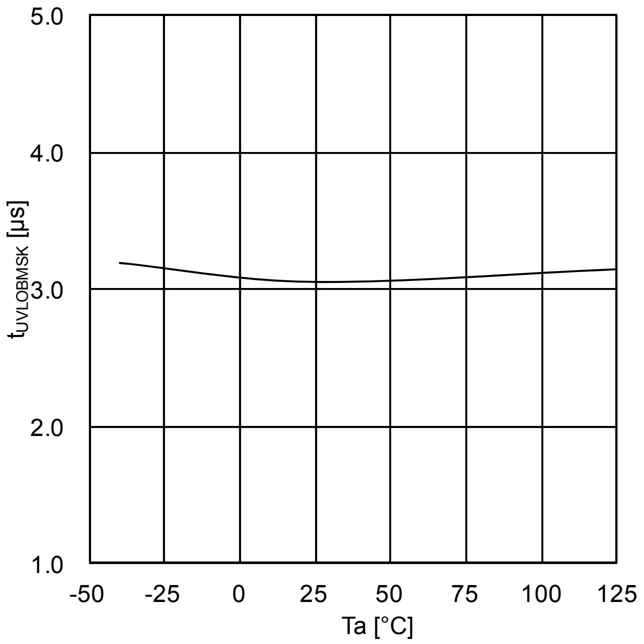


Figure 33. VCCB UVLOmask time

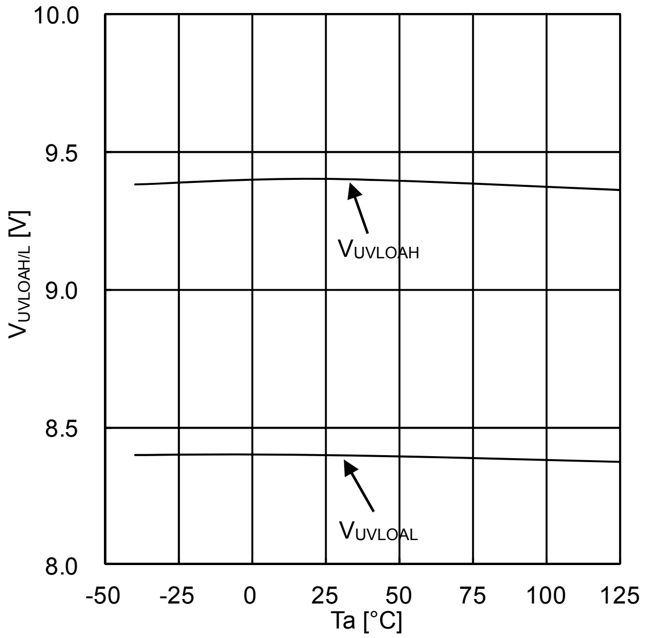


Figure 34. VCCA UVLO ON/OFF voltage

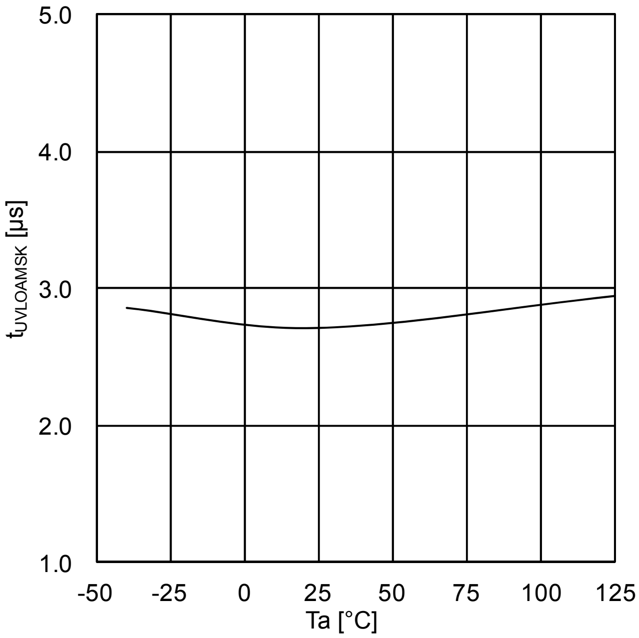


Figure 35. VCCA UVLO mask time

Power Dissipation

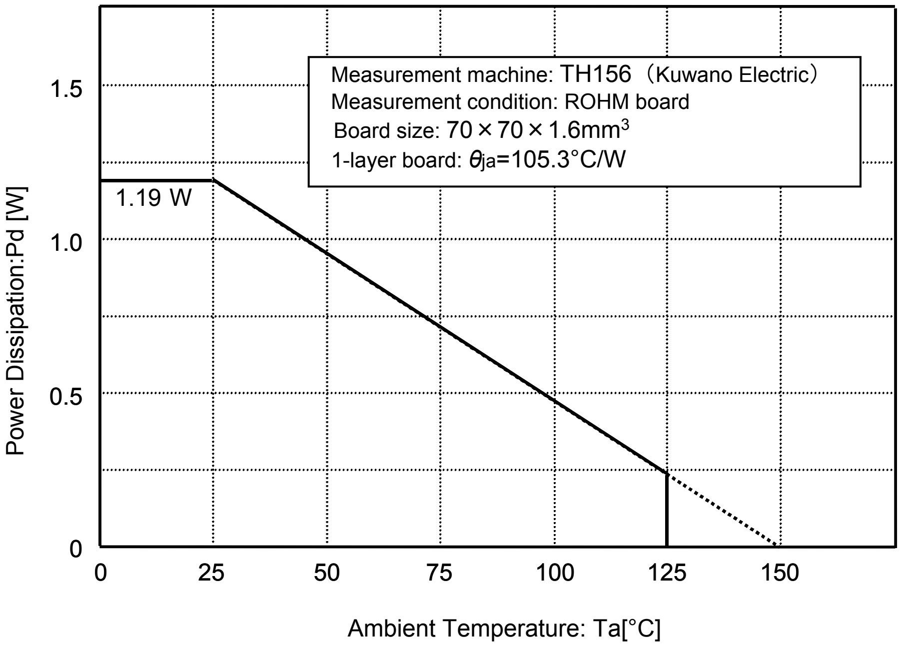
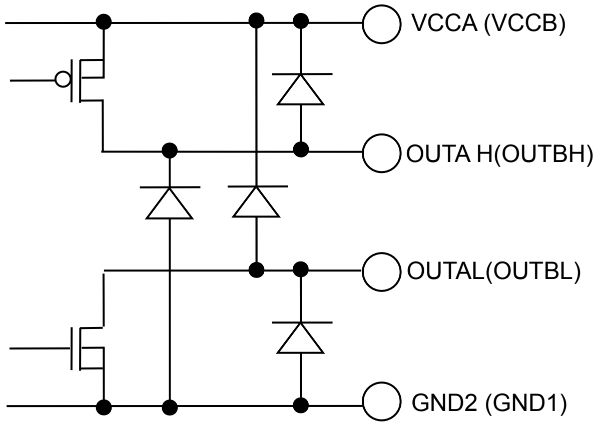
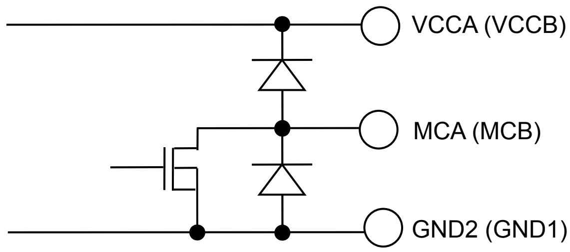
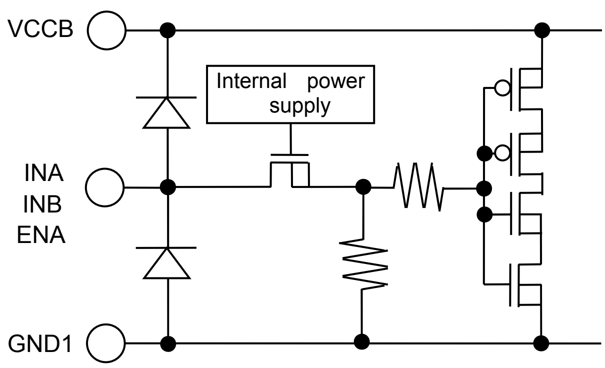


Figure 36. SSOP-B20W Derating Curve

Thermal Design

Please make sure that the IC's chip temperature Tj is not over 150°C, while considering the IC's power consumption (W), package power (Pd) and ambient temperature (Ta). When Tj=150°C is exceeded, the function as a semiconductor will not operate and some problems (ex. Abnormal operation of various parasitic elements and increasing of leak current) occur. Constant use under these circumstances leads to deterioration and eventually IC may destruct. Tjmax=150°C must be strictly followed under all circumstances.

I/O Equivalent Circuits

<table>
<tr><th>Pin No</th><th>Name
Function</th><th>I/O equivalence circuits</th></tr>
<tr><td rowspan="2">6</td><td>OUTAH</td><td rowspan="8"></td></tr>
<tr><td>High-side Output pin (Source)</td></tr>
<tr><td rowspan="2">5</td><td>OUTAL</td></tr>
<tr><td>High-side Output pin (Sink)</td></tr>
<tr><td rowspan="2">17</td><td>OUTBH</td></tr>
<tr><td>low-side Output pin (Source)</td></tr>
<tr><td rowspan="2">18</td><td>OUTBL</td></tr>
<tr><td>low-side Output pin (Sink)</td></tr>
<tr><td rowspan="2">4</td><td>MCA</td><td rowspan="4"></td></tr>
<tr><td>High-side Output pin for Miller Clamp</td></tr>
<tr><td rowspan="2">19</td><td>MCB</td></tr>
<tr><td>low-side Output pin for Miller Clamp</td></tr>
<tr><td rowspan="2">13</td><td>INA</td><td rowspan="6"></td></tr>
<tr><td>Logic input for high side gate driver output</td></tr>
<tr><td rowspan="2">14</td><td>INB</td></tr>
<tr><td>Logic input for low side gate driver output</td></tr>
<tr><td rowspan="2">12</td><td>ENA</td></tr>
<tr><td>Input enabling signal input pin</td></tr>
</table>

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

4. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

5. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

10. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

11. Regarding Input Pins of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

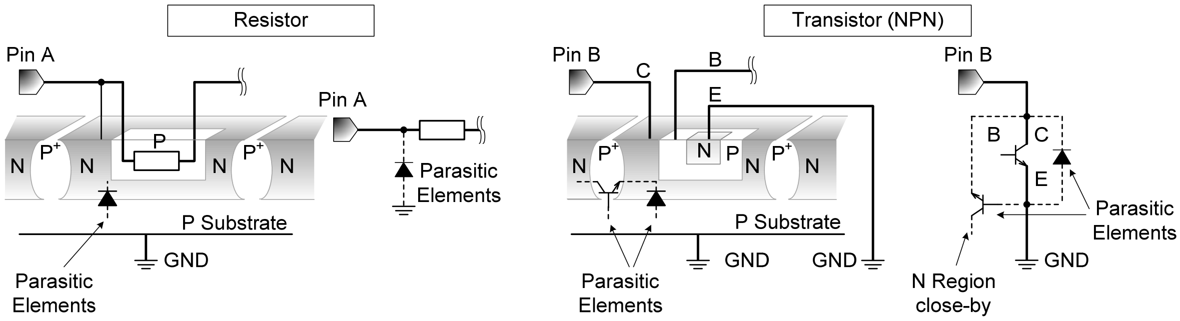


Figure 37. Example of IC structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

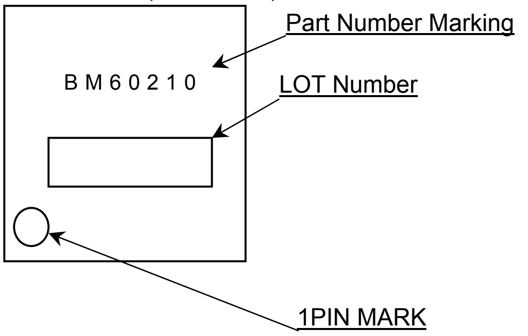
Ordering Information

B M 6 0 2 1 0 F V - CE 2

- Part Number
- Package
  FV: SSOP-B20W
- Rank
  C for Automotive applications
  Packaging and forming specificationE2:
  Embossed tape and reel

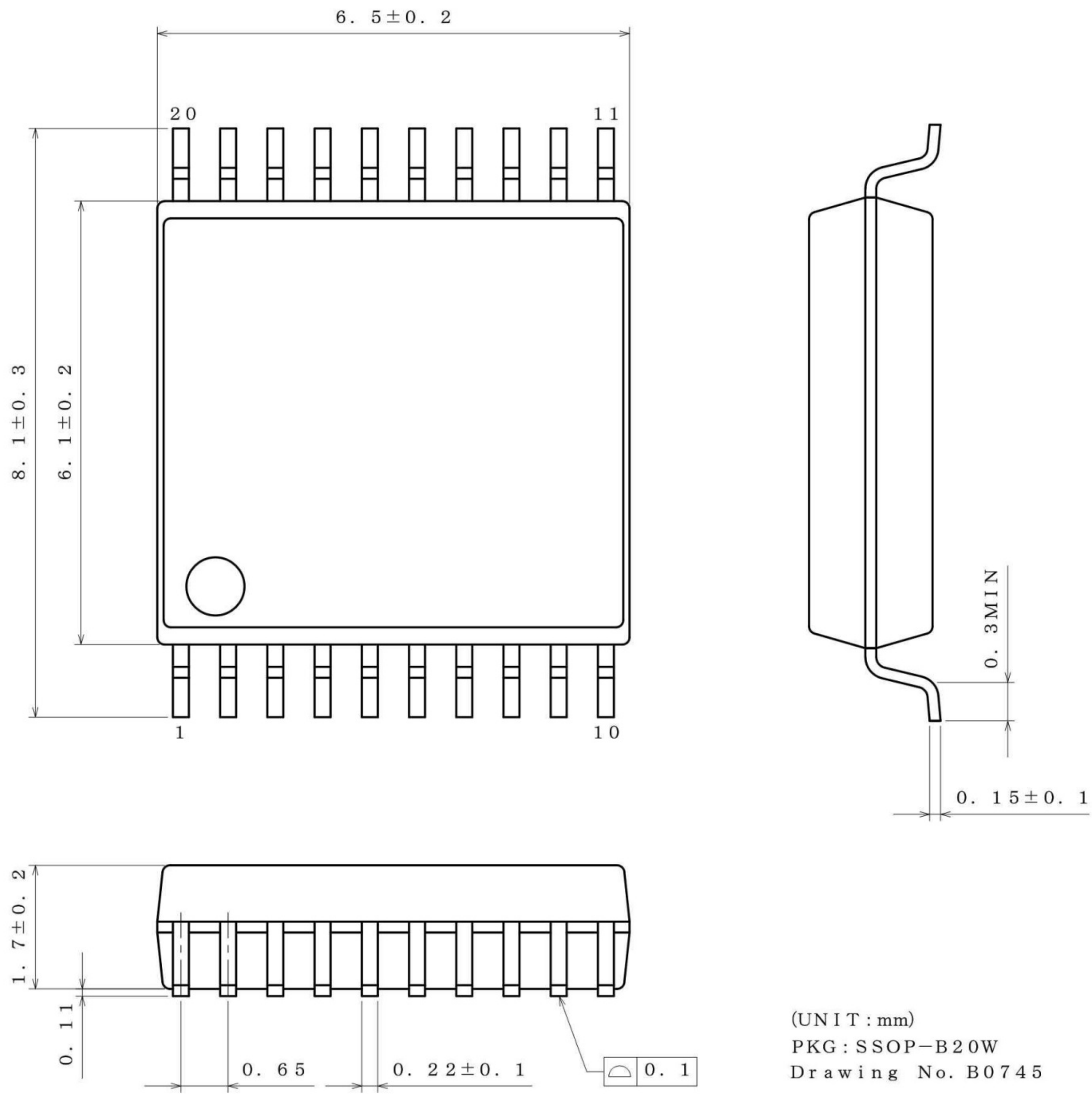
Marking Diagram

SSOP-B20W(TOP VIEW)



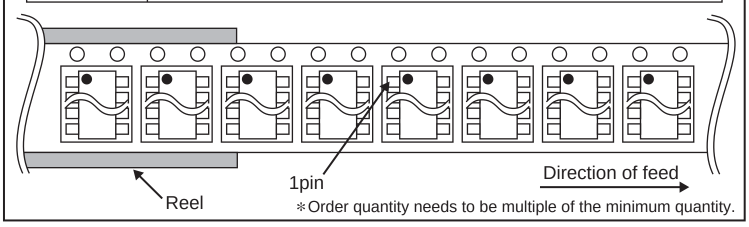
Physical Dimension, Tape and Reel Information

Package Name	SSOP-B20W



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



＊Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
19.Feb.2016	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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Precaution for Disposition

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BM60210FV-C - Web Page

Part Number	BM60210FV-C
Package	SSOP-B20W
Unit Quantity	2000
Minimum Package Quantity	2000
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes