

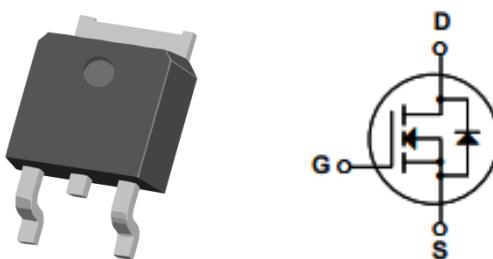
## Description

This N-channel MOSFETs use advanced trench technology and design to provide excellent RDS(on) with low gate charge. It can be used in a wide variety of applications.

## Features

BVDSS	RDS(on)	ID
200V	0.6Ω	5.0A

- 1) Low gate charge.
- 2) Green device available.
- 3) Advanced high cell density trench technology for ultra RDS(ON)
- 4) Excellent package for good heat dissipation.



TO-252

## Absolute Maximum Ratings $T_c=25^\circ\text{C}$ ,unless otherwise noted

Symbol	Parameter	Ratings	Units
VDS	Drain-Source Voltage	200	V
VGS	Gate-Source Voltage	±20	V
ID	Continuous Drain Current-1	5.0	A
	Continuous Drain Current-T=100°C	3.5	
	Pulsed Drain Current2	20	
EAS	Single Pulse Avalanche Energy3	—	mJ
PD	Power Dissipation4	43	W
TJ, TSTG	Operating and Storage Junction Temperature Range	-55 to +175	°C

## Thermal Characteristics

Symbol	Parameter	Ratings	Units
$\theta_{JC}$	Thermal Resistance ,Junction to Case1	—	°C/W
$\theta_{JA}$	Thermal Resistance, Junction to Ambient1	—	°C/W

## Package Marking and Ordering Information

Part NO.	Marking	Package
KSMD220N	KSMD220N0	TO-252

## Electrical Characteristics $T_c=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{DS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	200	—	—	V
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{\text{DS}}=0\text{V}, V_{\text{GS}}=32\text{V}$	—	—	25	$\mu\text{A}$
$I_{\text{GSS}}$	Gate-Source Leakage Current	$V_{\text{DS}}=\pm20\text{V}, V_{\text{GS}}=0\text{A}$	—	—	$\pm100$	nA
<b>On Characteristics</b>						
$V_{\text{GS}(\text{th})}$	GATE-Source Threshold Voltage	$V_{\text{DS}}=V_{\text{DS}}, I_{\text{D}}=250\mu\text{A}$	2.0	—	4.0	V
$R_{\text{DS}(\text{ON})}$	Drain-Source On Resistance <sup>2</sup>	$V_{\text{DS}}=10\text{V}, I_{\text{D}}=6\text{A}$	—	—	0.6	$\Omega$
		$V_{\text{DS}}=2.5\text{V}, I_{\text{D}}=5\text{A}$	—	—	—	
$G_{\text{FS}}$	Forward Transconductance	$V_{\text{DS}}=5\text{V}, I_{\text{D}}=12\text{A}$	2.6	—	—	S
<b>Dynamic Characteristics</b>						
$C_{\text{iss}}$	Input Capacitance	$V_{\text{DS}}=15\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$	—	300	—	pF
$C_{\text{oss}}$	Output Capacitance		—	53	—	
$C_{\text{rss}}$	Reverse Transfer Capacitance		—	15	—	
<b>Switching Characteristics</b>						
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	$V_{\text{DS}}=20\text{V}, V_{\text{GS}}=10\text{V}, R_{\text{GEN}}=3.3\Omega$	—	6.4	—	ns
$t_{\text{r}}$	Rise Time		—	11	—	ns
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time		—	20	—	ns
$t_{\text{f}}$	Fall Time		—	12	—	ns
$Q_{\text{g}}$	Total Gate Charge	$V_{\text{GS}}=4.5\text{V}, V_{\text{DS}}=20\text{V}, I_{\text{D}}=6\text{A}$	—	15	23	nC
$Q_{\text{gs}}$	Gate-Source Charge		—	2.4	3.6	nC
$Q_{\text{gd}}$	Gate-Drain "Miller" Charge		—	6.1	9.2	nC
<b>Drain-Source Diode Characteristics</b>						
$V_{\text{SD}}$	Source-Drain Diode Forward Voltage <sup>2</sup>	$V_{\text{GS}}=0\text{V}, I_{\text{S}}=1\text{A}$	—	—	1.3	V
$t_{\text{rr}}$	Reverse Recovery Time	$I_{\text{F}}=7\text{A}, di/dt=100\text{A}/\mu\text{s}$	—	90	140	ns
$Q_{\text{rr}}$	Reverse Recovery Charge		—	320	480	nC

Notes:

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board 2OZ copper.
2. The data tested by pulse width≤300us,duty cycle≤2%
3. The EAS data shows Max.rating.The test condition is V<sub>DD</sub>=25v,V<sub>GS</sub>=10V,L=0.1mH,i<sub>AS</sub>=17.8A
4. The power dissipation is limited by 150°C junction temperature.

**Typical Characteristics**  $T_J=25^\circ\text{C}$  unless otherwise noted

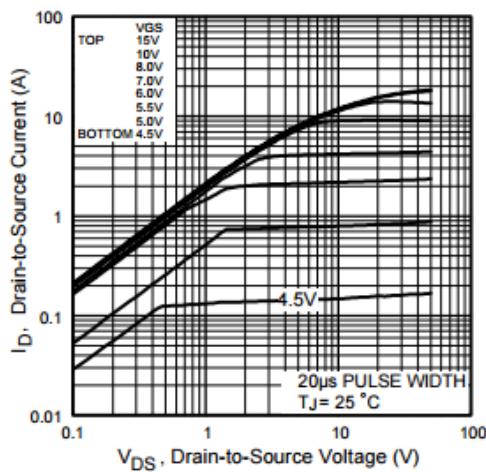


Fig 1. Typical Output Characteristics

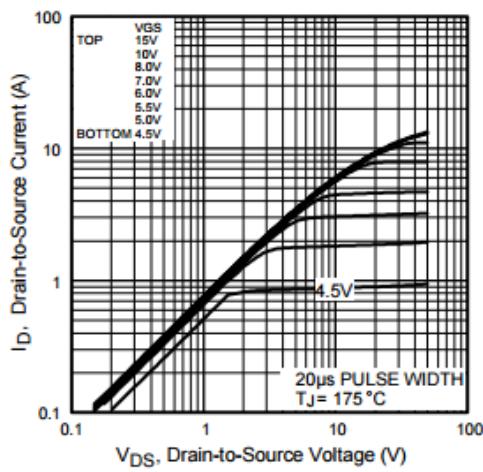


Fig 2. Typical Output Characteristics

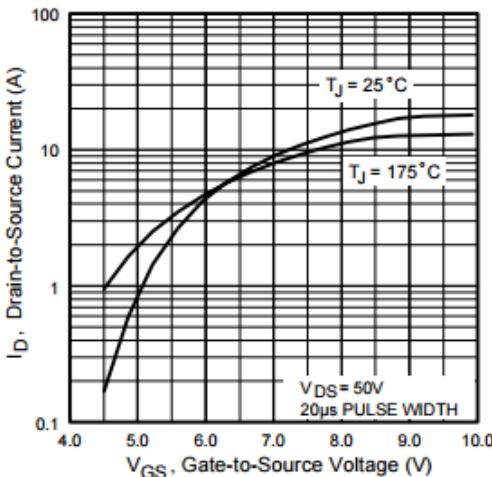


Fig 3. Typical Transfer Characteristics

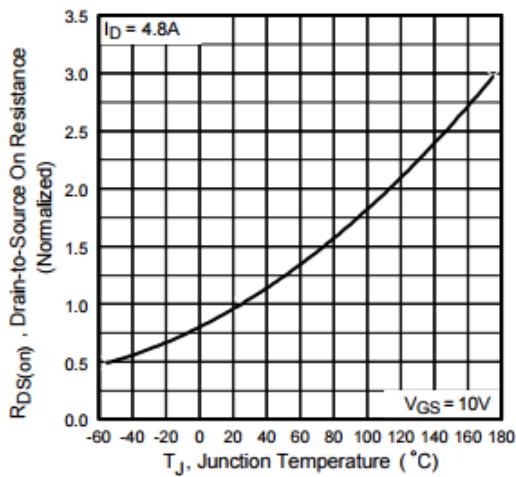
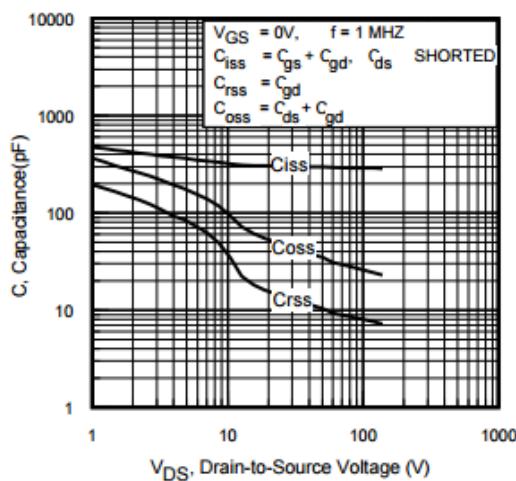
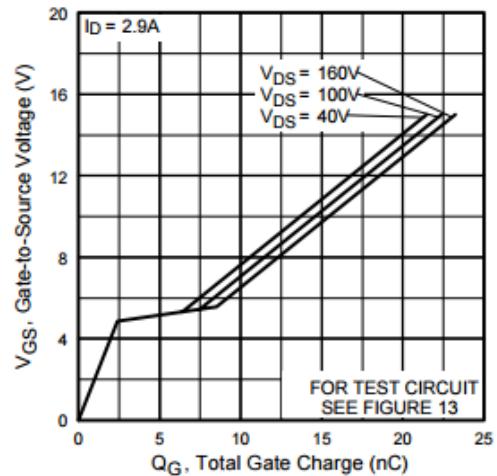


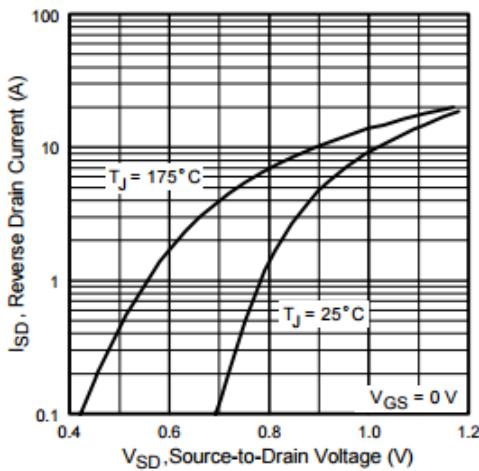
Fig 4. Normalized On-Resistance Vs. Temperature

**KERSMI ELECTRONIC CO.,LTD.**
**200V N-channel MOSFET**


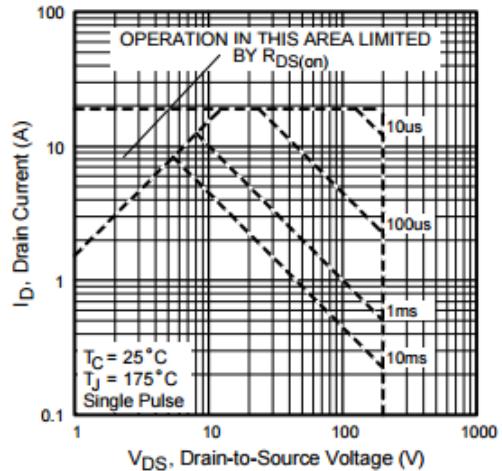
**Fig 5. Typical Capacitance vs.  
Drain-to-Source Voltage**



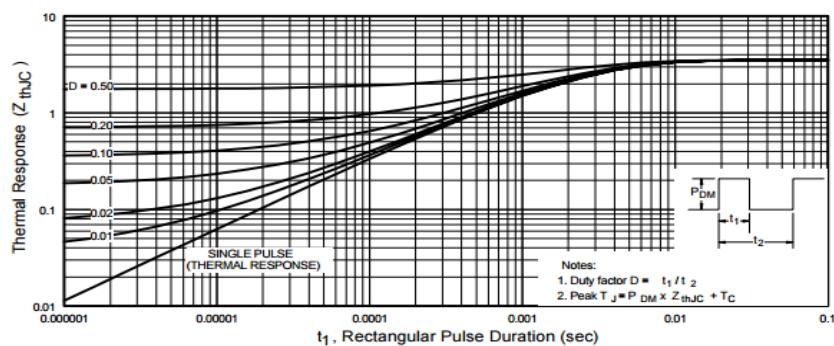
**Fig 6. Typical Gate Charge vs.  
Drain-to-Source Voltage**



**Fig 7. Typical Source-Drain Diode  
Forward Voltage**



**Fig 8. Maximum Safe Operating Area**



**Fig 9. Maximum Effective Transient Thermal Impedance, Junction-to-Case**