ROHM GROUP
LAPIS SEMICONDUCTOR

FEDL7066-01
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ML7066

400MHz Transceiver IC for Specified Low-Power Station

General Description

The ML7066 is an transceiver IC that can be used for specified low-power statiom , where the RF section, IF section, modem section and HOST interface section are integrated into one chip. It supports the 400MHz radio communication and complies with RCR STD-30 (426MHz) and ARIB STD-T67 (429MHz). The ML7066 is suitable for auto meter reading, home securithy systems, wireless fire alarm system, and industorial monitoring and control.

Features

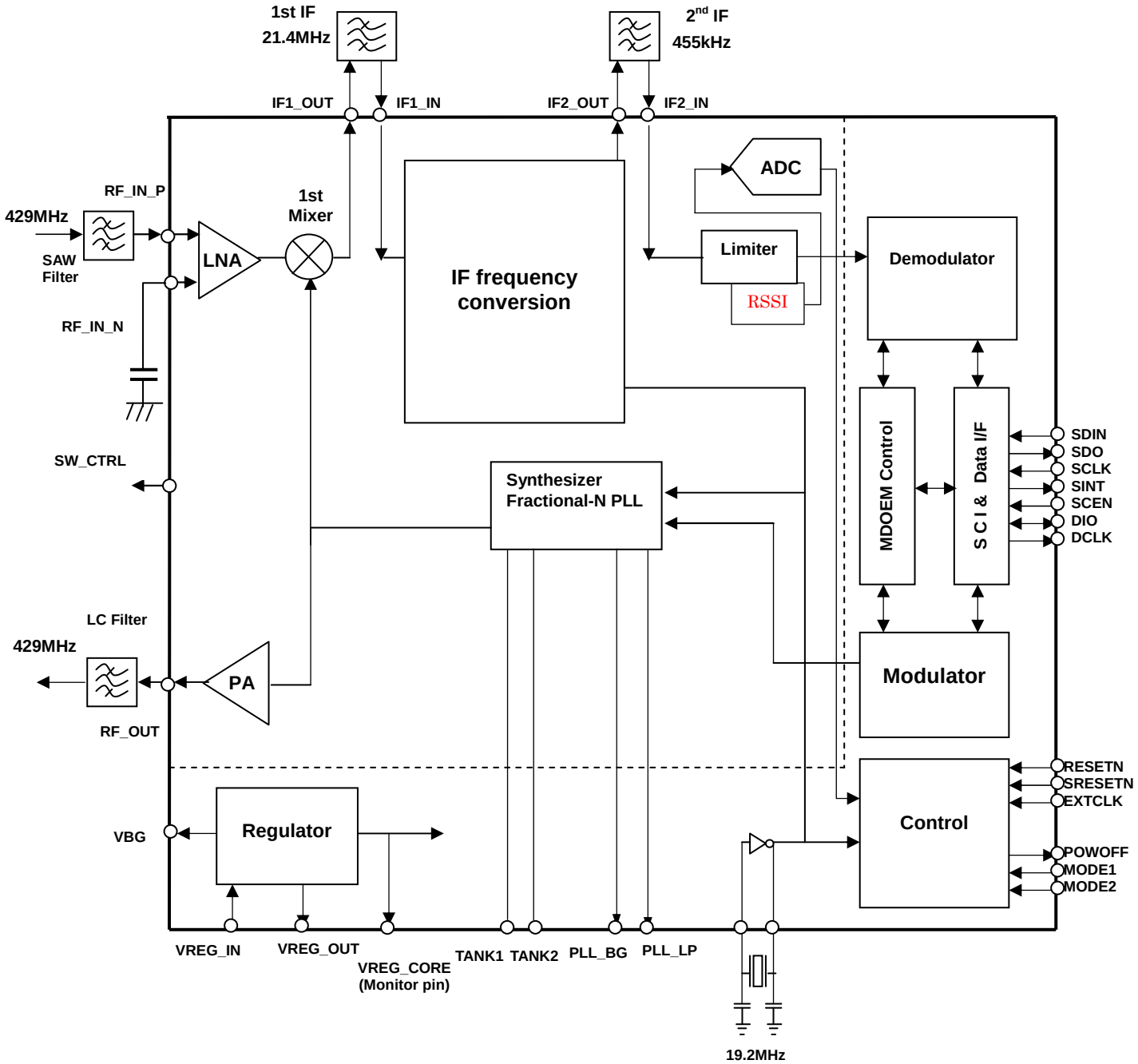
- Complies with RCR STD-30 (low-power radio security system) and ATIB STD-T67 (specified low-power radio statiion)
- Operating Frequency 426.0250 MHz to 426.8375 MHz
  429.1750 MHz to 429.9250 MHz
  Note: Including the frequency range that are not defined in the standards.
- Data transfer speed 1200 bps, 2400 bps and 4800 bps with NRZ coding
  600 bps, 1200 bps and 2400 bps with Manchester coding
- 2-FSK modulation
- Voltage regulator installed
- 19.2 MHz oscillator circuit installed
- Synchronous communication interface (SCI) installed
- Up to 8 oeration channel set function installed
- Carrier (0perating frequency) detect function installed
- Up to 16 bytes preamble generator and detecor installed
- Up to 18 bytes start-of-frame delimiter generator and detector installed
- Intermittent operation function installed (periodic transmition and receiving)
- PLL adjustment function availble to use 60ppm crystal
- Test pattern generatot installed (CW, PN9, PN15, all “0”, all”1”)

- Power supply voltage 2.1V to 3.6V
- Current consumption in the following states (typical);

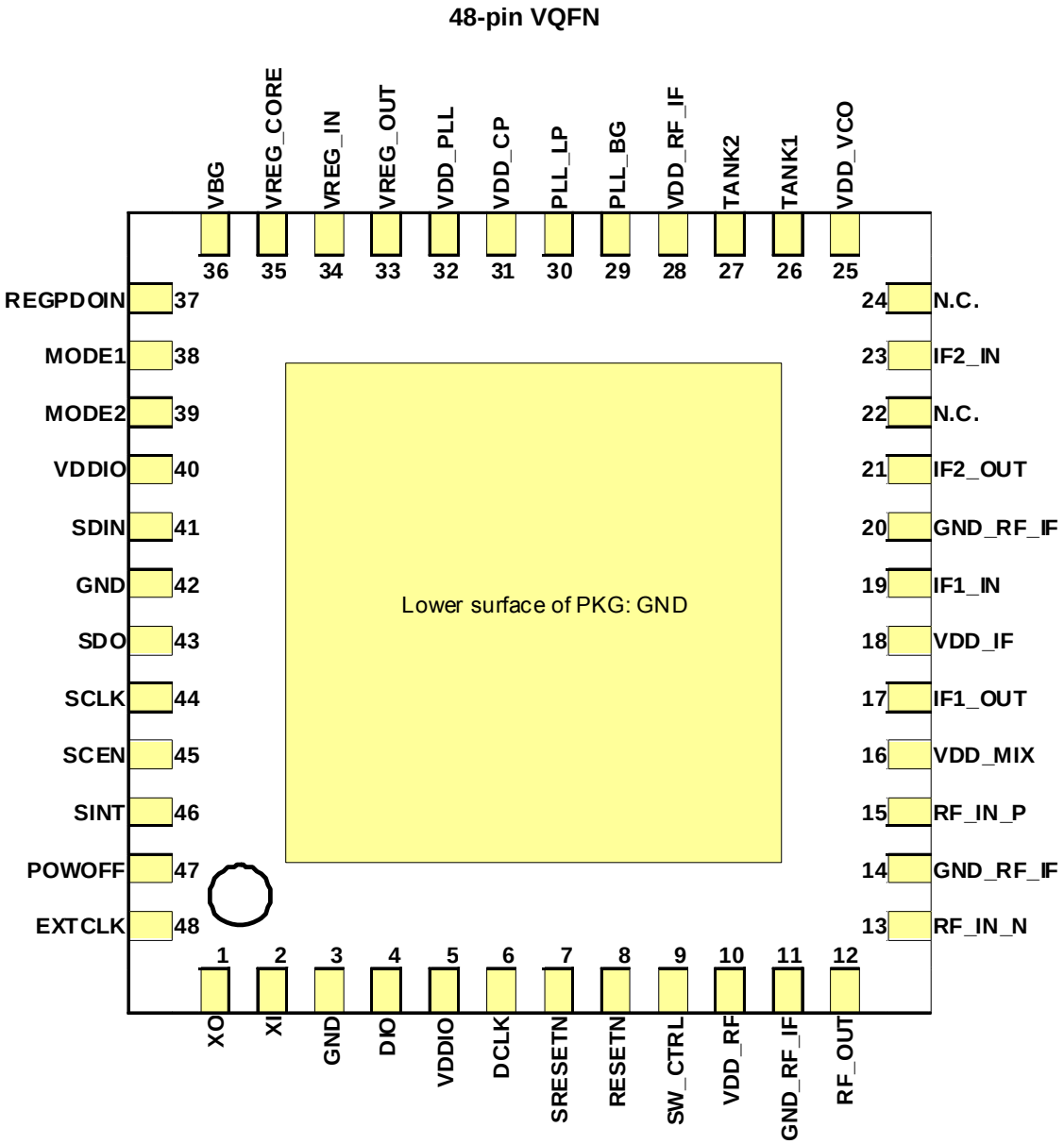
Stop mode:	0.7 uA
Sleep mode:	4 uA
Idle mode:	2 mA
At transmission (@10mW)	29.5 mA
At reception:	15.5 mA

- Package
  48-pin VQFN P-VQFN48-0707-0.50-T6 Product name: ML7066GDZ0AB
- Package
  Lead-free package conforming to RoHS

Block Diagram



Pin Configuration



Top View

Description of Pins

I/O definition

I_{RF}	:	RF input pin
I_A	:	Analog input pin
I	:	Digital input pin
I_S	:	Schmitt trigger input pin
I_U	:	Input pin with pull-up register
I_D	:	Input pin with pull-down register
I_{OS}	:	Input pin for 24MHz oscillation circuit
O_{RF}	:	RF control output pin
O_A	:	Analog output pin
O	:	Digital output pin
O_{OS}	:	Output pin for 24MHz oscillation circuit
O_D	:	Open drain output pin

RF Related Pins

Pin No.	Pin Name	Attribute/ value at reset	I/O	Active Level	Description
12	RF_OUT	O	O_{RF}	–	RF output pin
13	RF_IN_N	I	I_{RF}	–	Positive RF input pin (differential)
15	RF_IN_P	I	I_{RF}	–	Negative RF input pin (differential)
17	IF1_OUT	O	O_A	–	1st IF filter pin (output to filter)
19	IF1_IN	I	I_A	–	1st IF filter pin (input from filter)
21	IF2_OUT	O	O_A	–	2nd IF filter pin (output to filter)
23	IF2_IN	I	I_A	–	2nd IF filter pin (input from filter)
29	PLL_BG	O	O_A	–	Loop filter related pin
30	PLL_LP	O	O_A	–	Loop filter pin
26	TANK1	I	I_A	–	VCO tank inductor pin 1
27	TANK2	I	I_A	–	VCO tank inductor pin 2

Host Interface Pins

Pin No.	Pin Name	Attribute/ value at reset	I/O	Active Level	Description
41	SDIN	I	I	H or L	Synchronous communication interface data input pin
43	SDO	L	O	H or L	Synchronous communication interface data output pin
44	SCLK	I	I	P or N	Synchronous communication interface clock input pin
46	SINTN	H	O	L	Synchronous communication interface interrupt output pin
45	SCEN	I	I_U	L	Synchronous communication interface chip select input pin

TX/RX Data Related Pins

Pin No.	Pin Name	Attribute/ value at reset	I/O	Active Level	Description
4	DIO	I	IO	H or L	Data input/output pin (Initial value is Low when switch the state from input to output)
6	DCLK	L	O	P or N	Data clock output pin

Regulator Related Pins

Pin No.	Pin Name	Attribute/ value at reset	I/O	Active Level	Description
33	VREG_OUT	–	–	–	Power supply output pin for the RF block (Typ. 2.2V) Do not use this pin for purposes other than RF power supply.
35	VREG_CORE	–	–	–	Power supply monitor pin for the core (Typ. 2.2V) Do not use this pin for purposes other than monitoring purpose. Decuple this pin to ground with capacitor. (*1)
36	VBG	–	–	–	Back bias pin (Capacitance connection) Decuple this pin to ground with capacitor. (*1)
37	REGPDIN	L	ID	–	Regulator power down pin Always fix this pin to “L” input in normal operation.

*1: Please refer reference circuit.

Power Supply Pins

Pin No.	Pin Name	Attribute/ value at reset	I/O	Active Level	Description
34	VREG_IN	–	–	–	Power supply pin for regulator. (Typ. 3.0 V)
10	VDD_RF	–	–	–	Power supply pin for PA and LNA. Connect to VREG_OUT. (Typ. 2.2V).
25	VDD_VCO	–	–	–	Power supply pin for VCO. Connect to VREG_OUT. (Typ. 2.2V)
16	VDD_MIX	–	–	–	Power supply pin for mixer 1. Connect to VREG_OUT. (Typ. 2.2V)
31	VDD_CP	–	–	–	Power supply pin for charge pump. Connect to VREG_OUT. (Typ. 2.2V)
32	VDD_PLL	–	–	–	Power supply pin for PLL. Connect to VREG_OUT. (Typ. 2.2V)
18	VDD_IF	–	–	–	Power supply pin for IF, Limiter and RSSI. Connect to VREG_OUT. (Typ. 2.2V)
5, 40	VDDIO	–	–	–	Power supply pins for the digital I/O block and internal voltage regulator. (Typ. 3.0 V).
11, 14 20,28	GND_RF_IF	–	–	–	Ground pin for RF and IF block.
3,42	GND	–	–	–	Ground pin for digital block.
EL (*2)	–	–	–	–	Ground pin

(*2) EL is the lower surface of the LSI.

Other Pins

Pin No.	Pin Name	Attribute/ value at reset	I/O	Active Level	Description
8	RESETN	I	IS	L	Hardware reset pin
7	SRESETN	I	IU	L	Software reset pin Wake up pin when in sleep mode. This pin is active when RESETN=1.
2	XI	I	IOS	P or N	19.2 MHz crystal connection pin 1 External clock input pin.
1	XO	O	OOS	–	19.2 MHz crystal connection pin 2 Leave open when XI (pin #2) is configured as an external clock input pin.
9	SW_CTRL	O	OD	L	Antenna switch control pin L: In transmitting mode HiZ: In receiving mode
47	POWOFF	L	O	H	External component power on/off control pin Active level polarity is changeable by register setting.
48	EXTCLK	I	I	P or N	External 32.768 kHz clock input pin (*3)
38	MODE1	I	IO	H or L	Bit order on SCI Data setting pin L: LSB first H: MSB first
39	MODE2	I	I	H or L	Operation mode setting pin L: Normal mode H: Test mode Always fix this pin to “L” input in normal operation.
22,24	NC	O	OA	–	Unused. (Open)

(*3) Always EXTCLK input is required for ML7066 operation.

Recommended Handling of Unused Pins

LAPIS Semiconductor recommends handling unused pins as shown below so that the basic operation of the ML7275 is unimpaired.

Pin No.	Pin Name	Recommended pin handling
1	XO	Open (when XI is configured as an external clock input pin.)
7	SRESETN	Connect to VDDIO
47	POWOFF	Open

NOTE

If any input pins are left open, the current consumption may increase. Therefore, it is recommended that the unused input ports and I/O ports be always fixed with “L” or “H” input.

List of Command/Event

The following table shows the command/event specifications of ML7066. Command is send from MCU to the ML7066. Event is send from the ML7066 to MCU.

Command/event name	Type	code	Function
SET_TRX_STATE.request	Command	0x02	Requests the RF state change
SET_TRX_STATE.confirm	Event	0x03	Reports the result of RF state change request
SET_CHANNEL.request	Command	0x04	Sets the operating channel
SET_CHANNEL.confirm	Event	0x05	Reports the channel setting result
SET_CMP_DATA.request	Command	0x06	Sets the preamble or start-of-frame delimiter (SFD) pattern for generation (TX) and comparison (RX)
SET_CMP_DATA.confirm	Event	0x07	Reports the preamble/SFD pattern setting result
SET_RSSI_SETTING.request	Command	0x08	Sets the carrier detect condition
SET_RSSI_SEETING.confirm	Event	0x09	Reports the carrier detect condition setting result
SET_TX_POW.request	Command	0x0a	Sets the transmitting power
SET_TX_POW.confirm	Event	0x0b	Reports the transmitting power setting result
SET_TIMER.request	Command	0x0c	Sets the intermitting operation timing
SET_TIMER.confirm	Event	0x0d	Reports the intermittent operation setting result
SET_PLL_FIT.request	Command	0x0e	Adjusts the operating channel center frequency
SET_PLL_FIT.confirm	Event	0x0f	Reports the result of frequency adjustment request
SET_TEST.request	Command	0x10	Sets the test pattern
SET_TEST.confirm	Event	0x11	Reports the result of test pattern setting results
SET_CLK.request	Command	0x12	Requests the sleep mode operation and POWOFF pin polarity change.
SET_CLK.confirm	Event	0x13	Reports the result of sleep and POWOFF pin polarity request
SET_RESET.request	Command	0x14	Request the reset operation
SET_RESET.confirm	Event	0x15	Reports the result of reset request
SET_CONFIRM.request	Command	0x16	Requests the interrupt masking
SET_CONFIRM.confirm	Event	0x17	Reports the interrupt mask requests
SET_INT.request	Command	0x18	Requests the .confirm event masking
SET_INT.confirm	Event	0x19	Reports the result of .confirm event mask requests
SET_SPD.request	Command	0x18	Sets the data rate
SET_SPD.confirm	Event	0x19	Reports the data rate setting request
SET_CMP_DURATION.request	Command	0x0e	Sets the comparing receive data period
SET_CMP_DURATION.confirm	Event	0x0f	Reports the comparing period setting result
RX_DATA.indication	Event	0x20	Notices existing receive data
RSSI.indication	Event	0x21	Notices RSSI result
GET_TRX_STATE.request	Command	0x22	Reads the RF state report
GET_TRX_STATE.confirm	Event	0x23	Reports the current RF state
GET_CHANNEL.request	Command	0x24	Reads the channel setting
GET_CHANNEL.confirm	Event	0x25	Reports the setting operation channel(s)
GET_CMP_DATA.request	Command	0x26	Reads the setting of the preamble or SFD pattern
GET_CMP_DATA.confirm	Event	0x27	Reports the setting pattern of preamble or SFD
GET_RSSI_SETTING.request	Command	0x28	Reads the carrier detect setting or current RSSI
GET_RSSI_SEETING.confirm	Event	0x29	Reports the carrier detect setting or current RSSI
GET_TX_POW.request	Command	0x2a	Reads the transmitting power setting
GET_TX_POW.confirm	Event	0x2b	Reports the setting value of transmitting power
GET_TIMER.request	Command	0x2c	Reads the intermitting operation timing
GET_TIMER.confirm	Event	0x2d	Reports the setting value of intermittent operation
GET_PLL_FIT.request	Command	0x2e	Reads the PLL adjust value
GET_PLL_FIT.confirm	Event	0x2f	Reports the setting value for PLL adjustment

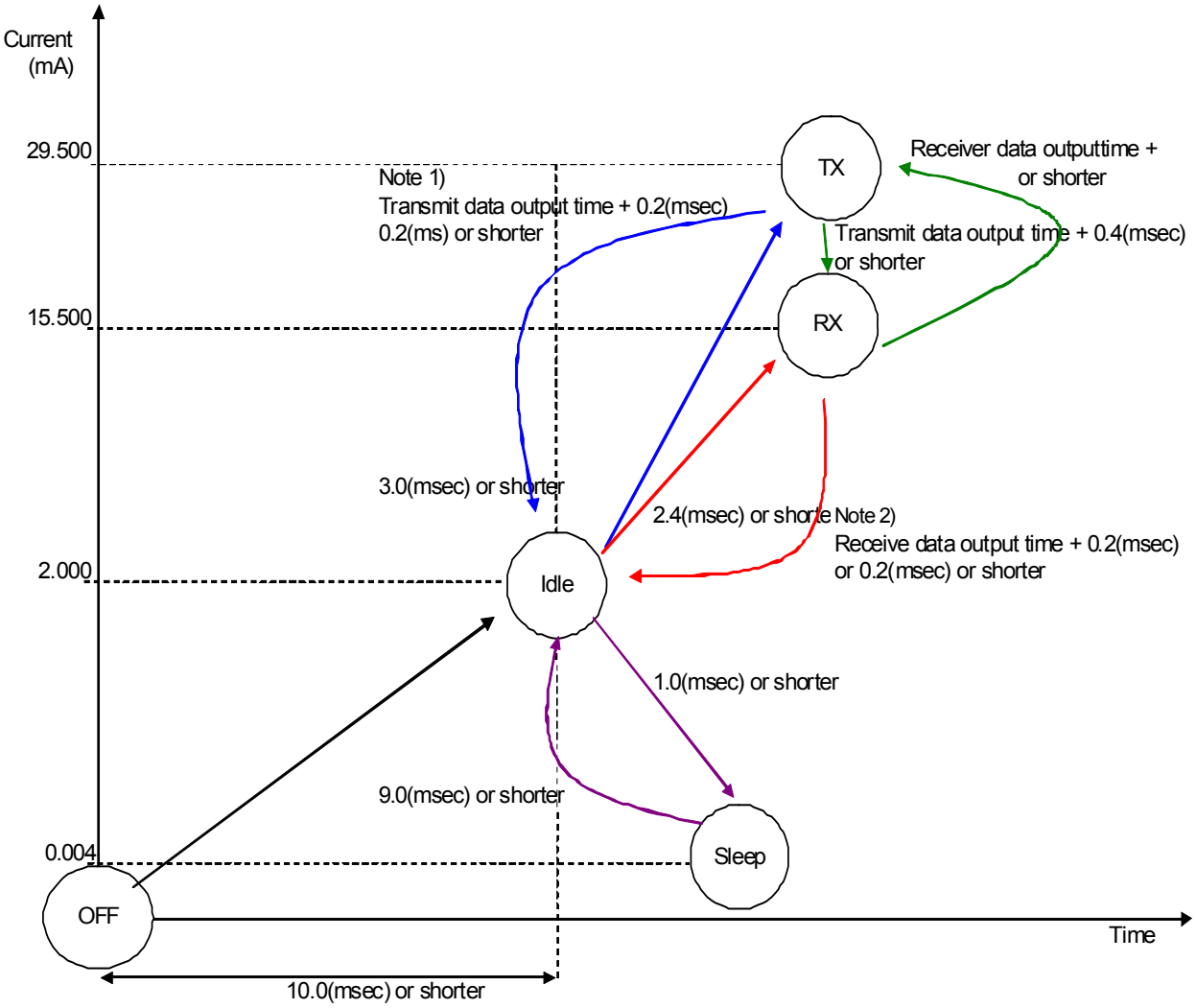
Command/event name	Type	code	Function
GET_TEST.request	Command	0x30	Reads the test pattern setting
GET_TEST.confirm	Event	0x31	Reports the setting of test pattern
GET_CLK.request	Command	0x32	Reads the POWOFF pin polarity setting
GET_CLK.confirm	Event	0x33	Reports the setting polarity of POWOFF pin
GET_INT.request	Command	0x34	Reads the .confirm event mask setting
GET_INT.confirm	Event	0x35	Reports the setting of .confirm event mask
GET_CONFIRM.request	Command	0x36	Reads the interrupt mask setting
GET_CONFIRM.confirm	Event	0x37	Reports the setting of interrupt mask
INT.indication	Event	0x38	Notices interrupt occurs
GET_SPD.request	Command	0x3a	Reads the data rate
GET_SPD.confirm	Event	0x3b	Reports the data rate setting
GET_CMP_DURATION.request	Command	0x0e	Reads the comparing period setting
GET_CMP_DURATION.confirm	Event	0x0f	Reports the setting value of comparing period
GET_ERRR_COUNTER.request		0x3e	Reads the receiving error status of operating channels
GET_ERR_COUNTER.confirm		0x3f	Reports the receiving data status of operating channels

List of Confirm

Code	Function	Note
0x05	INVALID_PARAMETER	INVALID_PARAMETER
0x06	RX_ON	RX_ON request when in RX_ON state
0x07	SUCCESS	Request accepted
0x08	TRX_OFF	TRX_OFF request when in TRX_OFF state
0x09	TX_ON	TX_ON request when in TX_ON state
0x0a	UNSPOORTED_STTRIBUTE	Data overrun or shortage

ML7066 State Diagram

The following figure shows the state transition time and the consumption current from power-on to each power state (Sleep, Idle, RX, TX) .



Note 1:
For the TRX_OFF instruction, the Idle state comes 0.2ms after the data transmission from ML7066 is completed.
For the FORCE_TRX_OFF instruction, it comes 0.2ms after the instruction is received.
Note 2:
For the TRX_OFF instruction, the Idle state comes 0.2ms after the time when the unreceived data from ML7066 reduces to the last one byte.
For the FORCE_TRX_OFF instruction, it comes 0.2ms after the instruction is received.

Notes on Operation

This section describes the notes on using the ML7066.

1) Initial settings

Initial settings are required for optimization of the RF characteristics. Perform the following **ML7066 initial settings** after reset.

ML7066 Initial Settings

No.	Direction	Type	Command	Data	SCI format
1	ML7066 → MCU	Confirm	0x15	0x07	SDO: 0C 02 15 07
2	MCU → ML7066	Request	0x5F	0x8888	SDI: 08 03 5F 88 88
3	MCU → ML7066	Request	0x42	0x2111	SDI: 08 03 42 11 21
4	MCU → ML7066	Request	0x40	0xB587	SDI: 08 03 40 87 B5
5	MCU → ML7066	Request	0x41	0x82E9	SDI: 08 03 41 E9 82
6	MCU → ML7066	Request	0x47	0x0883	SDI: 08 03 47 83 08
7	MCU → ML7066	Request	0x43	0xFE01	SDI: 08 03 43 01 FE
8	MCU → ML7066	Request	0x45	0x0020	SDI: 08 03 45 20 00
9	MCU → ML7066	Request	0x02	0x09	SDI: 08 02 02 09
10	ML7066 → MCU	Confirm	0x03	0x07	SDO: 0C 02 03 07
11	MCU → ML7066	Request	0x4D	0x0040	SDI: 08 03 4D 40 00
12	Set 2msec WAIT for MCU.				
13	MCU → ML7066	Request	0x02	0x08	SDI: 08 02 02 08
14	ML7066 → MCU	Confirm	0x03	0x07	SDO: 0C 02 03 07
15	MCU → ML7066	Request	0x45	0x0000	SDI: 08 03 45 00 00
16	MCU → ML7066	Request	0x42	0x2110	SDI: 08 03 42 10 21
17	MCU → ML7066	Request	0x5F	0x0000	SDI: 08 03 5F 00 00

2) Notification from ML7066

If ML7066 state settings cause a mismatch between an instruction and an internal status, a confirmation that is not listed in the data sheet may be notified fairly infrequently. If you receive such a confirmation, simply discard it.

Example) 04_**00** (Confirmation with Length=0)

04_02_02_**02** (SET_TRX_STATE.request never has the data 02)

04_**05**_05_05_05_05_05 (SET_RSSI.indication never has Length=5)

3) Seal

The first and second generations are distinguished by the seal.
The seal of the second generation is ML7066B.

Note that the first generation includes the following restriction.

Restrictions: The timer value set in the SET_TIMER.request command should be 15 seconds or shorter.

4) Regulator

The regulator in ML7066 has a built-in overcurrent protection circuit. The current control is switched between the following two levels, based on the supplied voltage. We have verified that the overcurrent protection circuit can prevent an occurred inrush current from affecting the function and lifetime of ML7066. However, it cannot prevent an inrush current of the charge in bypass capacitors or other parts at power-on alone. You should verify the protection on your implementation.

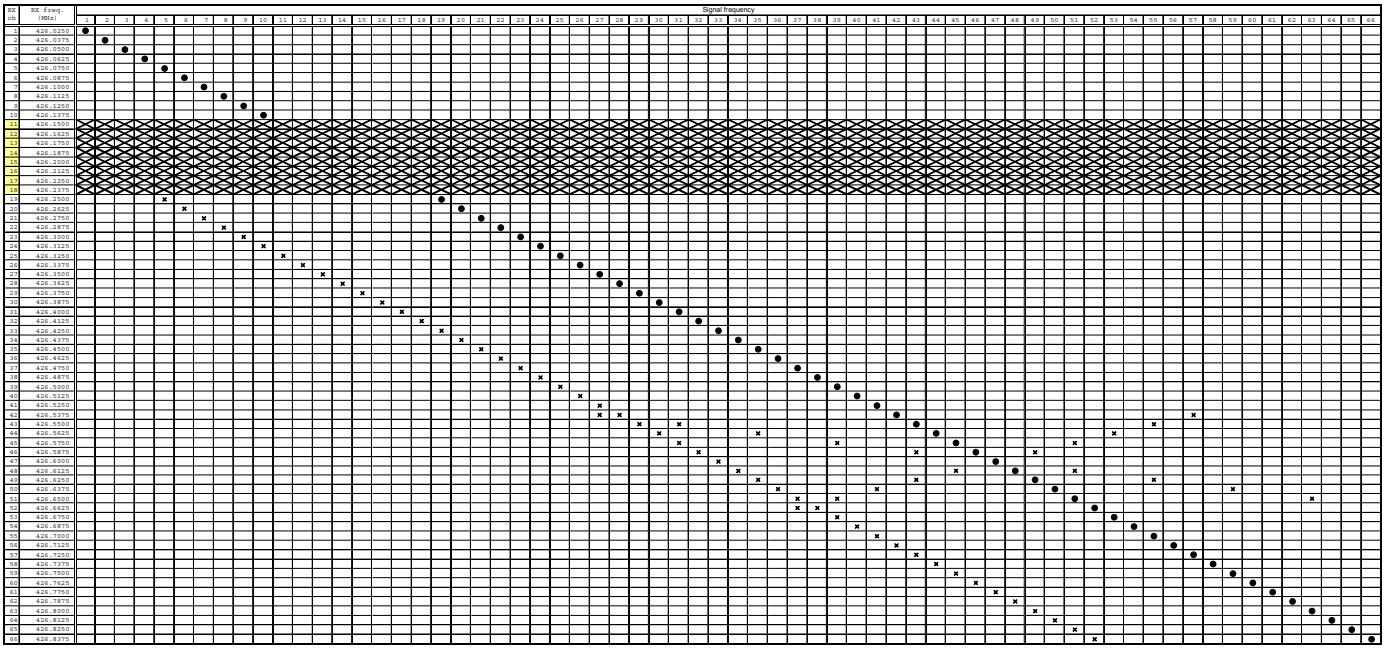
For a low VREG_OUT output voltage (VREG_IN*0.45V or lower): clamped at about 100mA.
For a high VREG_OUT output voltage (VREG_IN*0.45V or higher): clamped at about 500mA.

5) Fractional spurious

ML7066 maintains the accuracy of the RF clock frequency by fine-tuning the PLL oscillation frequency, which helps lower the component cost for generating the master clock. The Fractional-N PLL type is used to realize the fine tuning of the PLL oscillation frequency. We found that this PLL type could cause the fractional spurious depending on the combination of the reference clock, integer dividing ratio, and fractional dividing ratio. So, depending on the combination of the used frequencies (channels), a false detection of the RSSI value can occur. The following matrixes show the channel combinations with a possible false detection.

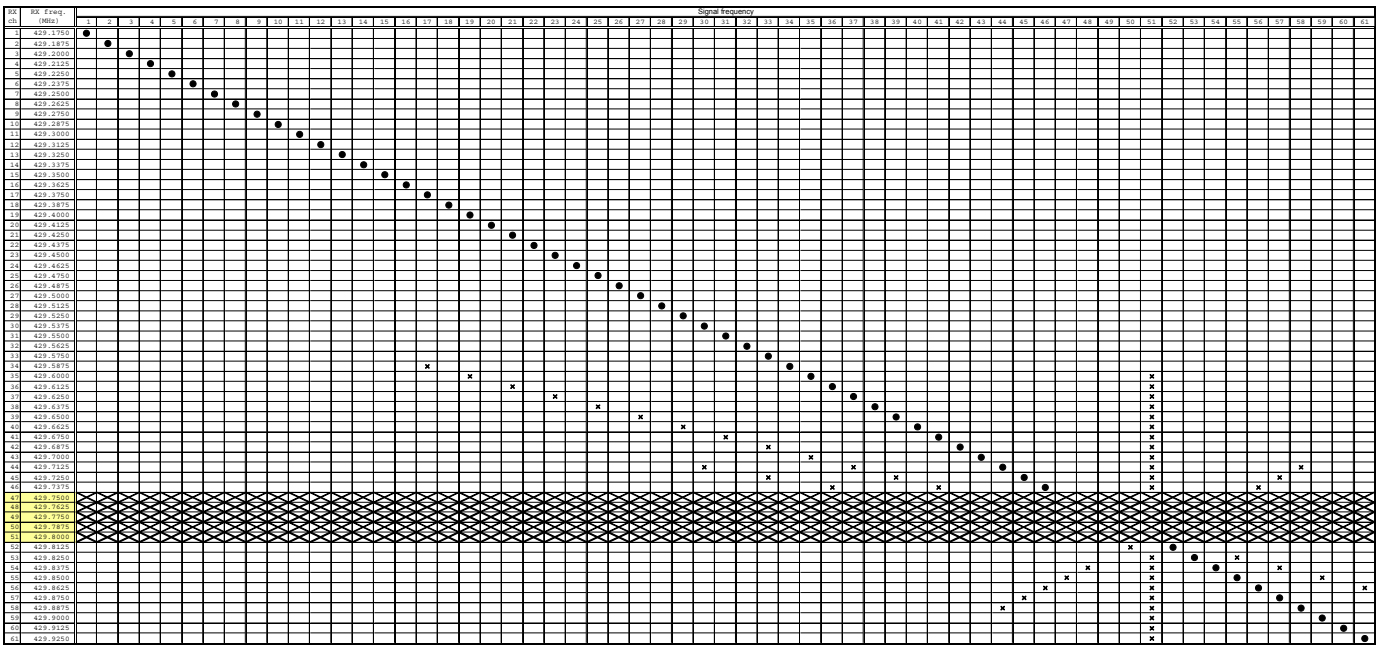
426MHz Band Channel False Detection Matrix

●symbol indicates the combination of the transmission and reception channels by the normal setting.
×symbol indicates the channel combination with a possible false detection.



429MHz Band Channel False Detection Matrix

●symbol indicates the combination of the transmission and reception channels by the normal setting.
×symbol indicates the channel combination with a possible false detection.



Electrical Characteristics

Absolute Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Power supply voltage (I/O) (*1)	V_{DDIO}	Ta=+25°C VSS=0V	-0.3~+4.6	V
Power supply voltage (RF) (*2)	V_{DD_RF}		-0.3~+3.6	V
Regulator input voltage	V_{REGIN}		-0.3~V_{DDIO}+0.3	V
Digital input voltage	V_{DIN}		-0.3~V_{DDIO}+0.3	V
RF input voltage	V_{RFIN}		-0.3~V_{DD_RF}+0.3	V
Analog input voltage	V_{AIN}		-0.3~V_{DDIO}+0.3	V
Regulator output voltage	V_{REGOUT}		-0.3~V_{DD_RF}+0.3	V
Digital output voltage	V_{DO}		-0.3~V_{DDIO}+0.3	V
RF output voltage	V_{RFO}		-0.3~V_{DD_RF}+0.3	V
Analog output voltage	V_{AO}		-0.3~V_{DDIO}+0.3	V
Digital input current	I_{DI}		-10~+10	mA
RF input current	I_{RF}		-2~+2	mA
Analog input current	I_{AI}		-2~+2	mA
Digital output current	I_{DO}		-10~+10	mA
RF output current	I_{RFO}		-2~+2	mA
Analog output current	I_{AO}		-2~+2	mA
Power dissipation	P_d	Ta=+25°C	660	mW
Storage temperature	T_{stg}	—	-55~+150	°C

*1: VDDIO pin
*2: RF power supply pins: VDD_RF, VDD_MIX, VDD_IF, VDD_VCO, VDD_CP, and VDD_PLL pins

Recommneded Operation Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage (I/O)	V_{DDIO}	VDDIO pin (*3)	2.1	3.0	3.6	V
Power supply voltage (RF)	V_{DD_RF}	(*2) (*4) RX	1.95	2.1	2.3	V
		(*2) (*4) TX	1.92	2.1	2.3	V
Regulator input voltage	V_{REGIN}	VREG_IN Pin (*3)	2.1	3.0	3.6	V
Operating temperature	T_a	—	-25	+25	+65	℃
Digital input rise time	T_{IR}	Digital input pins (*5)	—	—	20	ns
Digital input fall time	t_{IF}	Digital input pins (*5)	—	—	20	ns
Digital output load	C_{DL}	All digital output pins	—	—	20	pF
Master clock	F_{MCK}	XI pin (*20)	-4ppm	19.2	+4ppm	MHz
Master clock duty ratio	D_{MCK}	XI pin	45	50	55	%
Sub clock	F_{EXTCLK}	EXTCLK pin (*21)	-80ppm	32.768	+80ppm	kHz
Sub clock duty ratio	D_{EXTCLK}	EXTCLK pin	40	50	60	%
SCI clock input frequency	F_{SCLK}	SCLK pin	0.1	2	8	MHz
SCI clock input duty ratio	D_{SCLK}	SCLK pin	45	50	55	%
RF channel frequency1	F_{RF1}	RF_OUT pin, RF_IN pin 12.5kHz interval	426.0250	—	426.8375	MHz
RF channel frequency2	F_{RF2}	RF_OUT pin, RF_IN pin 12.5kHz interval	429.1750	—	429.9250	MHz

*3: V_{DDIO}=V_{REGIN}

*4: The VREG_OUT pin should be connected to each RF power supply pin.

*5: Applies to the pins that are indicated as I, I_S, I_U in the I/O column in the Pin Descriptions section.

*20: The input clock frequency deviation is shown in the following table.

*21: Reference value. The frequency accuracy of the sub clock only affects timers, and does not matter for the transmit/receive operation.

Table:Example of Input Clock Frequency and Receive Characteristics

Reference clock frequency accuracy	21.4MHz quartz filter (BPF) characteristics	455kHz ceramic filter (BPF) characteristics
±4ppm	±6kHz	±6.0kHz
±10ppm	±6kHz	±7.5kHz
±20ppm	±6kHz	±7.5kHz
±40ppm	±6kHz	±7.5kHz
±60ppm	±6kHz	±7.5kHz

You can use the PLL frequency adjustment function provided in this LSI to support a reference clock frequency with an accuracy worse than ±4ppm. When the accuracy of the reference clock frequency is worse than ±4ppm, you can adjust it to ensure the required frequency accuracy by the PLL frequency adjustment function.
In terms of the receive characteristics, the bandwidth of the external filter should be wide as shown in this table if the accuracy of the source reference clock frequency is worse than ±4ppm, which degrades the C/I characteristics.
In this table, the reference clock frequency accuracy includes the center frequency and the temperature variation.
The temperature variation of the reference clock frequency is uniformly assumed to be ±20ppm.

Current Consumption Specifications

(Operation power supply voltage: V_{DDIO}=V_{REGIN}=2.1V - 3.6V, Ta=-25 - +65°C)

Item	Symbol	Condition	Min.	Typ. (*7)	Max.	Unit
Current consumption (*6)	I_{DDS}	Total-stop state	—	0.7	—	µA
	I_{DD1}	Sleep state	—	4	—	µA
	I_{DD3}	Idle state	—	2	—	mA
	I_{DD4}	Receiving state (*8)	—	15.5	—	mA
	I_{DD5}	Transmitting state (*8)	—	29.5	—	mA

*6: The current consumption is the total current of the RF power supply pins (VDD_RF, VDD_MIX, VDD_IF, VDD_VCO, VDD_CP, and VDD_PLL pins) and the digital power supply pins (VDDIO and VREG_IN pins).

*7: The “Typ.” condition is V_{DDIO} = V_{REGIN} =3.0V, 25°C.

*8: The value applies to the following conditions (a higher value may occur depending on the MCU operation):
SCI interface clock is 2MHz; data transfer rate is 4800bps.

DC Common Characteristics

(Operation power supply voltage: V_{DDIO}=V_{REGIN}=2.1V - 3.6V, Ta=-25 - +65°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" level input voltage	V_{IH1}	(*9)(*10)(*11) XI pin excluded	V_{DDIO} X 0.75	—	V_{DDIO}	V
	V_{IH2}	XI pin	$V_{REGCORE}$ X 0.9	—	$V_{REGCORE}$	V
"L" level input voltage	V_{IL1}	(*9)(*10)(*11) XI pin excluded	0	—	V_{DDIO} X 0.1	V
	V_{IL2}	XI pin	0	—	$V_{REGCORE}$ X 0.25	V
Schmitt trigger "H" level judgment threshold	V_{T+}	(*10)	—	1.2	1.8	V
Schmitt trigger "L" level judgment threshold	V_{T-}	(*10)	0.4	0.8	—	V
Input leakage current	I_{IH1}	VIH= V_{DDIO} (*9)(*10)(*11)	-2	—	2	µA
	I_{IH2}	VIH= $V_{REGOUT2}$ (*19)	-2	—	2.3	µA
	I_{IL1}	VIL=0V (*9)(*10)	-2	—	2	µA
	I_{IL2}	VIL=0V (*11)	-200	-25	-5	µA
	I_{IL3}	VIL=0V (*19)	-2.3	—	2	µA
"H" level output voltage	V_{OH1}	IOH=-100µA (*13)	V_{DDIO} - 0.2	—	V_{DDIO}	V
	V_{OH2}	IOH=-4mA ($V_{DDIO=2.7\sim3.6V}$) (*13)	V_{DDIO} x 0.8	—	V_{DDIO}	V
		IOH=-4mA ($V_{DDIO=2.1\sim2.7V}$) (*13)	V_{DDIO} x 0.7	—	V_{DDIO}	V
	V_{OH3}	IOH=-100µA (*18)	1.65	—	2.35	V
"L" level output voltage	V_{OL1}	IOL=100µA (*13)	0	—	0.2	V
	V_{OL2}	IOL=4mA (*13)	0	—	V_{DDIO} x 0.2	V
	V_{OL3}	IOH=-100µA (*18)	0	—	0.45	V
Regulator output voltage	$V_{REGOUT1}$	When VREG_CORE pin is sleeping ($I_{REGOUT1}$=5µA)	1.2	1.7	2.2	V
	$V_{REGOUT2}$	When VREG_CORE pin is idling, transmitting, and receiving ($I_{REGOUT2}$=5mA)	1.95	2.2	2.3	V
	$V_{REGOUT3}$	When VREG_OUT pin is transmitting and receiving	1.95	2.2	2.3	V
Input capacitance	C_{IN}	Input pin (*9)(*10)(*11)	—	6	—	pF
	C_{OUT}	Output pin (*13)	—	9	—	pF
	C_{RFI}	RF input pin (*14)	—	9	—	pF
	C_{RFO}	RF output pin (*15)	—	9	—	pF
	C_{AI}	Analog input pin (*16)	—	9	—	pF
	C_{AO}	Analog output pin (*17)	—	9	—	pF

(*9) Applies to the pins indicated as I in the I/O column in the Pin Descriptions section.

*10: Applies to the pins indicated as I_S in the I/O column in the “Pin Descriptions” section.

*11: Applies to the pins that are indicated as I_U in the I/O column in the Pin Descriptions section.

*13: Applies to the pins that are indicated as O in the I/O column in the Pin Descriptions section, except for the XO pin.

*14: Applies to the pins that are indicated as I_{RF} in the I/O column in the Pin Descriptions section.

*15: Applies to the pins that are indicated as O_{RF} in the I/O column in the Pin Descriptions section.

*16: Applies to the pins that are indicated as I_A in the I/O column in the Pin Descriptions section.
*17: Applies to the pins that are indicated as O_A in the I/O column in the Pin Descriptions section.
*18: XO pin.
*19: XI pin.

RF Characteristics

Data rate	:	1200/2400/4800 bps
Modulation method	:	Binary FSK
Channel interval	:	12.5kHz
Frequency range	:	426.0250MHz~426.8375 MHz
	:	429.1750MHz~429.9250 MHz
Power supply voltage (RF)	:	1.95V - 2.35V (supplied from VREG_OUT)
Operating temperature	:	-25°C~65°C

Item	Condition	Min.	Typ.	Max.	Unit
Transmitting power	at 10mW Mode	5	10	12	mW
	at 1mW Mode	0.5	1	1.2	mW
Transmit adjacent channel leakage	RBW=±4.25kHz	—	—	40	dBc
Occupied bandwidth	99%	4	—	8.5	kHz
Frequency deviation		2	—	—	kHz
Transmit spurious emissions		—	—	2.5	μW
Receiver sensitivity	BER<10^{-2} Fdev:±1.5kHz at 2400bps	—	—	-113	dBm
	BER<10^{-6} Fdev::±1.5kHz at 2400bps	—	—	-107	dBm
Maximum input level	BER<10^{-6} Fdev::±1.5kHz at 2400bps	0	—	—	dBm
Receiver spurious response	Desired signal : Reference sensitivity + 3dB Interfering signal: CW BER<1%	40	—	—	dB
Receiver C/I adjacent interference 12.5kHz offset	Desired signal: Reference sensitivity + 3dB Interfering signal: Modulation wave BER<1%	30	—	—	dB
Receiver C/I alternate interference 25.0kHzoffset	Desired signal: Reference sensitivity + 3dB Interfering signal: Modulation wave BER<1%	30	—	—	dB
Receiver intermodulation characteristics	Desired signal: Reference sensitivity + 3dB Interfering signal: CW adjacent channel and second adjacent channel. BER<1%	40	-	-	dB
Receiver spurious emissions		—	—	4	nW
RSSI dynamic range		40	—	—	dB
RSSI minimum sensitive level		—	—	-105	dBm
State transition time: transmitting/receiving or receiving/transmitting		—	—	1	msec

(Notes)

In the Manchester encoding mode, the transmission rates of the baseband (DIO) and on the radio circuit (antenna end) are 600/1200/2400bps and 1200/2400/4800bps respectively.

These RF characteristics shall be measured using the antenna terminal on an application circuit.

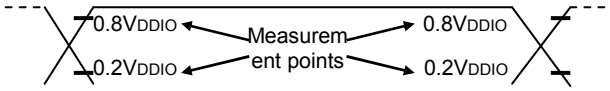
Synchronous Communication Interface (SCI) Characteristics

(Operation power supply voltage: 2.1V - 3.6V, Ta=—25 - +65°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
SCLK clock frequency	FSCLK	except suspend	Load capacitance CL= 50pF	0.1	2	8	MHz
SCEN input setup time	TCESU			125	—	—	ns
SCEN input hold time	TCEH			125	—	—	ns
SCLK "H" pulse width	TWCKH			50	—	—	ns
SCLK "L" pulse width	TWCKL			50	—	—	ns
SDIN input setup time	TDISU			5	—	—	ns
SDIN input hold time	TDIH			15	—	—	ns
SCEN output enable time	TCEEN0	Positive Clock		0	—	40	ns
	TCEEN1	Negative Clock		0	—	20	ns
SCEN assertion interval	TCEITVL			1	—	—	us
SCEN output disable time	TCEDIS			—	—	25	ns
SCLK output delay time	TCKOD			—	—	100	ns
	TCKODF			—	—	40	ns
SDO output hold time	TDOH			50	—	—	ns

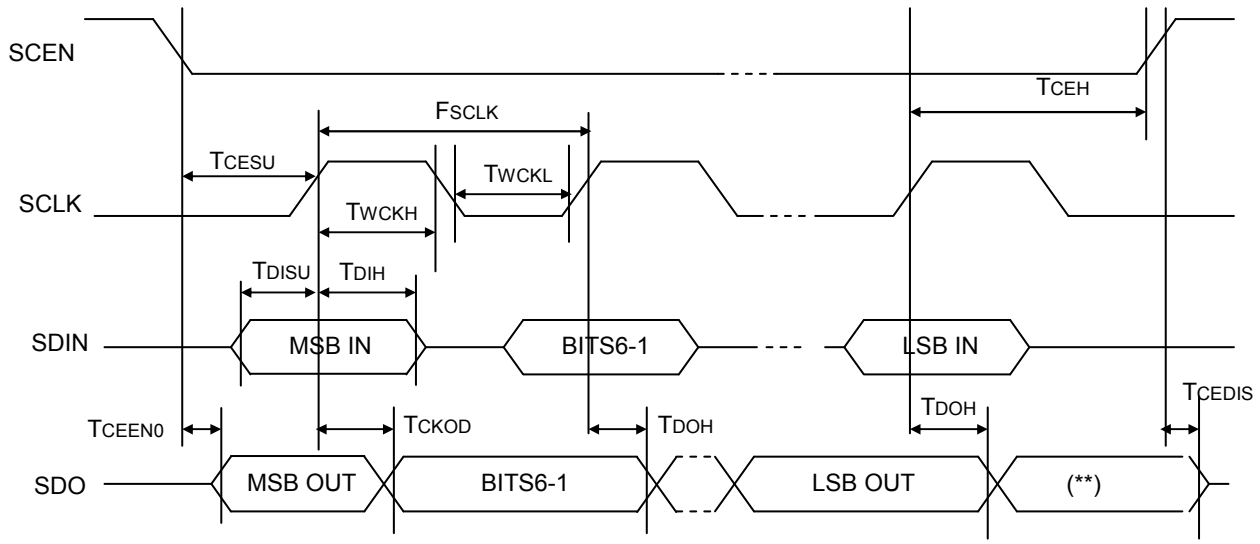
(Notes)
All the timings are measured at the 20% and 80% levels of VDDIO.

Measurement points

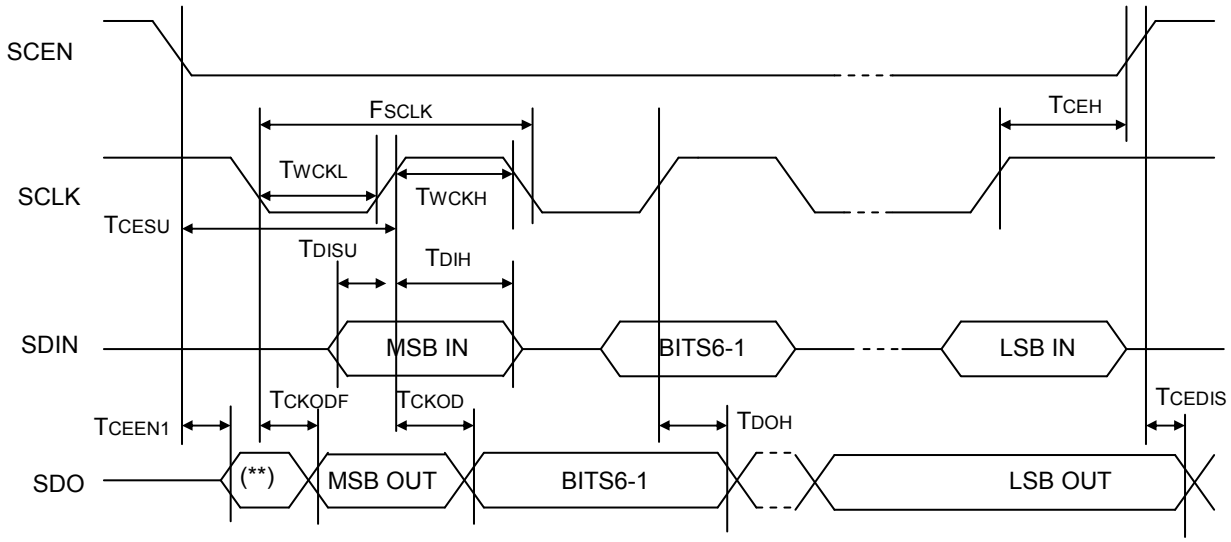


All the following measurement points are equivalent to the above ones.

When SCLK is a positive clock



When SCLK is a negative clock



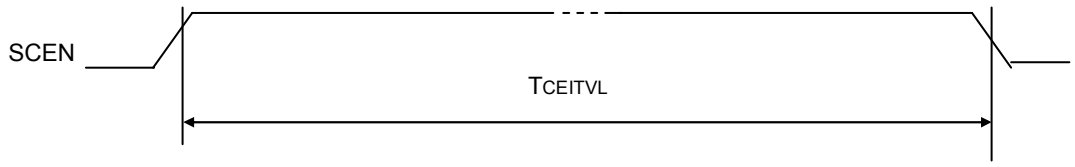
(Notes)

The SINT pin signal occurs at the timing independent of the signals of other clock synchronous serial interface related pins.

The above diagrams show the case of input/output from the MSB. It can be changed to input/output from the LSB through the MODE pin setting.

**: Although the output value is not specified, MSB data is output in the case of input/output from the MSB indicated above.

For input/output from the LSB, LSB data is output.



Transmit/Receive Data Interface Characteristics

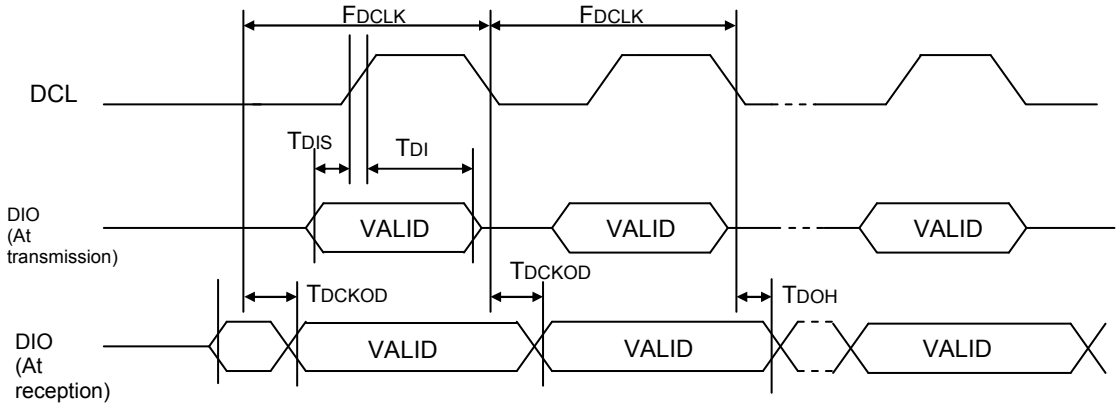
(Operation power supply voltage: 2.1V - 3.6V, Ta=-25 - +65°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
DIO input setup time	T_{DISU}	At transmission	Load capacitance CL= 50pF	20	—	—	ns
DIO input hold time	T_{DIH}	At transmission		20	—	—	ns
DCLK output delay time	T_{DCKOD}	At reception		—	—	40	ns
DIO output hold time	T_{DOH}	At reception		15	—	—	ns

(Notes)

All the timings are measured at the 20% and 80% levels of V_{DDIO}.

The DCLK clock frequency F_{DCLK} is 600Hz / 1200Hz / 2400Hz / 4800Hz.



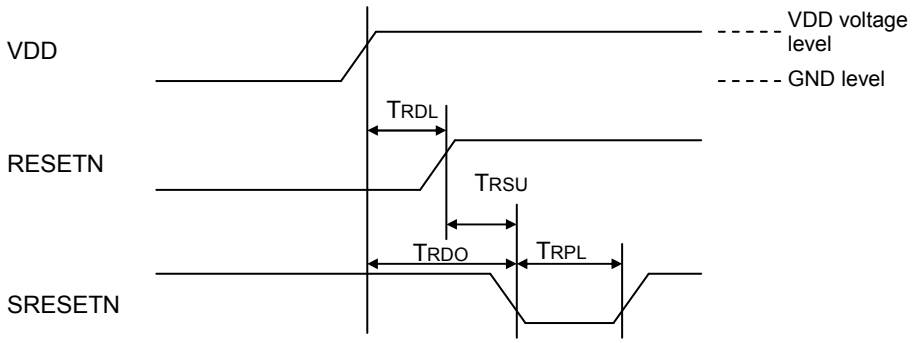
Reset Characteristics

(Operation power supply voltage: 2.1V - 3.6V, Ta=—25 - +65°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
RESETN delay time (at power on)	T_{RDL}	After all power supply pins are powered on	1	—	—	ms
SRESETN pulse time	T_{RPLS}	RESETN=1	200	—	—	ns
SRESETN delay time (when operating)	T_{RDOP}		1	—	—	ms
RESETN-SRESETN setup time (when operating)	T_{RSU}		10	—	—	ns

(Notes)

All the timings are measured at the 20% and 80% levels of V_{DDIO}.



Power ON and Power Down Characteristics

(Operation power supply voltage: 2.1V - 3.6V, Ta=—25 - +65°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power-on time difference	TPWON	At power on between VDDIO - VREG_IN pins	—	1	5	ms
Power-off time difference	TPWOFF	At power off between VDDIO - VREG_IN pins	—	1	5	ms

(Notes)

No specification for the power-on order. However, each reset time after power on regulated by the RESETN pin must be satisfied.

Timings are measured at the 20% and 80% levels of the minimum value of the power supply voltage of each power supply pin.

Regulator Characteristics

(Operation power supply voltage: 2.1V - 3.6V, Ta=—25 - +65°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Regulator power-on output response time	TREGON	At power on VREG_OUT pin	—	5	10	µs
Regulator power-off output response time	TREGOFF	At power off VREG_OUT pin	—	5	10	µs
Regulator voltage input time	TREGIN	—	5	-	-	ms

(Notes)

TREGON is the time from when the VREG_IN pin reaches 2.2V to when the 2.1V voltage is output from the VREG_OUT pin at power-on.

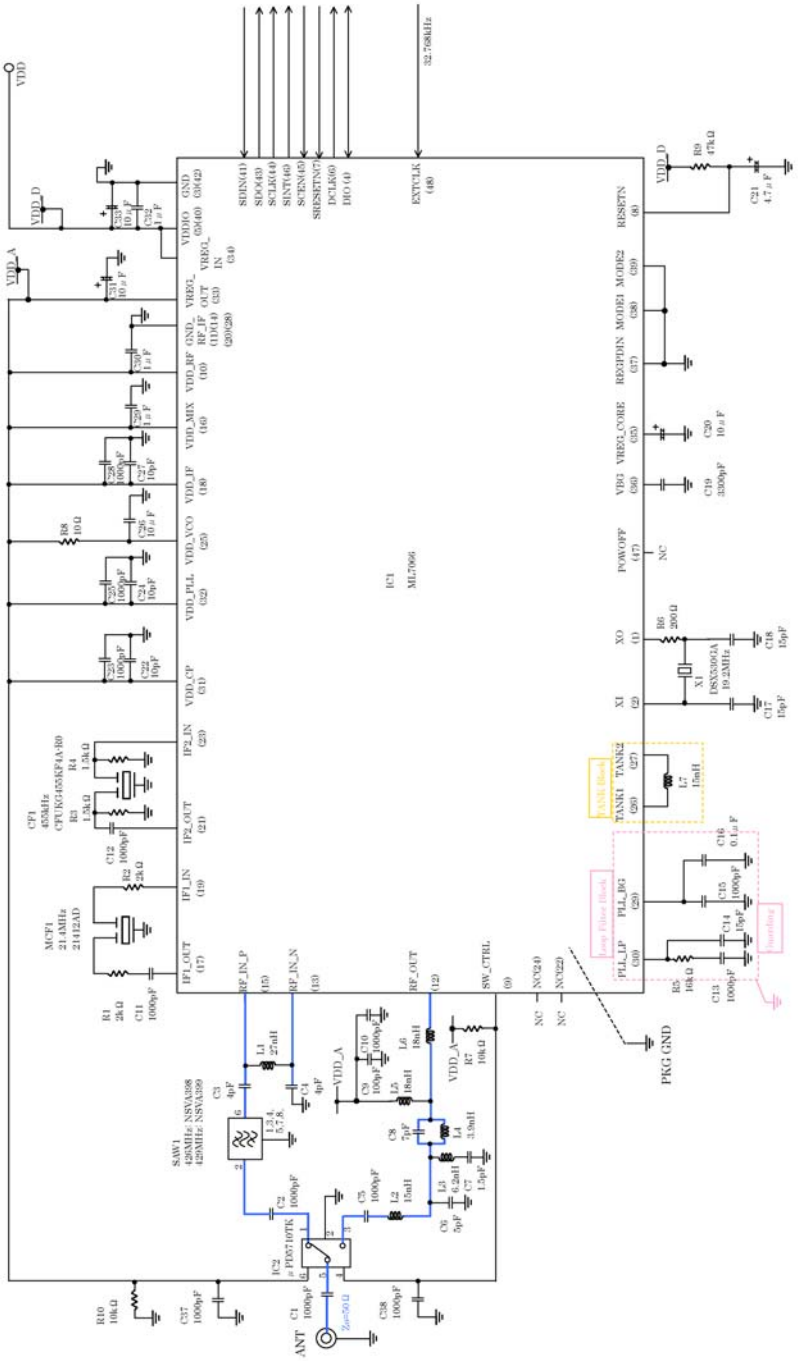
TREGOFF is the time from when the VREG_IN pin reaches 2.2V to when the output level of the VREG_OUT pin begins falling at power-off. Any required voltage output from the regulator should not be used after this time elapsed.

TREGIN is the rise time (0V→VDD level) of the voltage applied to the VREG_IN pin at power-on.

Application Circuit

The following shows the typical application circuit. This circuit may vary depending on the shipment time or other factor. This This circuit and componet list are used for ML066 evaluation board.
LAPIS Semiconductor recommended that choosing and finalize the best component valuse by evaluationg on the target board.

ML7066 Evaluation Board Circuit



Component List of ML7066 Evaluation Board

Parts No.	Type No.	Vendors	Remarks
IC1	ML7066	LAPIS Semiconductor	
IC2	µPD5710TK	NEC	CMOS SPDT SW
SAW1	NSVA398	Japan Radio	426MHz band SAW Filter
	NSVA399		429MHz band SAW Filter
MCF1	21412AD	Daishinku	Quartz filter 21.4MHz
CF1	CFUKG455KF4A-R0	Murata Manufacturing	Ceramic filter 455kHz
X1	DSX530GA	Daishinku	Crystal oscillator 19.2MHz
C1	1000pF	Murata Manufacturing	GRM1882 or equivalent
C2	1000pF	Murata Manufacturing	GRM1882 or equivalent
C3	4pF	Murata Manufacturing	GRM1882 or equivalent
C4	4pF	Murata Manufacturing	GRM1882 or equivalent
C5	1000pF	Murata Manufacturing	GRM1882 or equivalent
C6	5pF	Murata Manufacturing	GRM1882 or equivalent
C7	1.5pF	Murata Manufacturing	GRM1884 or equivalent
C8	7pF	Murata Manufacturing	GRM1882 or equivalent
C9	100pF	Murata Manufacturing	GRM1882 or equivalent
C10	1000pF	Murata Manufacturing	GRM1882 or equivalent
C11	1000pF	Murata Manufacturing	GRM1882 or equivalent
C12	1000pF	Murata Manufacturing	GRM1882 or equivalent
C13	1000pF	Murata Manufacturing	GRM1882 or equivalent
C14	15pF	Murata Manufacturing	GRM1882 or equivalent
C15	1000pF	Murata Manufacturing	GRM1882 or equivalent
C16	0.1µF	Murata Manufacturing	GRM1882 or equivalent
C17	15pF	Murata Manufacturing	GRM1882 or equivalent
C18	15pF	Murata Manufacturing	GRM1882 or equivalent
C19	3300pF	Murata Manufacturing	GRM1882 or equivalent
C20	10µF	NEC	E/SV line-up or equivalent
C21	4.7µF	NEC	E/SV line-up or equivalent
C22	10pF	Murata Manufacturing	GRM1882 or equivalent
C23	1000pF	Murata Manufacturing	GRM1882 or equivalent
C24	10pF	Murata Manufacturing	GRM1882 or equivalent
C25	1000pF	Murata Manufacturing	GRM1882 or equivalent
C26	10µF	Murata Manufacturing	GRM188 or equivalent
C27	10pF	Murata Manufacturing	GRM1882 or equivalent
C28	1000pF	Murata Manufacturing	GRM1882 or equivalent
C29	1µF	Murata Manufacturing	GRM1882 or equivalent
C30	1µF	Murata Manufacturing	GRM1882 or equivalent
C31	10µF	NEC	E/SV line-up or equivalent
C32	1µF	Murata Manufacturing	GRM1882 or equivalent
C33	10µF	NEC	E/SV line-up or equivalent
C34	1000pF	Murata Manufacturing	GRM1882 or equivalent
C35	1000pF	Murata Manufacturing	GRM1882 or equivalent
L1	27nH	Murata Manufacturing	LQG18 or equivalent
L2	15nH	Murata Manufacturing	LQG18 or equivalent
L3	6.2nH	Murata Manufacturing	LQW18AN6N2D00
L4	3.9nH	Murata Manufacturing	LQW18AN3N9D10
L5	18nH	Murata Manufacturing	LQG18 or equivalent
L6	18nH	Murata Manufacturing	LQG18 or equivalent
L7	15nH	Murata Manufacturing	LQW18AN15NJ10
R1	2kΩ	KOA	RK73B 1J or equivalent
R2	2kΩ	KOA	RK73B 1J or equivalent
R3	1.5kΩ	KOA	RK73B 1J or equivalent
R4	1.5kΩ	KOA	RK73B 1J or equivalent
R5	16kΩ	KOA	RK73B 1J or equivalent
R6	200Ω	KOA	RK73B 1J or equivalent
R7	10kΩ	KOA	RK73B 1J or equivalent
R8	10Ω	KOA	RK73B 1J or equivalent
R9	47kΩ	KOA	RK73B 1J or equivalent
R10 (* 1)	10kΩ	KOA	RK73B 1J or equivalent

(* 1): This resistor can be inserted anywhere in the connected power line, but mandatory.
In some past cases, ML7066 could not start up successfully without this resistor.

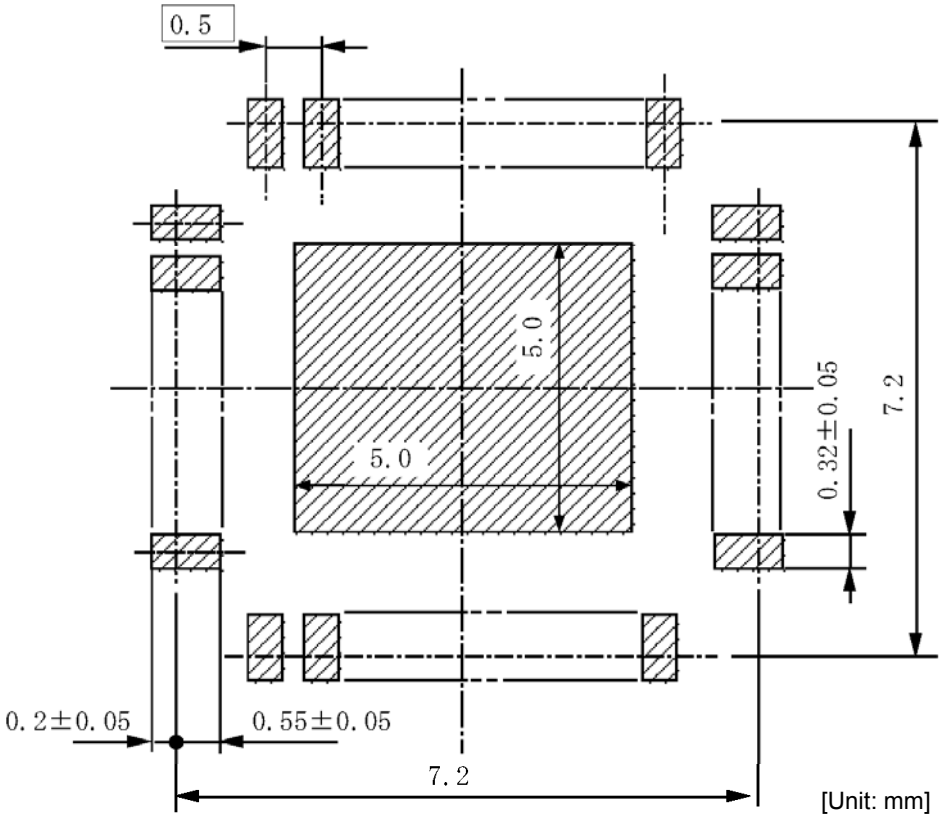
Package Information

Recommended PCB Layout

P-VQFN48-0707-0.50-T6

Reference Diagram

Recommended Land Pattern



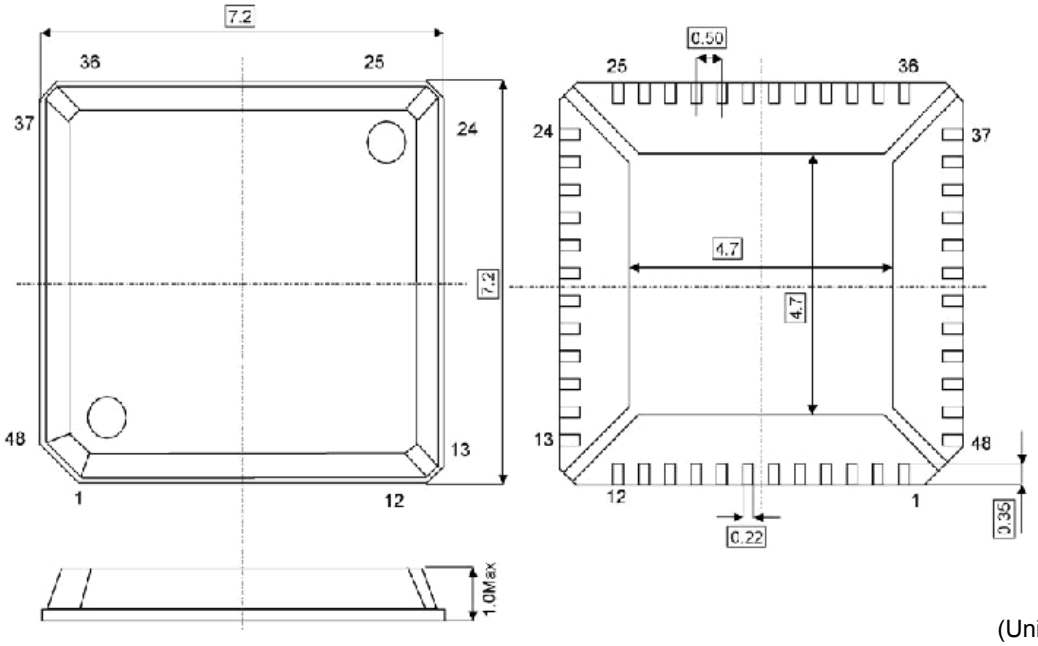
[Unit: mm]

When designing the land pattern of the mounting board, you should give due consideration to ease of mounting, reliability of connection, wiring, and no solder bridging.
The optimal design of the land pattern depends on the board material, solder type, thickness, and soldering method. This material shall be used for reference only when designing the land pattern.

LAPIS Semiconductor Co.,Ltd.

Package Dimensions

48 Pin VQFN



(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact ROHM's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7066-01	Apr.28, 2011	–	–	Edition 1

NOTE

Any editorial changes are not listed up.

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