

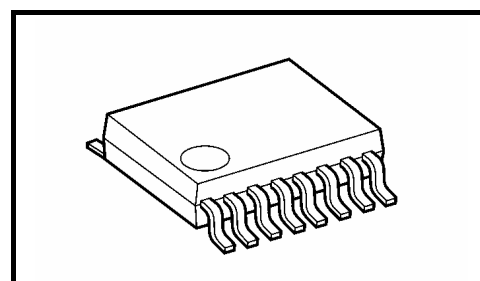
T6B70BFNG

Interface IC for Hot Water Dispensers

The T6B70BFNG is designed to be used mainly as an interface IC for communication between hot water dispensers and the corresponding controller unit, and comes equipped with a two channel 4-bit D/A converter, pseudo sine wave generator and an external analog signal detection circuit.

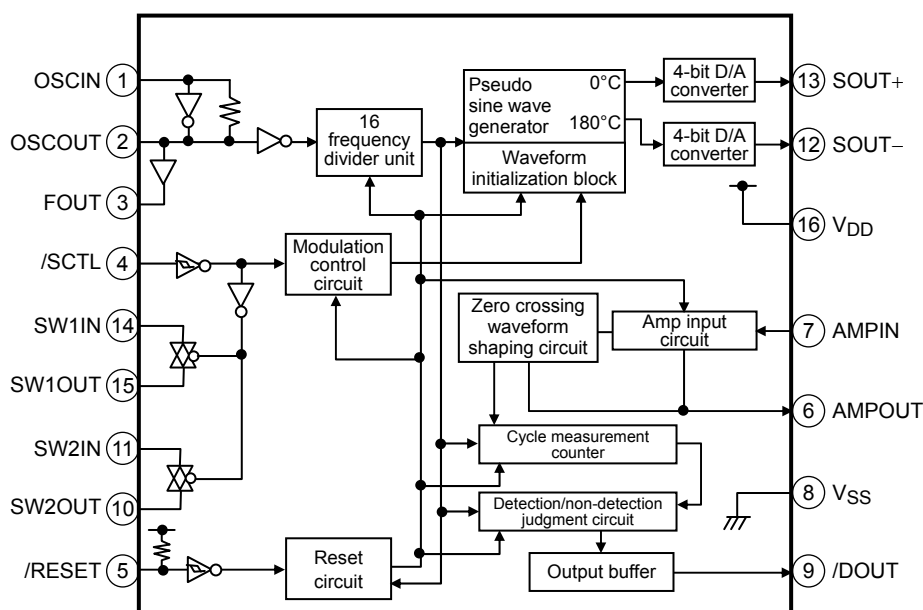
Features

- Built-in two channel 4-bit D/A converter (opposite polarities)
- Built-in pseudo sine wave generator (external clock 1/16 frequency divider)
- Built-in external analog signal detection/non-detection circuit
- Built-in two channel analog switch

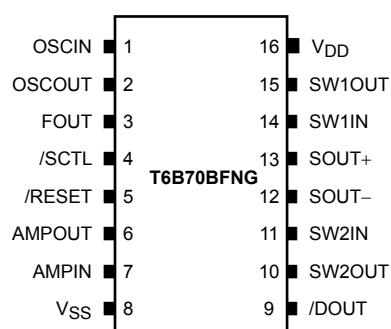


Weight: 0.07 g (typ.)

Block Diagram



Pin Assignment Diagram



Pin Functions

| Pin No. | Symbol | Input/Output | Function |
|---------|-----------------|--------------|--|
| 1 | OSCIN | Input | Pins connected to oscillation |
| 2 | OSCOU | Output | Pins connected to oscillation |
| 3 | FOU | Output | Output pin for oscillation waveform shaping circuit |
| 4 | /SCTL | Input | Modulation control signal input pin |
| 5 | /RESET | Input | Reset signal input pin |
| 6 | AMPOU | Output | Amplifier signal output pin |
| 7 | AMPIN | Input | Amplifier signal input pin |
| 8 | V _{SS} | — | Device ground pin (0 V) |
| 9 | /DOU | Output | Output pin for amplifier input signal detector |
| 10 | SW2OU | Output | Output pin on analog SW2 side |
| 11 | SW2IN | Input | Input pin on analog SW2 side |
| 12 | SOU- | Output | Pseudo sine wave (opposite polarity of SOUT + output) output pin |
| 13 | SOU+ | Output | Pseudo sine wave output pin |
| 14 | SW1IN | Input | Input pin on analog SW1 side |
| 15 | SW1OU | Output | Output pin on analog SW1 side |
| 16 | V _{DD} | — | Device power supply pin (+5 V) |

The equivalent circuit diagrams provided in the above table are given to facilitate understanding in designing the external circuitry but are not intended to accurately represent the internal circuitry.

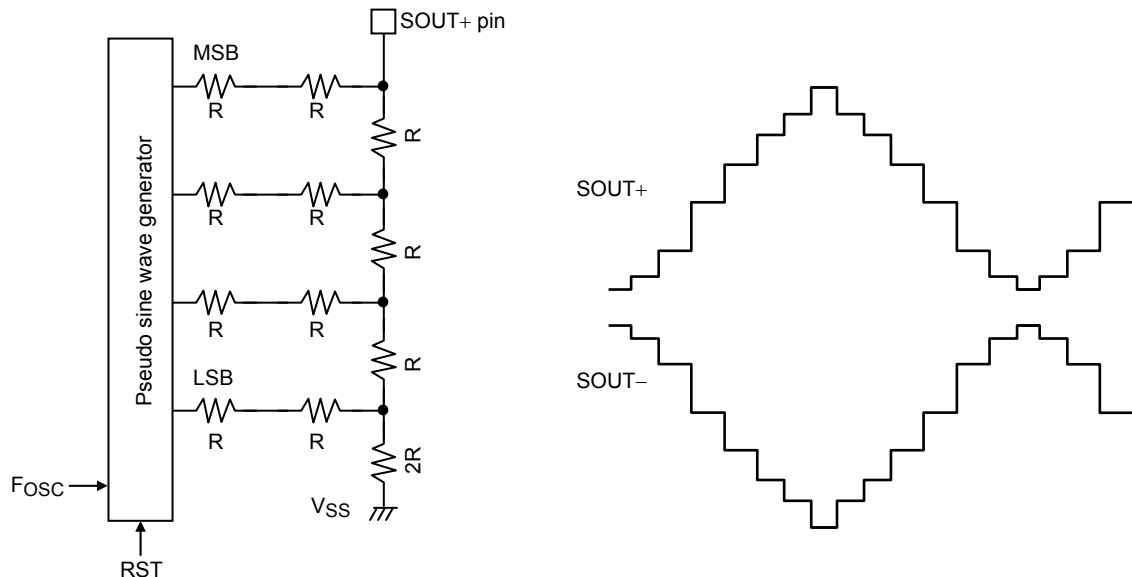
Functions

1. Pseudo sine wave generator and 4-bit D/A converters (transmission block)

The pseudo sine wave signal with $F_{osc}/16$ frequency is output from the pseudo sine wave output pins (SOUT+ and SOUT-).

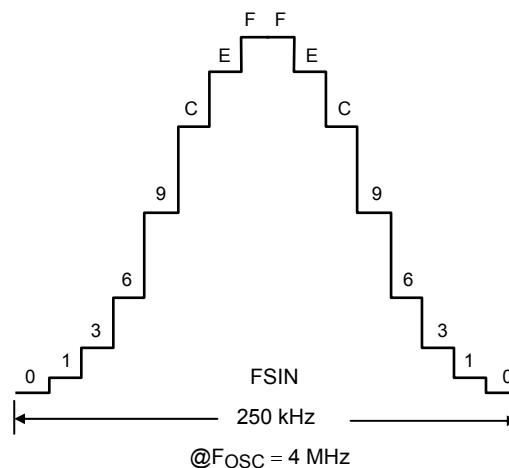
The output polarity of SOUT+ and SOUT- are the opposite.

The transmission block (pseudo sine wave generator and 4-bit D/A converter are as shown below (SOUT+ pin side):



The data of the pseudo sine wave generator is output in the following sequence:

0 → 1 → 3 → 6 → 9 → C → E → F → F → E → C → 9 → 6 → 3 → 1 → 0 (hexadecimal)



Therefore, when there is no load, the pseudo sine waveform of the positive and negative output is like a staircase (as illustrated above).

An analog switch is built-in so that the driver output buffer connects to the transmission line only during transmission.

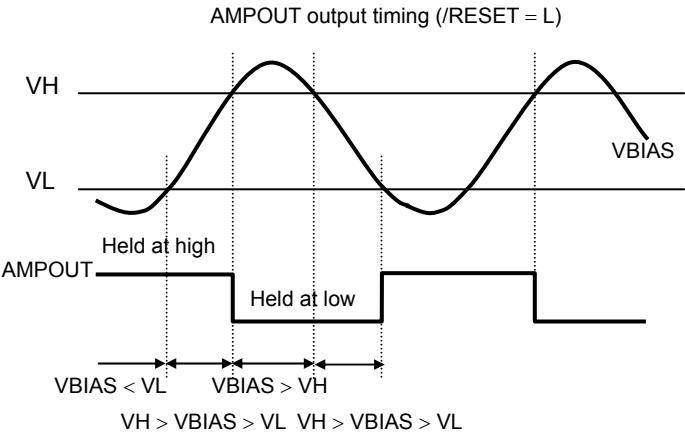
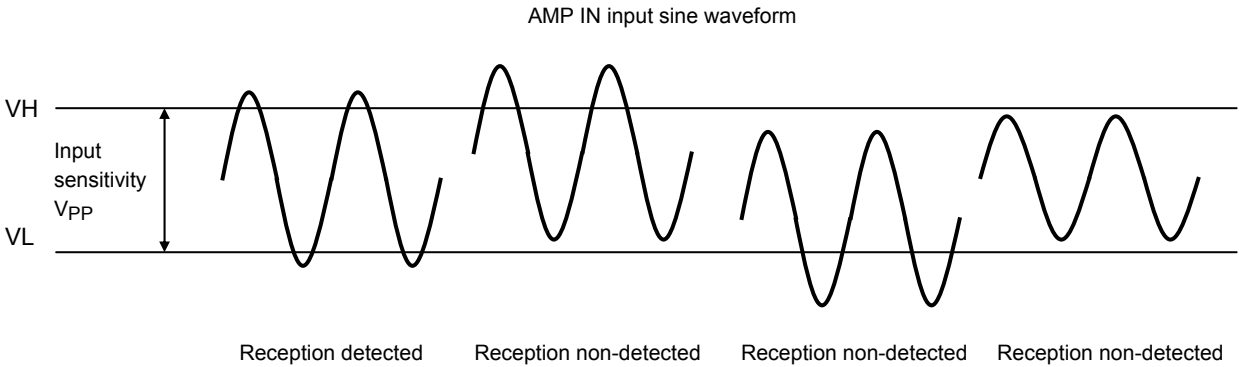
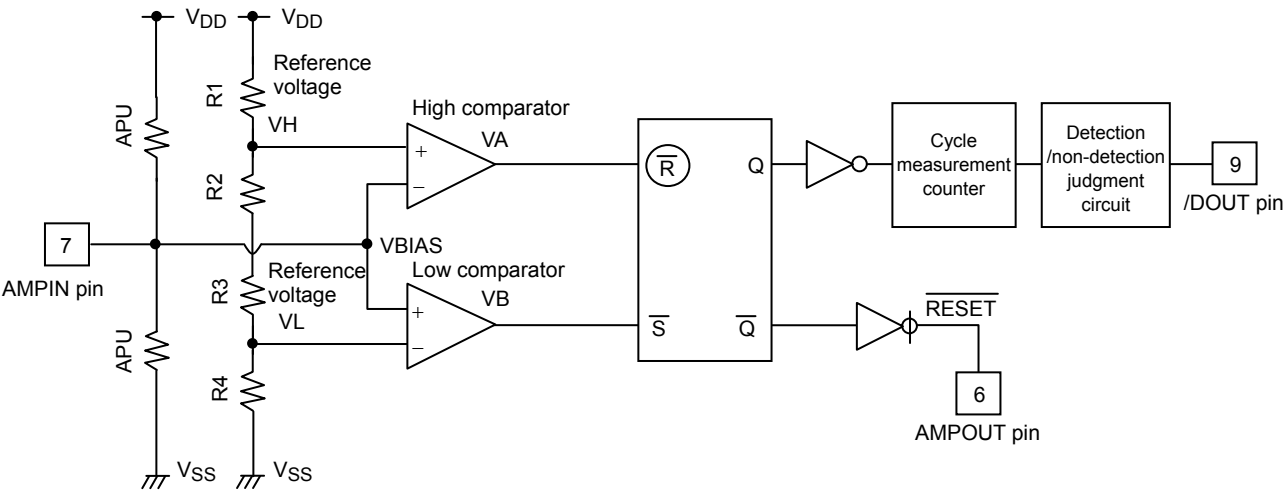
However, an emitter follower circuit is externally connected to the driver output buffer.

The phase difference between the positive and negative output is within $180^\circ \pm 5^\circ$ (to account for fluctuation in the pseudo sine wave output phase).

2. Amplifier input circuit and signal detection/non-detection circuit (reception block)

The modulation signal input block is equipped with high and a low comparator to detect only when the external sine wave signal's amplitude is above the defined threshold. In this way, signals with amplitudes lower than the specified threshold (e.g., noise signals) are prevented from being mistakenly detected as sine waves.

The detection frequency range (frequency window) is determined by the divider ratio 1/17 to 1/15 of F_{osc} . Detection/non-detection confirmation conditions are such that when the signals within the specified frequency range are detected (or not detected) in succession, the signals are controlled. It takes about 9 to 15 waves (based on F_{osc} 1/16 frequency) to make detection/non-detection confirmation in this manner.



| AMPOUT Truth Table | | | |
|--------------------|----|----|--------|
| | VA | VB | AMPOUT |
| VBIAS > VH | L | H | L |
| VH > VBIAS > VL | H | H | Hold |
| VBIAS < VL | H | L | H |

3. Transmission block function and timing

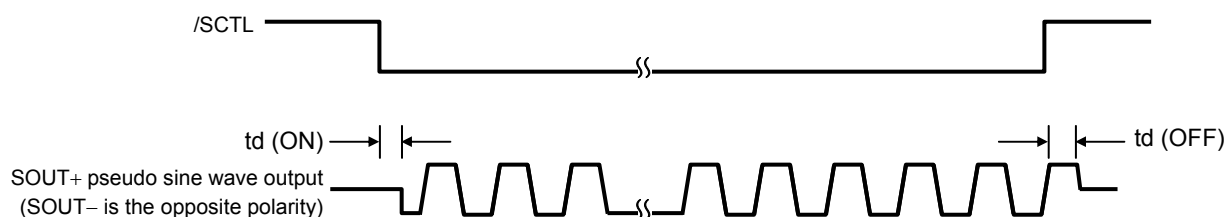
When the modulation control input (/SCTL) is in High-level, the pseudo sine wave output is held at 0° phase of the pseudo sine wave. When the modulation control input changes from High-level to Low-level, the pseudo sine wave output (SOUT+) initially outputs from -90° (SOUT- outputs from +90°).

The time required to turn ON in this case is as follows:

$t_d(\text{ON}) < 500 \text{ ns}$

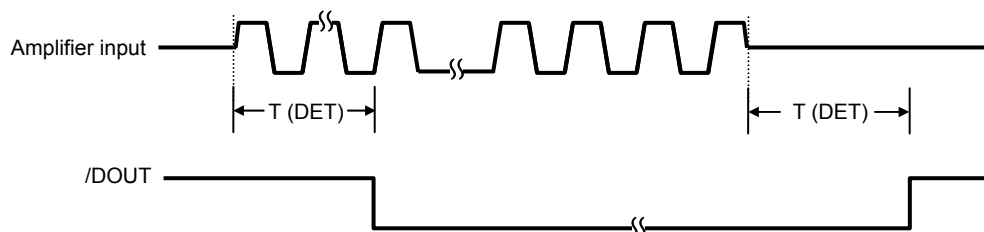
When modulation control input changes from Low-level to High-level, the phase is forcibly held at 0° (the pseudo sine wave output is stopped), regardless of the phase of the pseudo sine wave output. The time required to turn OFF in this case is as follows:

$t_d(\text{OFF}) < 1 \mu\text{s}$



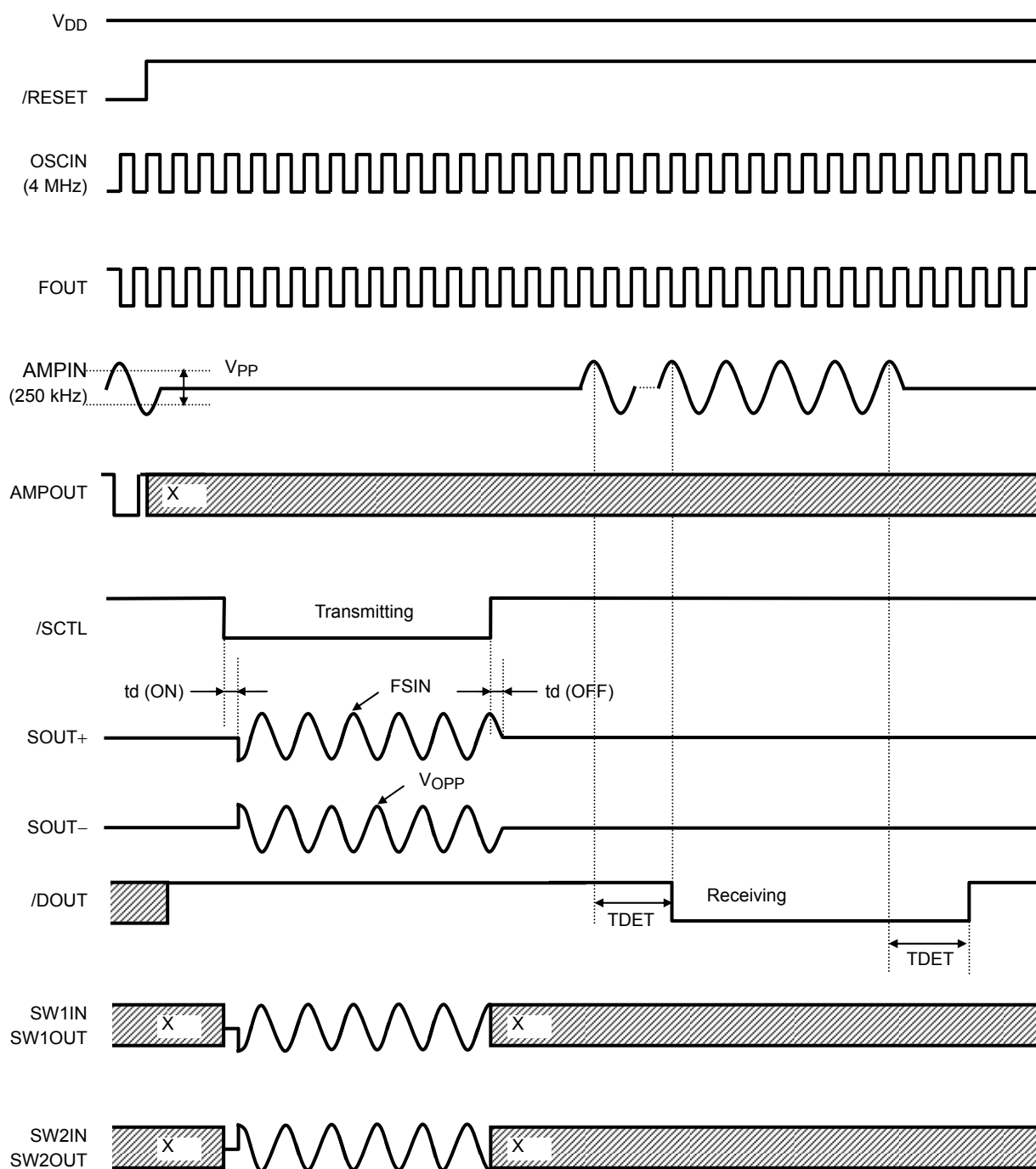
4. Reception block function and timing

Once it is okay to receive the amplifier input signal, the time it takes for the /DOUT pin to changes from High to Low (T (DET)) is about 9 to 15 waves (based on $F_{\text{osc}} 1/16$ frequency). This condition is only valid when the cyclic input signal within the range specified by the frequency window is detected (or not detected) in continuation.



Note 1: You are free to use any kind of communication protocol you wish, however be sure to configure a time of carrier wave $\times 15$ waves or more for both when there are and aren't signals.

Timing Chart (SOUT+ = SW1IN, SW1OUT, SOUT- = SW2IN, SW2OUT)



Absolute Maximum Ratings (Ta = 25 ± 1.5°C)

| Characteristics | Symbol | Rating | Unit |
|-----------------------|-------------------------|----------------------------------|------|
| Power supply voltage | V _{DD} | −0.3 to 6.0 | V |
| Input voltage | V _I | −0.3 to V _{DD} + 0.3 | V |
| Input peak current | I _{IK} | −20 to 20 | mA |
| Operating temperature | T _{opr} | −20 to 80 | °C |
| Storage temperature | T _{stg} | −55 to 125 | °C |
| Power dissipation | P _D (Note 1) | 0.82 | W |

▲CAUTION The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.

Note 1: Power dissipation decreases approximately 8.2 mW per degree (Centigrade).

Electrical Characteristics

 (unless otherwise specified, $V_{DD} = 5.0\text{ V}$, $V_{SS} = 0\text{ V}$, $F_{OSC} = 4\text{ MHz}$ and $T_a = -20\text{ to }80^\circ\text{C}$)

| Characteristics | | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|------------|------------------|--------------|--|-----------------------|-------|-----------------------|------|
| V _{DD} pin (pin 16) | | | | | | | | |
| Operating voltage | | V _{DD} | — | | 4.5 | 5.0 | 5.5 | V |
| Current consumption | | I _{DD} | 1 | When there is no load; F _{OSC} = 4 MHz | — | — | 10 | mA |
| OSCIN pin (pin 1) and OSCOUT pin (pin 2) | | | | | | | | |
| Oscillation frequency | | F _{OSC} | 2 | | 1 | 4 | 10 | MHz |
| Input voltage | High level | VIHOSC | 3 | | 0.7 V _{DD} | — | V _{DD} | V |
| | Low level | VILOSC | 3 | | V _{SS} | — | 0.3 V _{DD} | |
| Input current | High level | IIHROSC | 4 | V _{IN} = 5 V, Ta = 25°C | 3.2 | 6.58 | 13.2 | μA |
| | Low level | IILROSC | 4 | V _{IN} = 0 V, Ta = 25°C | −3.2 | −6.58 | −13.2 | |
| Output voltage | High level | VOHOSC | 3 | IOH = −0.1 mA | V _{DD} − 1 | — | V _{DD} | V |
| | Low level | VOLOSC | 4 | IOL = +0.1 mA | V _{SS} | — | V _{SS} + 0.6 | |
| /RESET pin (5 pin) | | | | | | | | |
| Low to High input switching level | | VIHRST | 5 | | 0.65 V _{DD} | — | V _{DD} | V |
| High to Low input switching level | | VILRST | 5 | | V _{SS} | — | 0.35 V _{DD} | V |
| High-level input current | | IIHRST | 6 | V _{IN} = V _{DD} | −10 | — | 10 | μA |
| Pull-up resistance 1 | | IILRRST1 | 7 | V _{IN} = V _{SS} , Ta = 25°C | 9 | 15 | 21 | kΩ |
| Pull-up resistance 2 | | IILRRST2 | 7 | V _{IN} = V _{SS} , Ta = −20 to 80°C | 6.3 | — | 27.3 | kΩ |
| /SCTL pin (pin 4) | | | | | | | | |
| Low to High input switching level | | VIHSCTL | 8 | | 0.65 V _{DD} | — | V _{DD} | V |
| High to Low input switching level | | VILSCTL | 8 | | V _{SS} | — | 0.35 V _{DD} | V |
| Input current | High level | IIHSCTL | 9 | V _{IN} = V _{DD} | −1 | — | 1 | μA |
| | Low level | IILSCTL | 9 | V _{IN} = V _{DD} | −1 | — | 1 | |
| FOUT pin (pin 3) | | | | | | | | |
| Output voltage | High level | VOHFOUT | 10 | IOH = −1.0 mA | V _{DD} − 1 | — | V _{DD} | V |
| | Low level | VOLFOUT | 11 | IOL = +1.0 mA | V _{SS} | — | V _{SS} + 0.6 | |
| /DOUT pin (pin 9) | | | | | | | | |
| Output voltage | High level | VOHDOUT | 12 | IOH = −1.0 mA | V _{DD} − 1.0 | — | V _{DD} | V |
| | Low level | VOLDOUT | 13 | IOL = +1.0 mA | V _{SS} | — | V _{SS} + 0.6 | |
| Non-reception to reception detection time | | TDET1 | 19 | F _{OSC} = 4 MHz, AMPIN = 250 kHz Time it takes for /DOUT to change from High to Low | 40 | — | 60 | μs |
| Reception to non-reception detection time | | TDET2 | 19 | F _{OSC} = 4 MHz, AMPIN = 250 kHz Time it takes for /DOUT to change from Low to High | 36 | — | 56 | μs |

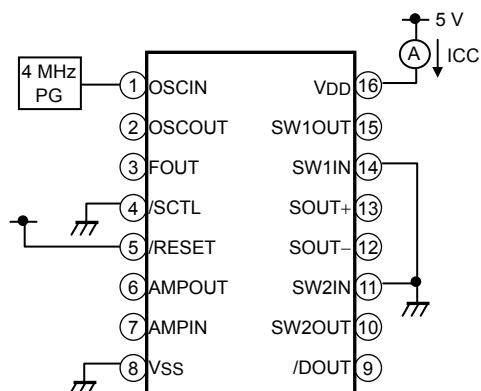
Note: The direction of current flow should be + (sink) when flowing into the IC and − (drain) when flowing out of the IC.

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|--|----------|--------------|---|---------------|------|----------|---------------|
| AMPIN pin (pin 7) | | | | | | | |
| Input dynamic range | VAMPIN | 14 | | V_{SS} | — | V_{DD} | V |
| Pull-up resistance 1 | IILRAPU1 | 15 | $V_{IN} = V_{SS}$, $T_a = 25^\circ\text{C}$ | 11.6 | 19.4 | 27.2 | $k\Omega$ |
| Pull-up resistance 2 | IILRAPU2 | 15 | $V_{IN} = V_{SS}$, $T_a = -20$ to 80°C | 7 | — | 38 | $k\Omega$ |
| Pull-down resistance 1 | IIHRAPD1 | 16 | $V_{IN} = V_{DD}$, $T_a = 25^\circ\text{C}$ | 5.9 | 9.8 | 13.7 | $k\Omega$ |
| Pull-down resistance 2 | IIHRAPD2 | 16 | $V_{IN} = V_{DD}$, $T_a = -20$ to 80°C | 3 | — | 19.2 | $k\Omega$ |
| Amplifier input bias voltage | VBIAS | 17 | No load (design target) | 1.54 | 1.63 | 1.71 | V |
| Amplifier input sensitivity | VPP | 18 | No load, receivable amplitude range is 250 kHz, when sine wave signal is applied. (design target) | 0.3 | — | 0.45 | V |
| Detection frequency range | DETON | 19 | $F_{OSC} = 4$ MHz | 236 | — | 266 | kHz |
| Non-detection frequency (low frequency) | DETOFF1 | 19 | $F_{OSC} = 4$ MHz | — | — | 236 | kHz |
| Non-detection frequency (high frequency) | DETOFF2 | 19 | $F_{OSC} = 4$ MHz | 266 | — | — | kHz |
| SW1IN pin (pin 14) and SW1OUT pin (pin 15) | | | | | | | |
| Analog switch input voltage | VINASW1 | — | | V_{SS} | — | V_{DD} | V |
| Analog switch output voltage | VOUTASW1 | — | | V_{SS} | — | V_{DD} | V |
| OFF-leak current of analog switch 1 | IOFFASW1 | 20 | /SCTL = H, SW1IN = V_{DD} , SW1OUT = V_{SS} | –1 | — | 1 | μA |
| ON-resistance of analog switch 1 | RONASW1 | 21 | /SCTL = L, SW1IN = 5 V, SW1OUT = 0 V Current measure | 35 | — | 105 | Ω |
| SW2IN pin (pin 11) and SW2OUT pin (pin 10) | | | | | | | |
| Analog switch input voltage | VINASW2 | — | | V_{SS} | — | V_{DD} | V |
| Analog switch output voltage | VOUTASW2 | — | | V_{SS} | — | V_{DD} | V |
| OFF-leak current of analog switch 2 | IOFFASW2 | 20 | /SCTL = H, SW2IN = V_{DD} , SW2OUT = V_{SS} | –1 | — | 1 | μA |
| ON-resistance of analog switch 2 | RONASW2 | 21 | /SCTL = L, SW2IN = 5 V, SW2OUT = 0 V Current measure | 35 | — | 105 | Ω |
| SOUT+ pin (13 pin), SOUT– pin (12 pin) | | | | | | | |
| Output voltage | VOPP | 22 | Maximum voltage value when there is no load | $0.85 V_{DD}$ | — | V_{DD} | V |
| Pseudo sine wave output frequency | FSIN | 23 | $F_{OSC} = 4$ MHz | — | 250 | — | kHz |
| Pseudo sine wave output start time | tdON | 23 | /SCTL = H \rightarrow L | — | — | 500 | ns |
| Pseudo sine wave output stop time | tdOFF | 23 | /SCTL = L \rightarrow H | — | — | 1 | μs |
| Equivalent output impedance | ROUTSIN | 24 | No load | 2.8 | 4 | 5.2 | $k\Omega$ |

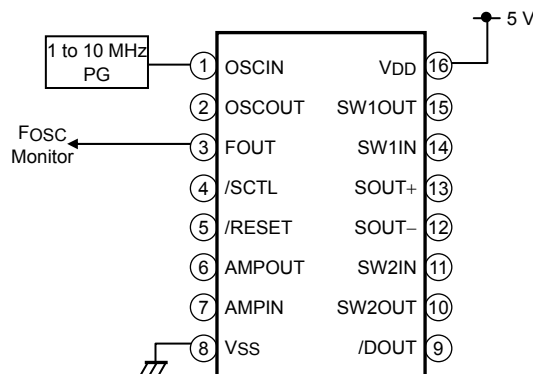
Note: The direction of current flow should be + (sink) when flowing into the IC and – (drain) when flowing out of the IC.

Test Circuit

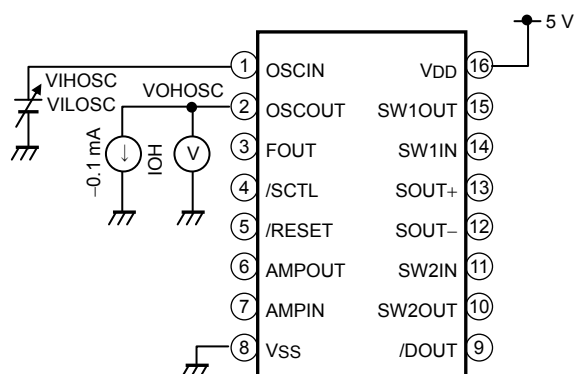
(1) Current consumption



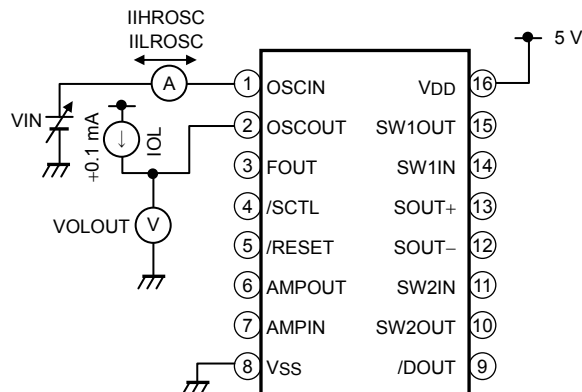
(2) Oscillation frequency



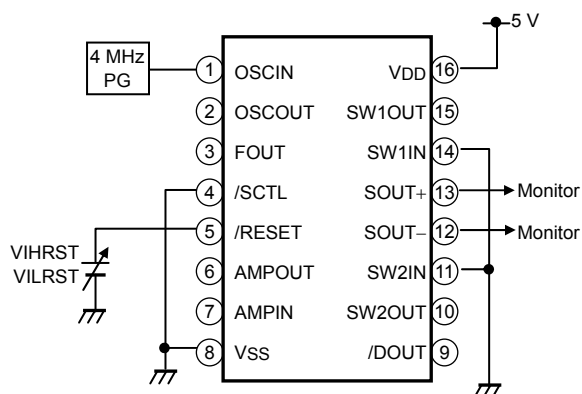
(3) High-level input voltage Low-level input voltage High-level output voltage



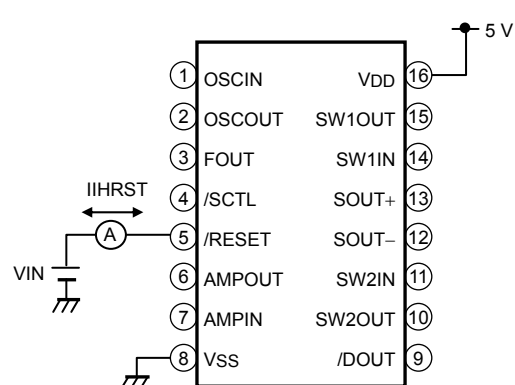
(4) High-level input current Low-level input current Low-level output voltage



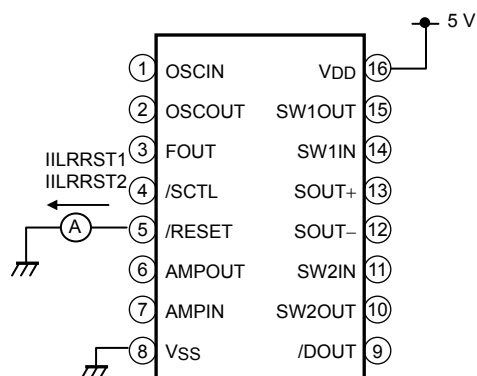
(5) Low to High input switching level High to Low input switching level



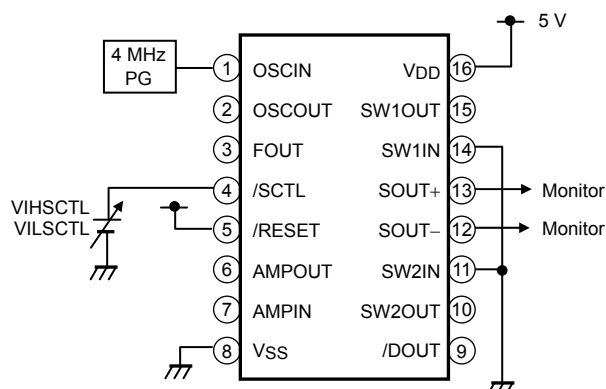
(6) High-level input current



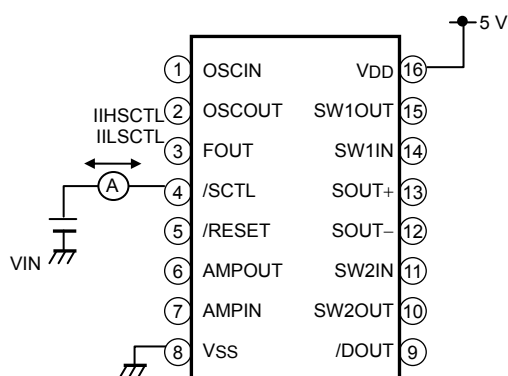
(7) Pull-up resistance 1 Pull-up resistance 2



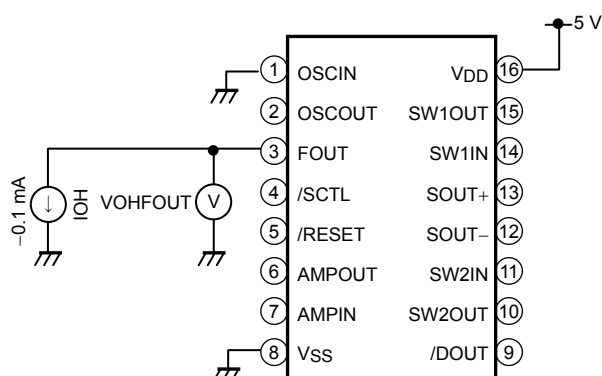
(8) Low to High input switching level High to Low input switching level



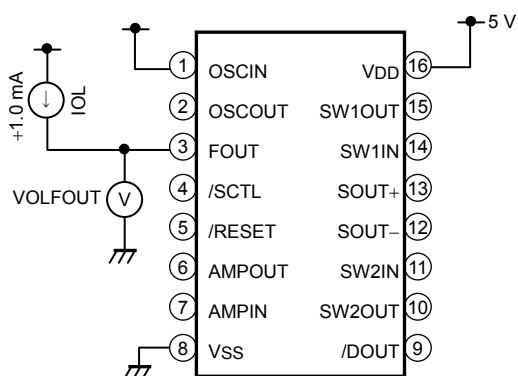
(9) High-level input current Low-level input current



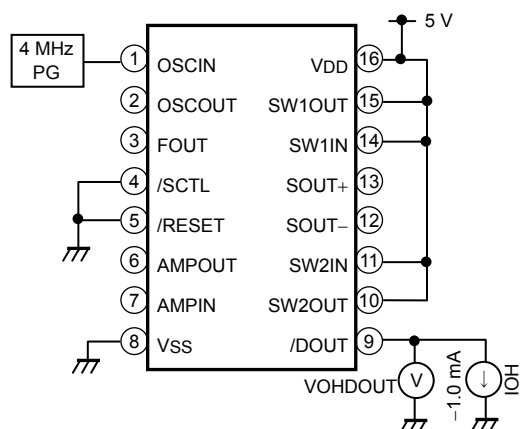
(10) High-level output voltage



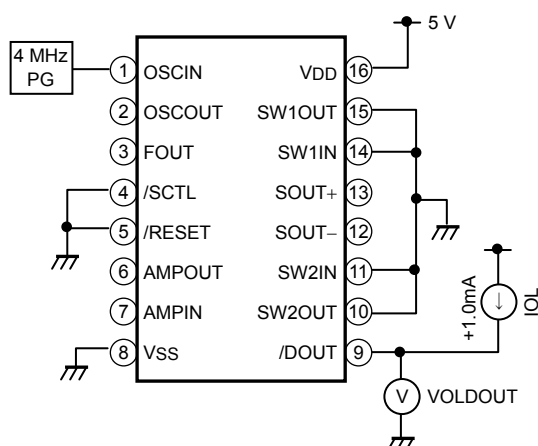
(11) Low-level output voltage



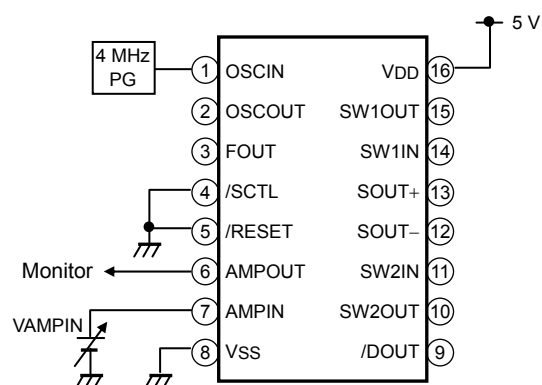
(12) High-level output voltage



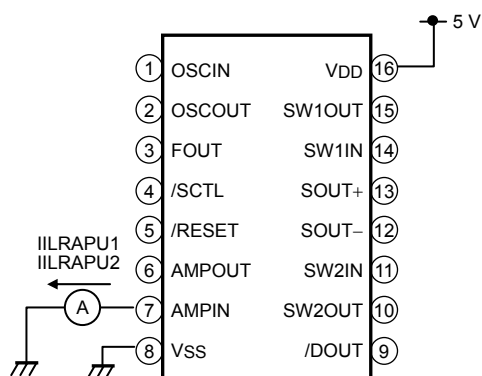
(13) Low-level output voltage



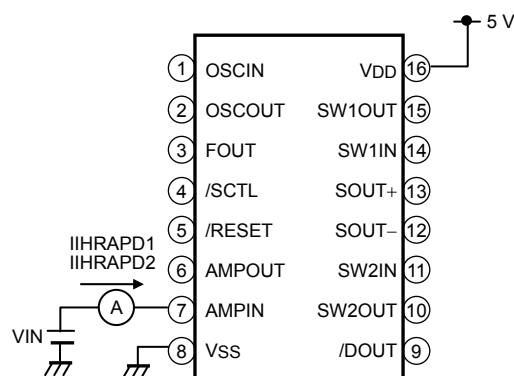
(14) Input dynamic range



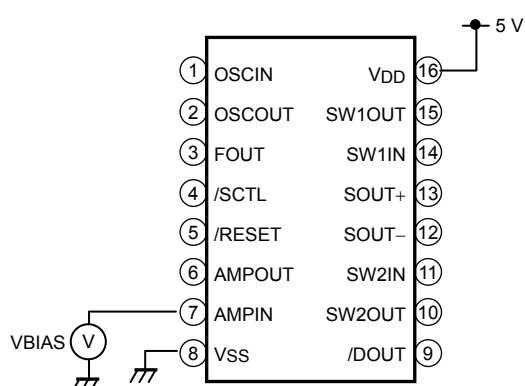
**(15) Pull-up resistance 1
Pull-up resistance 2**



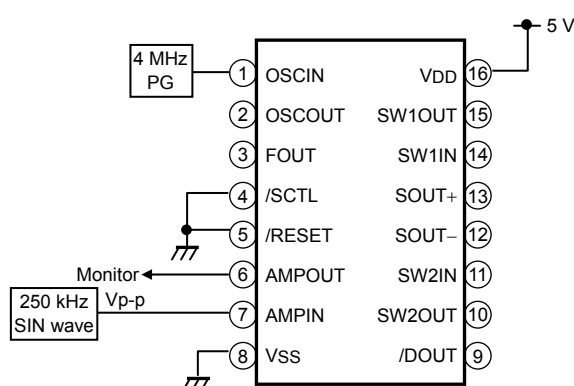
**(16) Pull-down resistance 1
Pull-down resistance 2**



(17) Amplifier input bias voltage

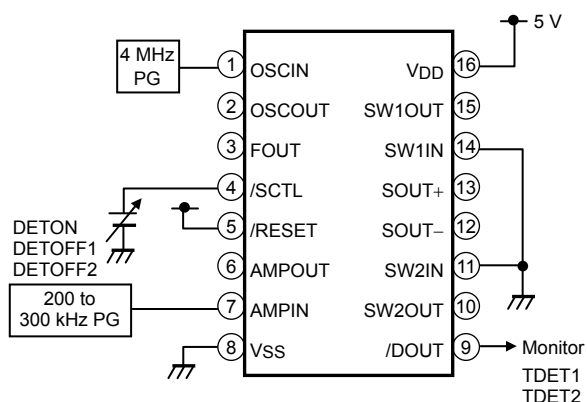


(18) Amplifier input sensitivity



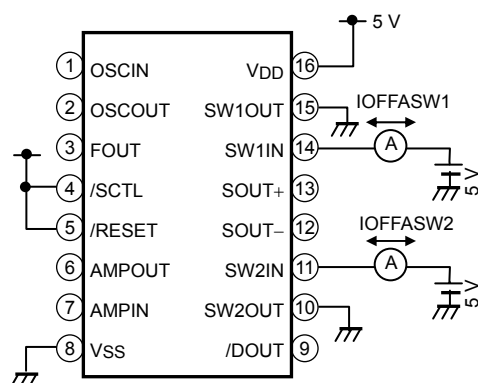
(19) Detection frequency range

Non-detection frequency (low frequency)
 Non-detection frequency (high frequency)
 Non-reception to reception detection time
 Reception to non-reception detection time



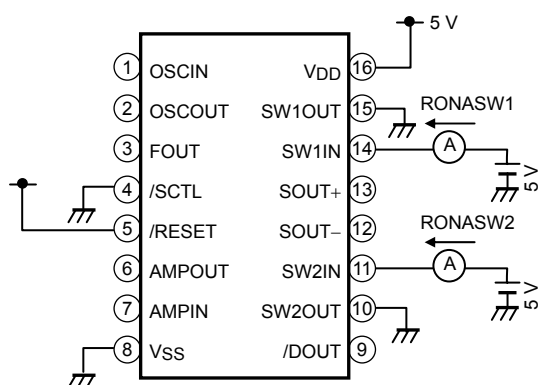
(20) OFF-leak current of analog switch 1

OFF-leak current of analog switch 2

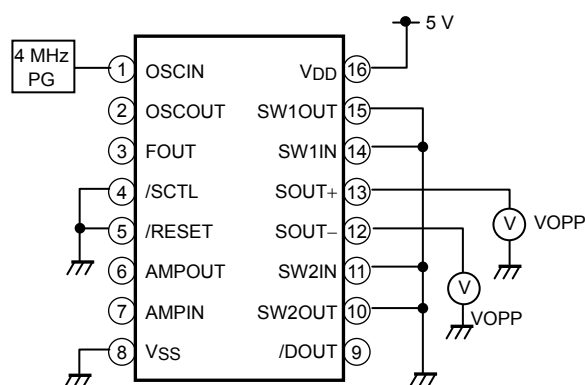


(21) ON-resistance of analog switch 1

ON-resistance of analog switch 2

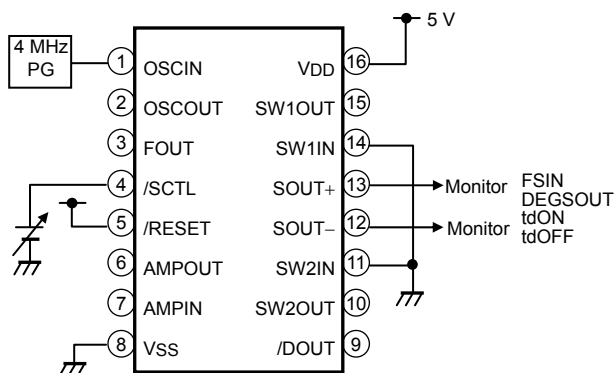


(22) Output voltage

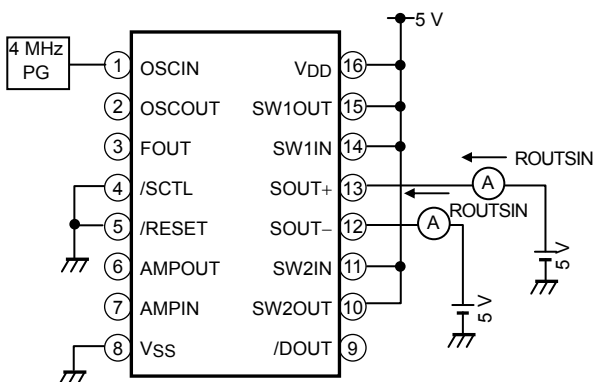


(23) Pseudo sine wave output frequency

Pseudo sine wave output start time
 Pseudo sine wave output stop time



(24) Equivalent output impedance



IC Marking Specification



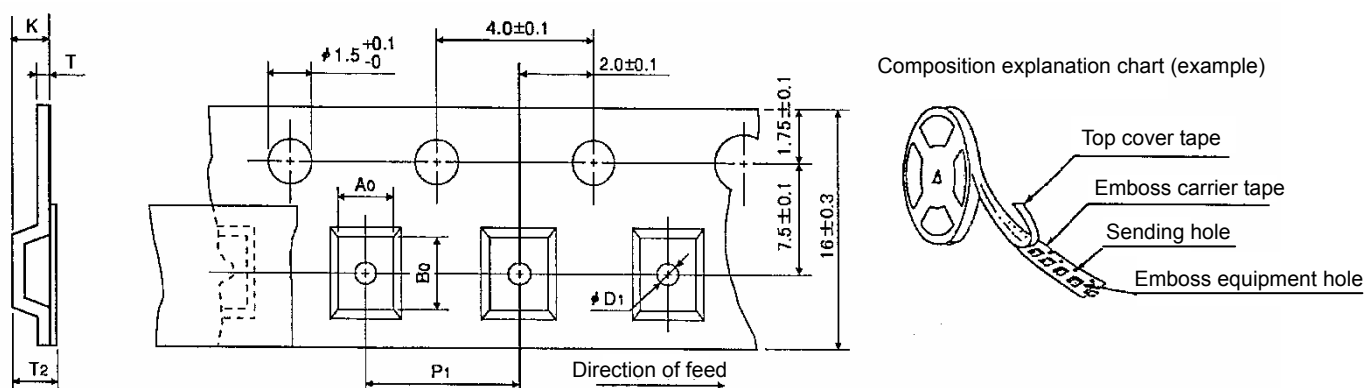
Toshiba CMOS SSOP Embossed Taping - Common Specifications

1. Applicable Scope

This specification defines the embossed taping package specifications and related items for Toshiba flat package CMOS ICs.

2. Specifications

2.1 Tape Form and Dimensions



Unit: mm

| Package Code | A0 | B0 | P1 | T | K | T2 | D1 |
|--------------------|--------------|--------------|--------------|--------------|---------------|----------|---------------|
| SSOP16-P-225-0.65B | 6.8 ± 0.1 | 5.5 ± 0.1 | 8.0 ± 0.1 | 0.3 ± 0.1 | 2.15 ± 0.3 | 2.45 MAX | 1.65 ± 0.1 |

Note: The maximum value of K dimensions is adopted in the table though the one that the tape thickness was added to K dimensions becomes T2 dimensions.

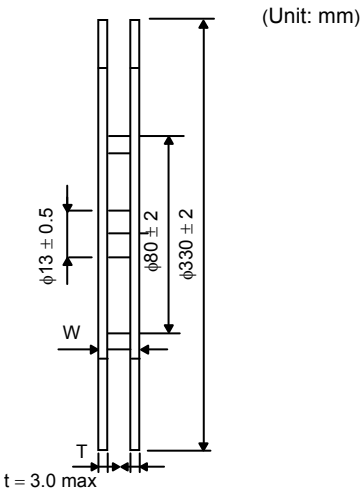
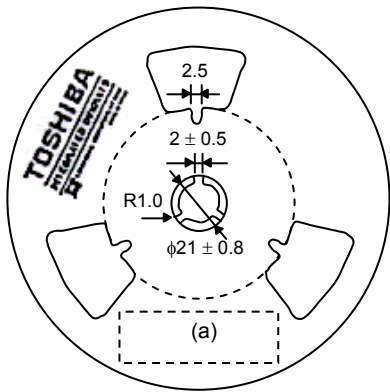
(The Tape thickness is considered within the range of the allowance of K dimensions.)

2.2 Seal Tape Dimensions

Unit: mm

| | Tape Width | Tape Thickness |
|--------------------|------------|----------------|
| SSOP16-P-225-0.65B | 13.5 | 0.06 |

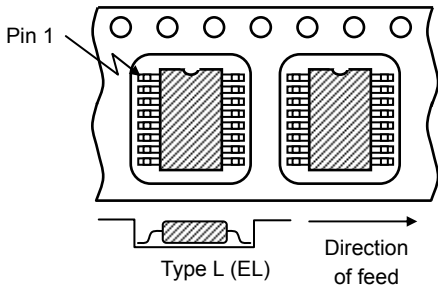
2.3 Reel Form and Dimensions



| | | |
|-------------|--------------------|---|
| Unit: mm | | |
| W dimension | SSOP16-P-225-0.65B | $16.4 \begin{smallmatrix} +2.0 \\ -0 \end{smallmatrix}$ |

(a) Bar code label (See page 18)

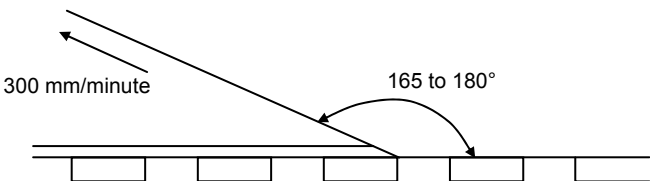
2.4 Insertion Direction



2.5 Tape Minimum Bending Radius

The strength of the seal tape shall not change even when an IC is inserted into the tape and the tape is bent 40 mm. In addition, the tape and inserted IC shall not change under the corresponding conditions.

2.6 Seal Tape Peeling Strength

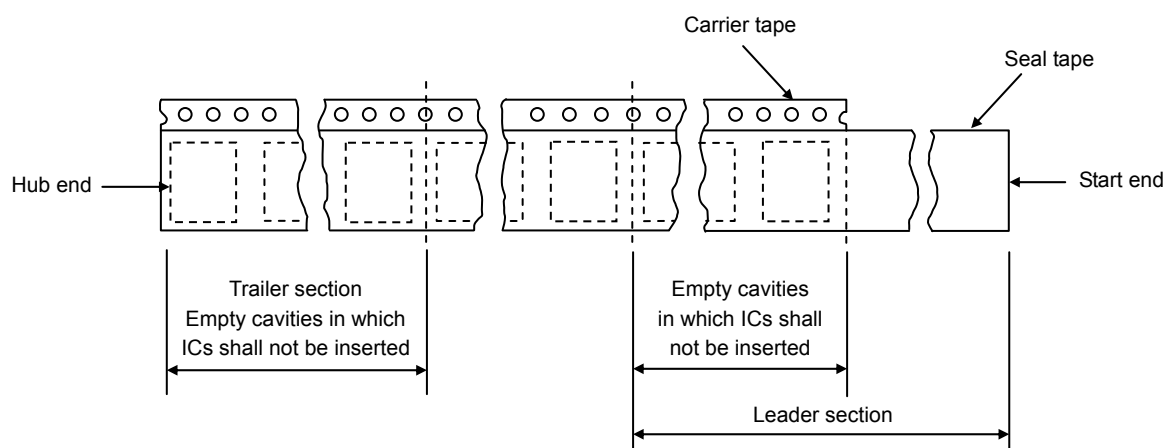


The seal tape shall maintain a peeling strength of 0.1 N (10 gf) when tape bonding surface is at 165 to 180° and being pulled at a speed of 300 mm per minute. However, the seal tape shall not fracture or break when it is being peeled.

2.7 Leader and Trailer Sections of the Tape

Empty cavities shall be created in leader and trailer sections of the tape in which ICs shall not be inserted as specified below:

| | Seal Tape | Carrier Tape |
|-----------------|-------------------|-------------------|
| Leader section | Minimum of 500 mm | Minimum of 400 mm |
| Trailer section | Minimum of 400 mm | Minimum of 400 mm |



2.8 IC Insertion Failure Ratio

| Item | Tolerated Ratio | Comments |
|-----------------------------------|--------------------------|--|
| Consecutive insertion failure | None | Does not apply to the empty cavities in the leading and trailing sections of the tape. |
| Non-consecutive insertion failure | 0.1 % or less (per reel) | |

3. Standard Packaging Unit

The standard packaging unit for one reel of tape shall be 2000 units.

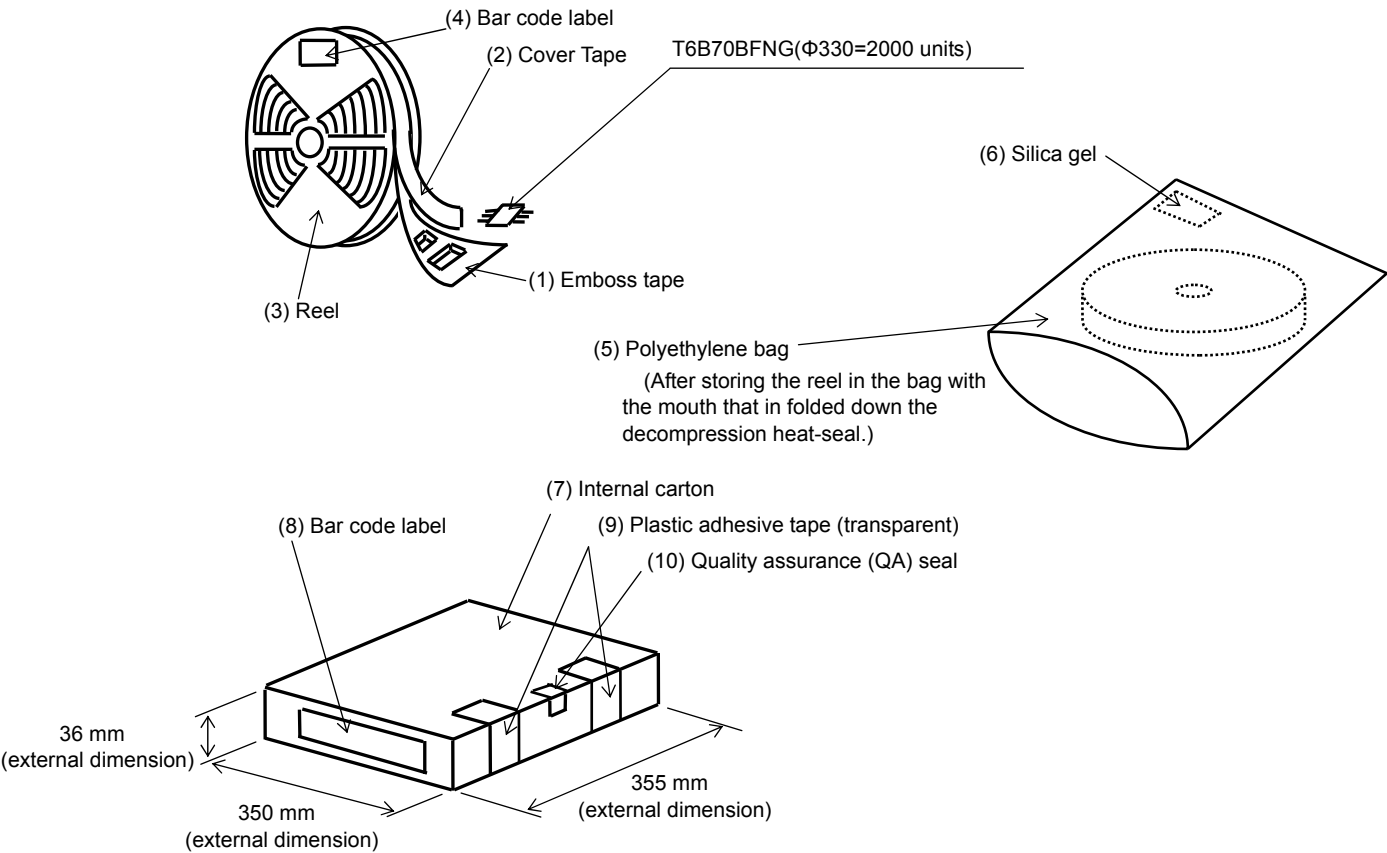
4. Labeling

The reel shall be labeled with the following:

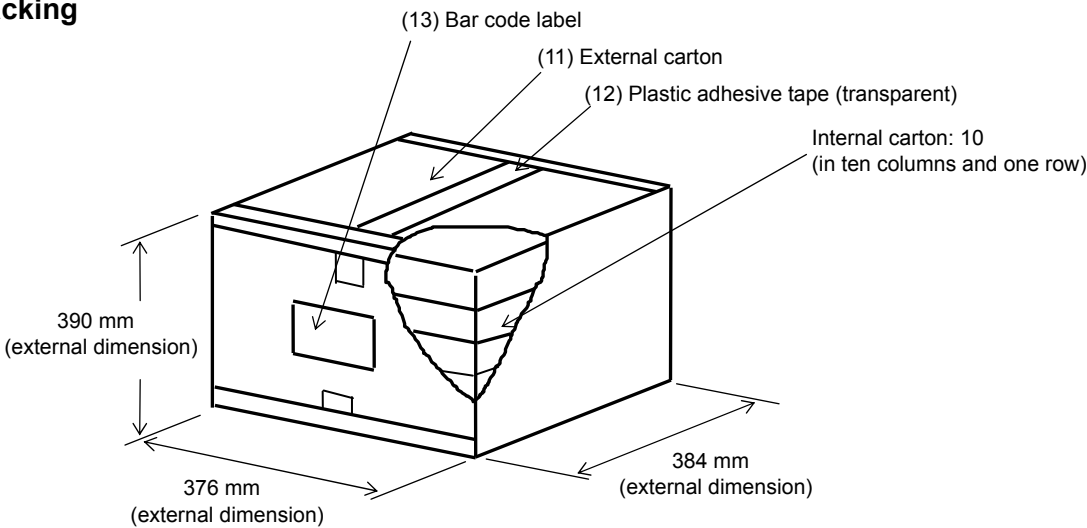
- 1) Product Name
- 2) Quantity
- 3) Lot No.

5. Boxing

Internal packing



External packing



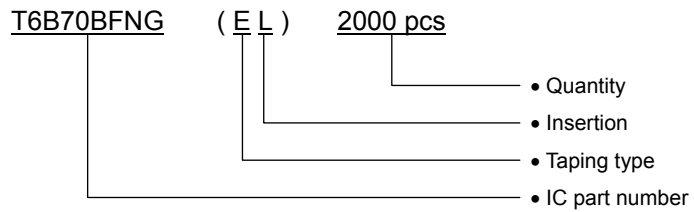
Bar code label

| | | | |
|---------------------------|-------------|----------------------|--|
| P/N: | | TOSHIBA | |
| TYPE | T6B70BFNG | SEALED Mmm, dd, yyyy | |
| ADDC (EL) | Q'TY xxxpcs | DIFFUSED IN JAPAN | |
| XXXXXX | 58F | ASSEMBLED IN JAPAN | |
| [[G]]/RoHS COMPATIBLE | | BARCODE SAMPLE | |
| (Y)401H7425xxxxxxXUzzzzzz | | *** | |

6. Issuing Purchase Orders

When issuing IC purchase orders using the taping packaging information, be sure to include the product name, taping type, insertion direction and quantity as follows:

Example:

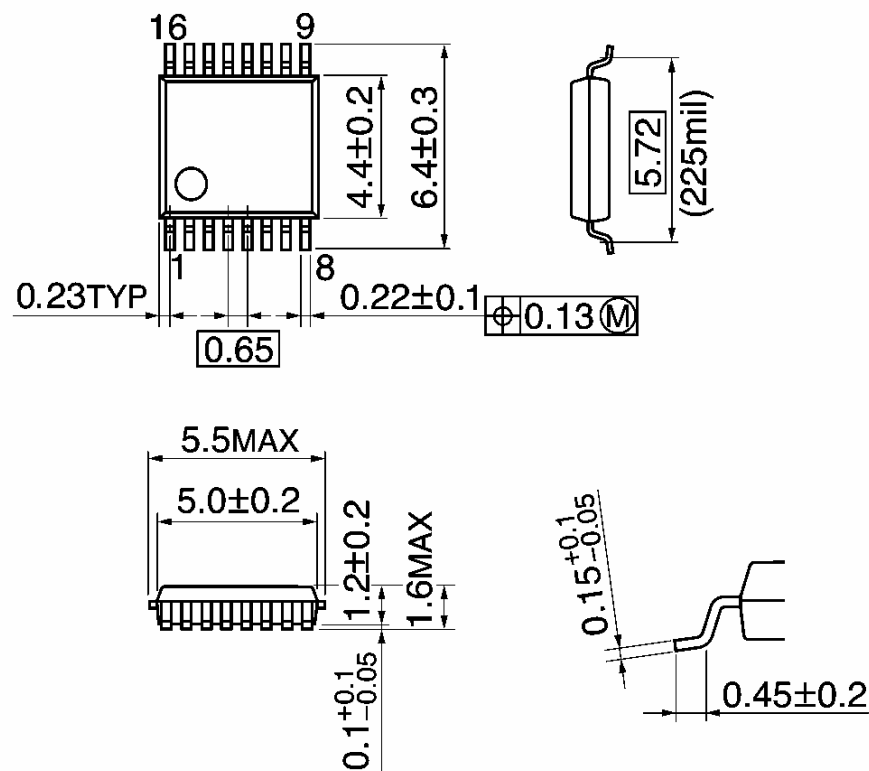


7. Delivery and Storage Precautions

Tape reels should be delivered with enough care so as to prevent extreme vibration from impacting the product. Tape reels should be kept out of direct sunlight and be kept below 45°C during delivery and storage so as to prevent wearing down the peeling strength of seal tape and/or causing other deformities to the tape.

Package Dimensions

SSOP16-P-225-0.65B



Weight: 0.07 g (typ.)

About solderability, following conditions were confirmed

- Solderability

- (1) Use of Sn-37Pb solder Bath

- solder bath temperature = 230°C
 - dipping time = 5 seconds
 - the number of times = once
 - use of R-type flux

- (2) Use of Sn-3.0Ag-0.5Cu solder Bath

- solder bath temperature = 245°C
 - dipping time = 5 seconds
 - the number of times = once
 - use of R-type flux

RESTRICTIONS ON PRODUCT USE

070711EBA

- The information contained herein is subject to change without notice.
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..
- The TOSHIBA products listed in this document are designed and manufactured for usage in hot water dispensers. Do not use any of these products for any purposes other than hot water dispensers, unless otherwise agreed in writing by TOSHIBA.
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