AS1370

High Voltage, Low Quiescent Current, 200mA LDO

General Description

The AS1370 low-power, positive voltage regulator is designed to deliver up to 200mA, while consuming only 3µA of quiescent current. The device is available in fixed output voltages between 1.2V and 5.5V (programmable in 100mV steps). Standard options of 1.2, 1.8, 2.5, 3.0, 3.3, 4.5, 5.0 and 5.5V are also available. The input voltage ranges from 2.6V to a maximum of 50V. Operation with large input to output differential voltages is limited by the maximum power dissipation available from package and environment.

The very-low dropout voltage (550mV @ 200mA load) prolongs battery life and allows high current in small applications with minimum input-to-output voltage differentials. The device features very stable output voltage (using only 1µF ceramic capacitor), and excellent line- and load-regulation. The AS1370 also features a Power-OK Output. The device features integrated short-circuit and over current protection. Thermal Protection shuts down the device when die temperature reaches 170°C. This is a useful protection when the device is under sustained short circuit conditions.

The AS1370 is available in an 8-Pin MLPD 3mm x 3mm package and is qualified for -40°C to 125°C operation.

Ordering Information and *Content Guide* appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS1370, High Voltage, Low Quiescent Current, 200mA LDO are listed below:

Figure 1:
**Added Value of Using AS1370**

Benefits	Features
• Ideal for industrial or automotive applications	• Input voltage from 2.6V to 50V • Operating temperature from -40°C to 125°C
• Ideal for a battery-driven always-on regulator	• Very low quiescent current of 3µA
• Supports a variety of end applications	• Guaranteed output current of 200mA • Output voltage from 1.2V to 5.5V • Power-OK indication

Benefits	Features
• Over-temperature and over-current protection and shutdown	• Integrated temperature and output power monitoring
• Cost-effective, small PCB area needed	• Less external components needed • Small 8-pin MLPD 3mm x 3mm package

Applications

The wide input voltage range, low quiescent current and high-accuracy output voltage make the devices perfectly suited for a wide variety of industrial sensors, automotive and battery-powered applications, where the regulators have to be always on. The devices are also ideal for many other industrial applications.
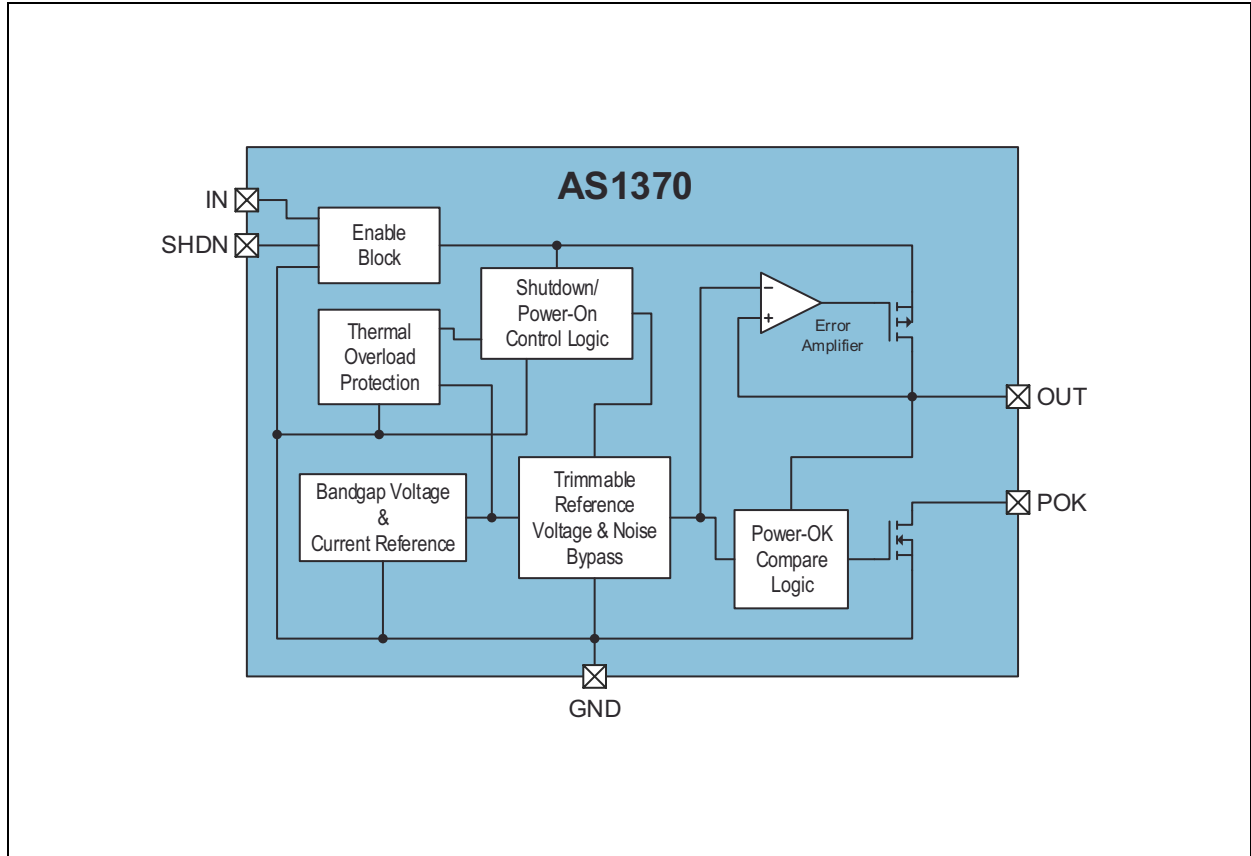
Figure 2:
AS1370 Typical Application Diagram
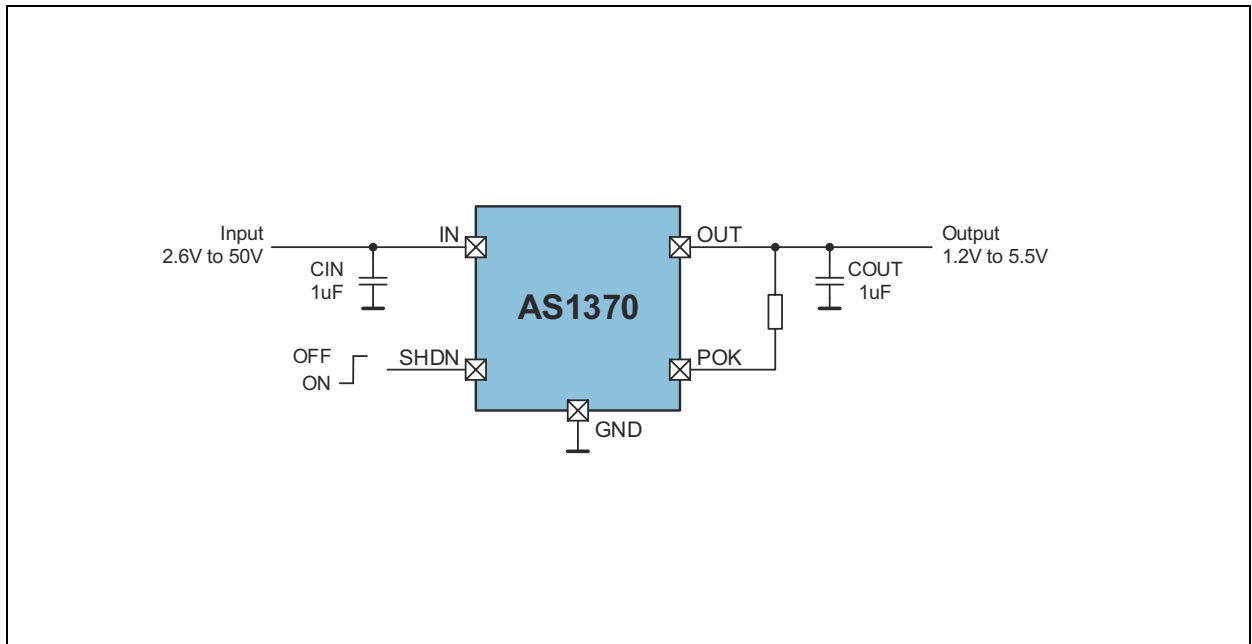
Block Diagram

The functional blocks of this device are shown below:

Figure 3:
AS1370 Block Diagram

Pin Assignment

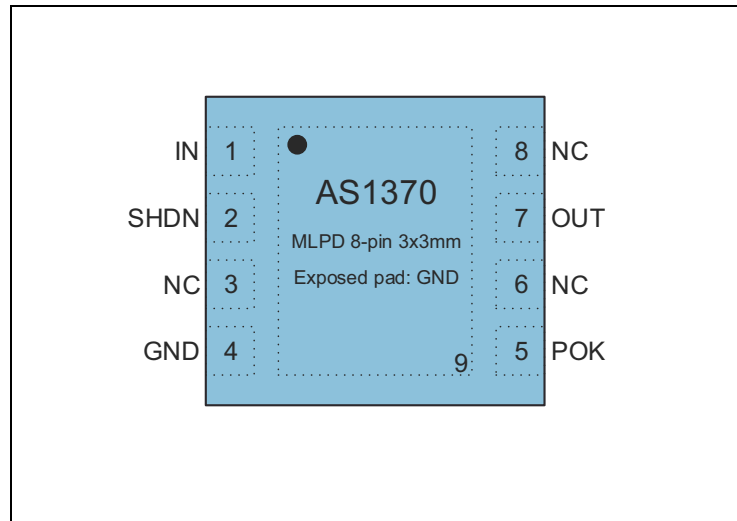| Pin Name	Pin Number	Description
IN	1	**Unregulated Input Voltage.** This pin should be connected to the positive terminal of the input capacitor. Bypass with 1µF capacitor to GND. Input voltage can range from 2.6V to 50V.
SHDN	2	**Active-High Shutdown Input.** A logic high reduces the ground pin current to < 1µA. Connect this pin to GND for normal operation.
NC	3	**Not Connected.** This pins must be not connected.
GND	4	**Ground.**
POK	5	**Power-OK Output.** Active-low, open-drain output indicates an out-of-regulation condition. Connect a 100kΩ pull-up resistor to pin OUT for logic levels. Leave this pin unconnected if the Power-OK feature is not used.
NC	6	**Not Connected.** This pins is not connected.
OUT	7	**Regulated Output Voltage.** This pin should be connected to the positive side of the load and to the positive terminal of the output capacitor. Current flowing out of this pin is equivalent to a DC load current. Fixed 1.2, 1.8, 2.5, 3.0, 3.3, 4.5, 5.0 and 5.5V output, as well as versions from 1.2V up to 5.5V can be ordered. Bypass with 1µF capacitor to GND.
NC	8	**Not Connected.** This pin is not connected.
Exposed Pad	9	**Exposed Pad.** This pin functions as a heat sink. Solder it to a large pad or to the circuit-board ground plane to maximize power dissipation.

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
Electrical Parameters				
IN	-0.9	+55	V	
SHDN	-0.3	$V_{IN} + 0.3$	V	
OUT	-0.3	$V_{IN} + 0.3$	V	
POK	-0.3	$V_{OUT} + 0.3$	V	
Latch-Up Immunity	-100	+100	mA	
Electrostatic Discharge				
Electrostatic Discharge HBM	±1.5		kV	MIL 883 E method 3015
Temperature Ranges and Storage Conditions				
Thermal Resistance θ$_{JA}$	36		°C/W	Junction-to-ambient thermal resistance is very dependent on application and board-layout. In situations where high maximum power dissipation exists, special attention must be paid to thermal dissipation during board design.
Operating Temperature Range	-40	125	°C	
Storage Temperature Range	-65	150	°C	
Package Body Temperature	260		°C	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Relative Humidity (non-condensing)	5	85	%	
Moisture Sensitivity Level	1			Represents a max. floor life time of "Unlimited"

Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

V_{IN} = $V_{OUT(NOMINAL)}$ + 1V, or V_{IN} = 2.6V (whichever is greater), SHDN = GND, C_{IN} = C_{OUT} = 1µF, I_{OUT} = 100µA; T_{AMB} = -40°C to 125°C (unless otherwise specified); typical values are at T_{AMB} = 25°C.

Figure 7:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input voltage		2.6		50	V
V_{OUT}	Output voltage		1.2		5.5	V
Acc	DC output voltage accuracy	T_{AMB} = 25°C	-1		+1	%
		T_{AMB} = -40°C to 125°C, I_{OUT} = 100µA to 200mA	-4		+4	
I_{LIM}	Short circuit current		230	370		mA
I_Q	Ground pin current	I_{OUT} = 0mA		3	8	µA
		I_{OUT} = 200mA		3.7		
		T_{AMB} = 85°C, I_{OUT} = 0mA			6.7	
VDROP	Dropout voltage[1]	I_{OUT} = 100mA		280	600	mV
		I_{OUT} = 200mA		550		
		T_{AMB} = 85°C, I_{OUT} = 100mA			500	
ΔV_{LNR}	Line regulation[2]	V_{IN} = $V_{OUT(NOMINAL)}$ + 1V to 50V	-0.05		+0.05	%/V
ΔV_{LDR}	Load regulation	I_{OUT} = 1mA to 200mA		0.01		%/mA
PSRR	Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 10mA		50		dB

| Symbol	Parameter	Conditions	Min	Typ	Max	Units
Shutdown[3]						
t_{ON}	Exit delay from shutdown[4]			1.25	5	ms
I_{OFF}	Shutdown current	SHDN = V_{IN}		0.6	1.2	µA
V_{IH}	Shutdown digital input threshold	SHDN decreasing	1.6			V
V_{IL}		SHDN increasing			0.4	
I_{SHDN}	Shutdown input bias current	SHDN = V_{IN}		0.1	30	nA
Power-OK Output						
V_{POK}	Power-OK voltage threshold	V_{OUT} falling	93	95	97	% V_{OUT}
		Hysteresis		1		
I_{POK}	Power-OK leakage current	$0 \leq V_{POK} \leq V_{OUT}$, V_{OUT} in regulation			50	nA
Thermal Protection						
T_{SHDN}	Thermal shutdown temperature			170		ºC
ΔT_{SHDN}	Thermal shutdown hysteresis			15		ºC

Note(s):

1. Dropout voltage = V_{IN} - V_{OUT} when V_{OUT} is 100mV < V_{OUT} for V_{IN} = $V_{OUT(NOMINAL)}$ +1V (applies only to output voltages $\geq$ 2.6V).

2. $V_{OUT(NOMINAL)} \geq 1.6$V.

3. The rise and fall time of the shutdown signal must not exceed 100ns.

4. The delay time is defined as time required to set V_{OUT} to 95% of its final nominal value.
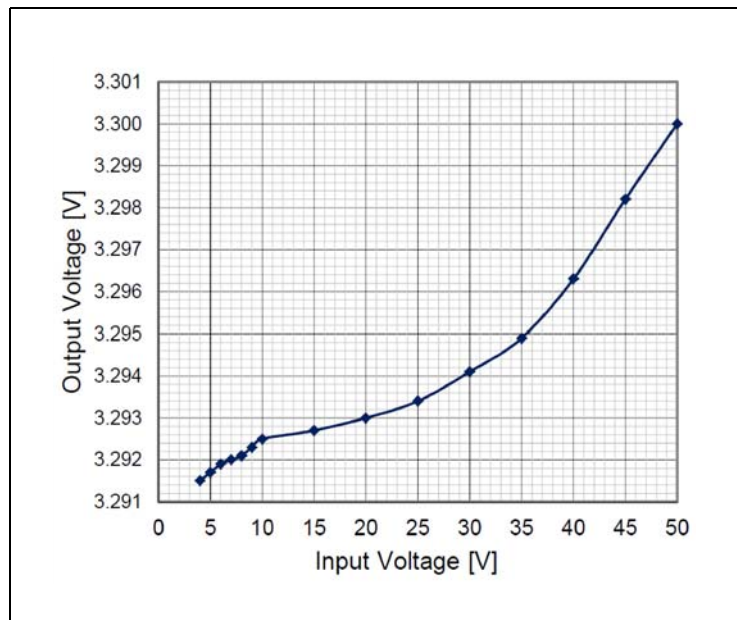
Typical Operating Characteristics

$V_{OUT(NOMINAL)}$ = 3.3V, V_{IN} = 4.3V, I_{OUT} = 100µA, C_{IN}=C_{OUT} = 1µF; typical values are at T_{AMB} = 25°C (unless otherwise specified).
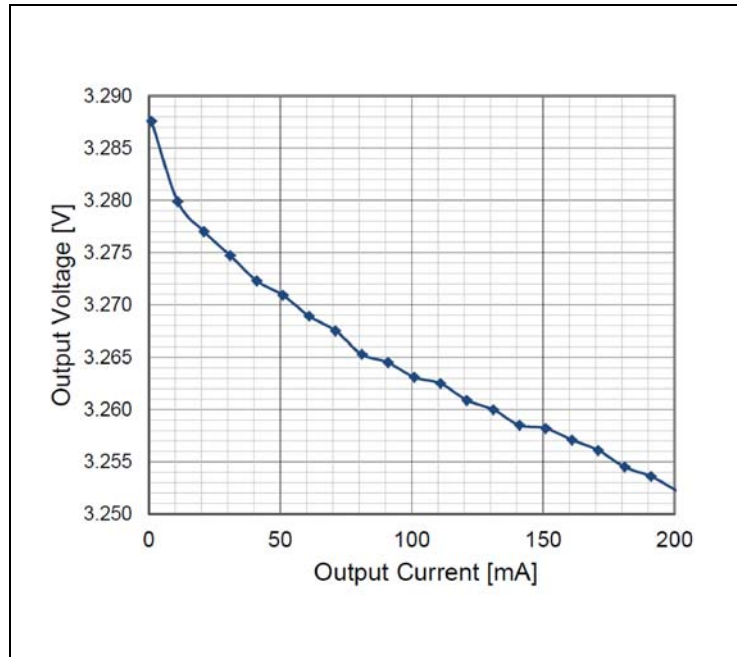
Figure 8:
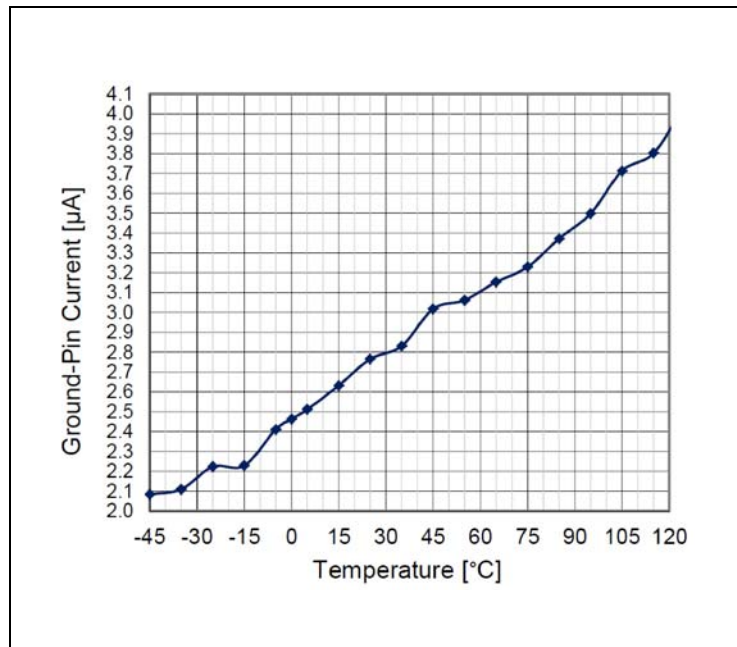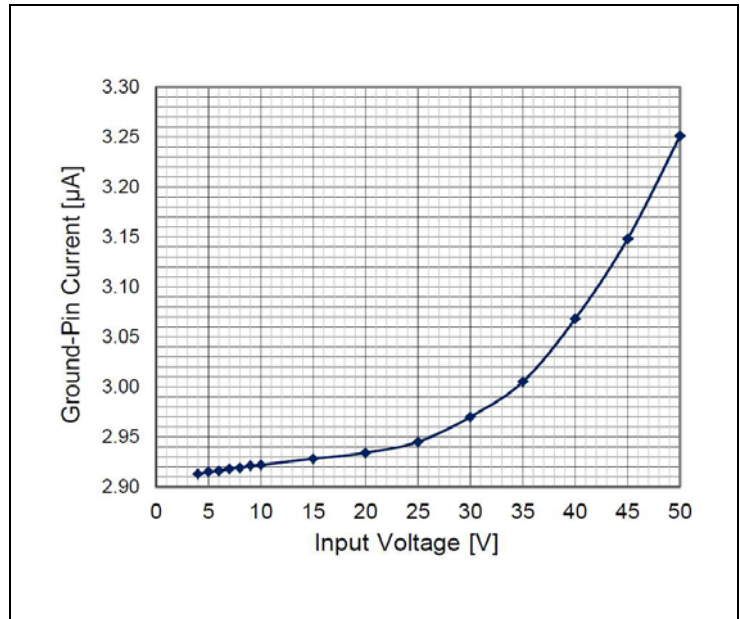**Output Voltage vs. Temperature**
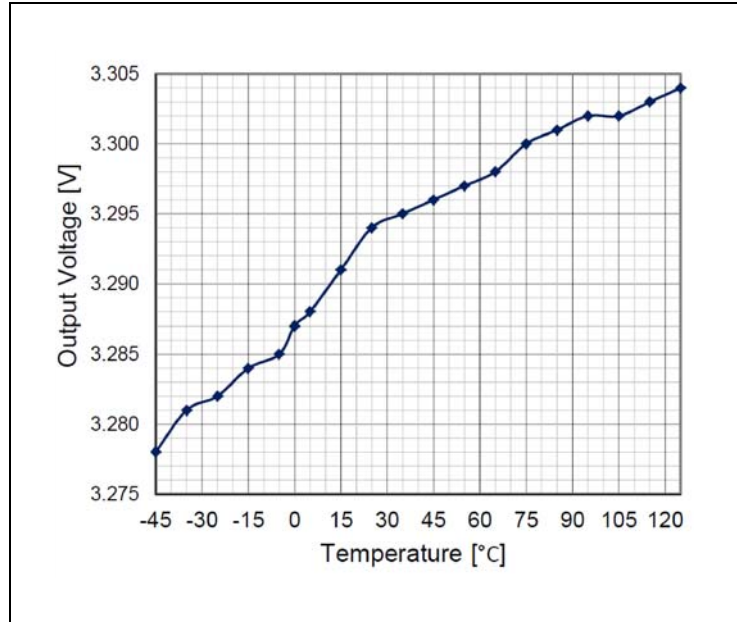
Figure 9:
Line Regulation
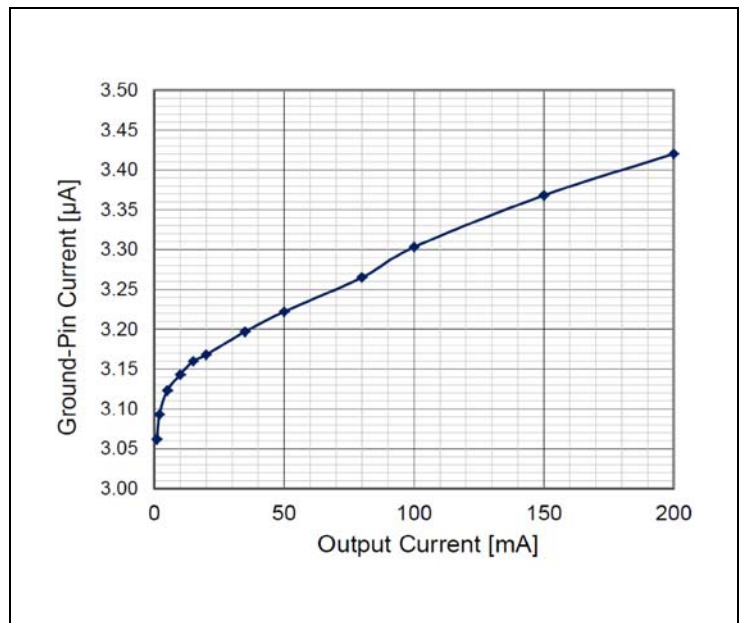
Figure 10:
Load Regulation

Figure 11:
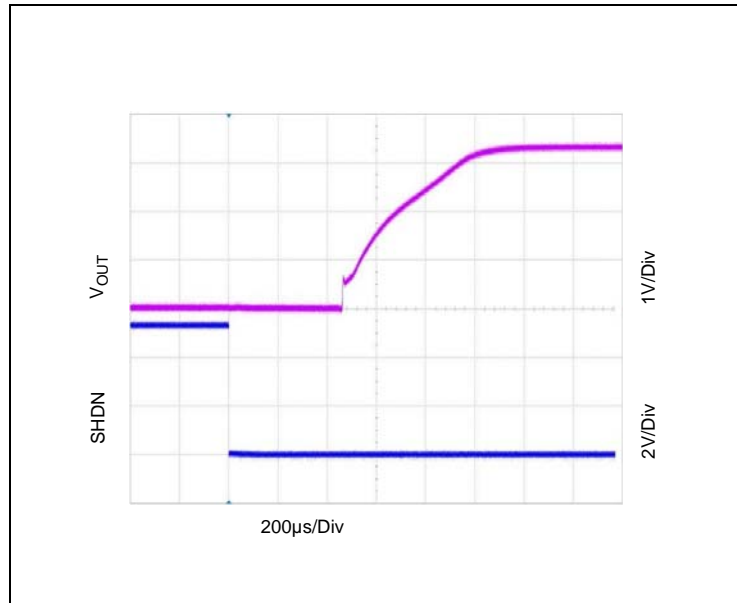**Ground Pin Current vs. Temperature**

Figure 12:
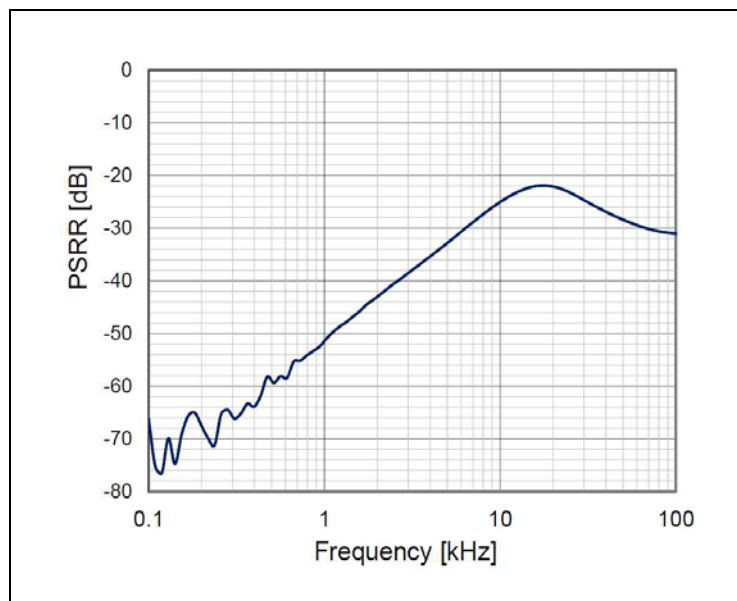**Ground Pin Current vs. Input Voltage**

Figure 13:
Ground Pin Current vs. Output Current

Figure 14:
Exit Delay from Shutdown

Figure 15:
Power Supply Ripple Rejection vs. Frequency, I_OUT = 10mA

Detailed Description

The AS1370 is a low-dropout, low-quiescent-current linear regulators intended for LDO regulator applications where output current load requirements range from no load to 200mA.

The AS1370 also features a Power-OK output to indicate when the output is within 5% of final value, and also a Shutdown pin. Shutdown current for the whole regulator is typically 600nA. The device features integrated short-circuit and over current protection. Undervoltage lockout prevents erratic operation when the input voltage is slowly decaying (e.g. in a battery powered application). Thermal protection shuts down the device when die temperature reaches 170°C. This is a useful protection when the device is under sustained short circuit conditions.

Figure 3 shows the block diagram of the AS1370. It identifies the basics of a series linear regulator employing a P-Channel MOSFET as the control element. A stable 1.2V voltage reference (REF in Figure 3) is compared with an attenuated sample of the output voltage. Any difference between the two voltages (reference and sample) creates an output from the error amplifier that drives the series control element to reduce the difference to a minimum. The error amplifier incorporates additional buffering to drive the relatively large gate capacitance of the series pass P-channel MOSFET, when additional drive current is required under transient conditions. Input supply variations are absorbed by the series element, and output voltage variations with loading are absorbed by the low output impedance of the regulator.

Output Voltages

Standard products are factory-set with output voltages from 1.2V. A two-digit suffix of the part number identifies the nominal out (see Ordering Information). Non-standard devices are available. For more information contact www.ams.com/contact.

Power-OK Functionality

The AS1370's Power-OK is built around a N-channel MOSFET.

The Power-OK feature is not active during shutdown and provides a power-on-reset function that can operate down to $V_{IN} = 1.2V$. A capacitor to GND may be added to generate a power-on-reset delay. To obtain a logic-level output, connect a pull-up resistor from pin POK to pin OUT. Larger values for this resistor will help to minimize current consumption; a 100kΩ resistor is perfect for most applications (see Figure 2).

Current Limiting

The AS1370 include current limiting circuitry to protect against short-circuit conditions. The circuitry monitors and controls the gate voltage of the P-channel MOSFET, limiting the output current to 370mA. The P-channel MOSFET output can be shorted to ground for an indefinite period of time without damaging the device.

Thermal-Overload Protection

The devices are protected against thermal runaway conditions by the integrated thermal sensor circuitry. Thermal shutdown is an effective tool to prevent die overheating since the power transistor is the principle heat source in the device.

If the junction temperature exceeds 170°C, the thermal sensor starts the shutdown logic, at which point the P-channel MOSFET is switched off. After the device temperature has dropped by approximately 15°C, the thermal sensor will turn the P-channel MOSFET on again. Note that this will be exhibited as a pulsed output under continuous thermal-overload conditions.

Note(s): The absolute maximum junction-temperature of 170°C should not be exceeding during continual operation.

Application Information

Dropout Voltage

Dropout is the input to output voltage difference, below which the linear regulator ceases to regulate. At this point, the output voltage change follows the input voltage change. Dropout voltage may be measured at different currents and in particular at the regulator maximum one. From this the MOSFET maximum series resistance over temperature is obtained. More generally:

(EQ1) $$V_{DROPOUT} = I_{LOAD} \times R_{SERIES}$$

Dropout is a key specification when the regulator is used in a battery application. The dropout performance of the regulator defines the useful "end of life" of the battery before replacement or re-charge is required.

Figure 16:
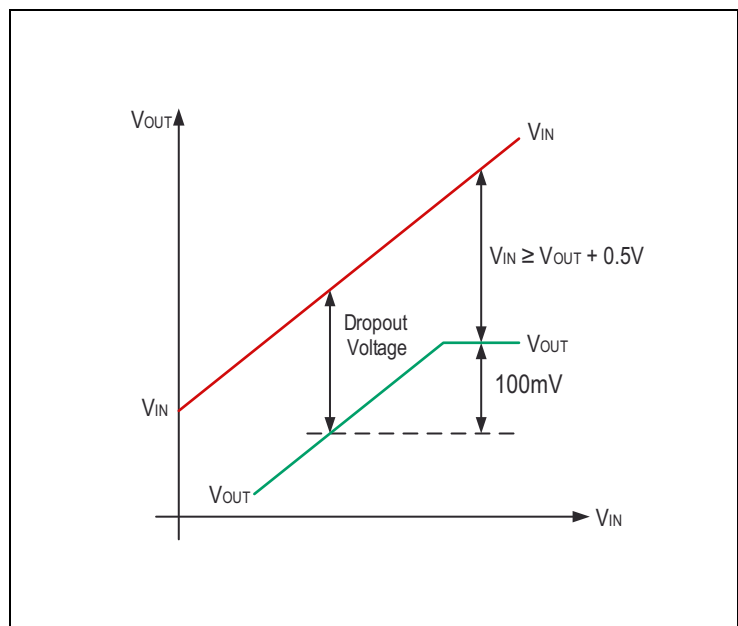**Graphical Representation of Dropout Voltage**

Figure 16 shows the variation of V_{OUT} as V_{IN} is varied for a certain load current. The practical value of dropout is the differential voltage ($V_{OUT} - V_{IN}$) measured at the point where the LDO output voltage has fallen by 100mV below the nominal, fully regulated output value. The nominal regulated output voltage of the LDO is that obtained when there is 500mV (or greater) input-output voltage differential.

Efficiency

Low quiescent current and low input-output voltage differential are important in battery applications amongst others, as the regulator efficiency is directly related to quiescent current and dropout voltage. Efficiency is given by:

(EQ2) $\text{Efficiency} = \dfrac{V_{OUT} \times I_{LOAD}}{V_{IN} \times (I_Q + I_{LOAD})} \times 100 \ \%$

Where:

I_Q = Quiescent current of LDO measured.

Power Dissipation

The power dissipated by the internal series MOSFET *PD$_{(MAX)}$ (Seriespass)* is calculated as:

(EQ3) $PD_{(MAX)} \ (\text{Seriespass}) = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{LOAD(MAX)} \ [W]$

Internal power dissipation *PD$_{(MAX)}$ (Bias),* result of the quiescent current required to bias the internal voltage reference and the error amplifier, is calculated as:

(EQ4) $PD_{(MAX)} \ (\text{Bias}) = V_{IN(MAX)} \times I_Q \ [W]$

The maximum power dissipation *PD$_{(MAX)}$ (Total)* of the LDO is calculated as:

(EQ5) $PD_{(MAX)} \ (\text{Total}) = PD_{(MAX)} \ (\text{Seriespass}) + PD_{(MAX)} \ (\text{Bias}) \ [W]$

Junction Temperature

Under operating conditions, the maximum junction temperature should not exceed 125°C. Regulating the maximum junction temperature requires knowledge of the heat path from junction to case Θ_{JC} [°C/W] fixed by the IC manufacturer, and adjustment of the case to ambient heat path Θ_{CA} [°C/W] by manipulation of the PCB copper area adjacent to the IC position.

Figure 17:
Steady State Heat Flow Equivalent Circuit
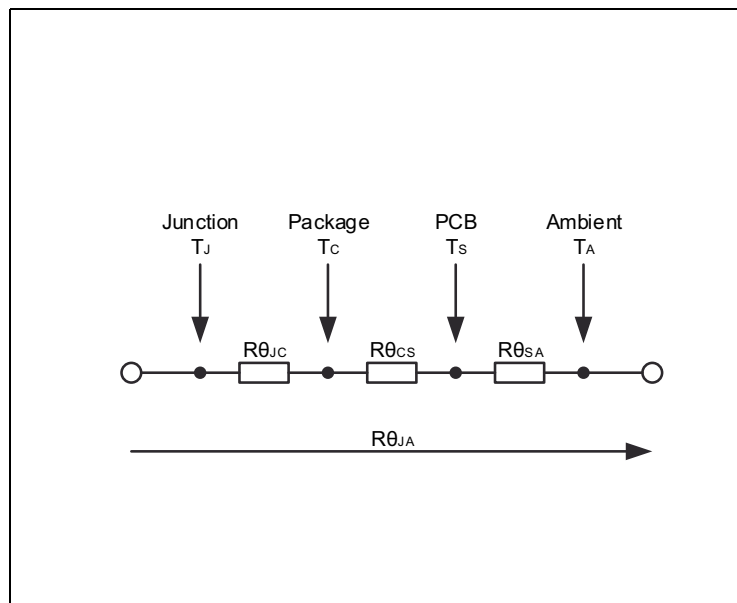
Total Thermal Path Resistance (junction-to-ambient) is determined by:

(EQ6) $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$ [°C/W]

Junction Temperature is determined by:

(EQ7) $T_J = PD_{(MAX)} \times \theta_{JA} + T_{AMB}$ [°C]

Explanation of Steady State Specifications

Line Regulation

Line regulation is defined as the percentual change in output voltage when the input (or line) voltage is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the input voltage changes. More generally:

(EQ8) $\text{Line Regulation} = \dfrac{\Delta V_{OUT}}{\Delta V_{IN}}$ and is a pure number

In practise, line regulation is referred to the regulator output voltage in terms of % / V_{OUT}. This is particularly useful when the same regulator is available with numerous output voltage trim options.

(EQ9) $\text{Line Regulation} = \dfrac{\Delta V_{OUT}}{\Delta V_{IN}} \times \dfrac{100}{V_{OUT}}$ [% / V]

Load Regulation

Load regulation is defined as the change of the output voltage when the load current is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the load changes. Load regulation is a measure of the DC closed loop output resistance of the regulator. More generally:

(EQ10) $\text{Load Regulation} = \dfrac{\Delta V_{OUT}}{\Delta I_{OUT}}$ [Ω]

In practise, load regulation is referred to the regulator output voltage in terms of % / mA. This is particularly useful when the same regulator is available with numerous output voltage trim options.

(EQ11) $\text{Load Regulation} = \dfrac{\Delta V_{OUT}}{\Delta I_{OUT}} \times \dfrac{100}{V_{OUT}}$ [% / mA]

Setting Accuracy

Accuracy of the final output voltage is determined by the reference accuracy and the input offset voltage of the error amplifier. When the regulator is supplied pre-trimmed, the output voltage accuracy is fully defined in the output voltage specification.

The reference tolerance is given both at 25°C and over the full operating temperature range.

Total Accuracy

Away from dropout, total steady state accuracy is the sum of setting accuracy, load regulation and line regulation. Generally:

(EQ12) *Total Accuracy % = Setting Accuracy % + Load Regulation % + Line Regulation %*

Explanation of Dynamic Specifications

Power Supply Rejection Ratio (PSRR)

Known also as Ripple Rejection, this specification measures the ability of the regulator to reject noise and ripple beyond DC. PSRR depends on a summation of the individual rejections of the error amplifier, reference and AC leakage through the series pass transistor. The specification, in the form of a typical attenuation plot with respect to frequency, shows up the gain bandwidth compromises forced upon the designer in low load current conditions. Generally:

(EQ13) $PSSR = 20Log\dfrac{\delta V_{OUT}}{\delta V_{IN}}$ [dB] using lower case δ to indicate AC values

Power supply rejection ratio is fixed by the internal design of the regulator. Additional filtering must be provided externally.

Output Capacitor ESR

The series regulator is a negative feedback amplifier, and as such is conditionally stable. The ESR of the output capacitor is usually used to cancel one of the open loop poles of the error amplifier in order to produce a single pole response; maximum ESR should be less than 500mΩ. Excessive ESR values may actually cause instability by excessive changes to the closed loop unity gain frequency crossover point. The range of ESR values for stability is usually shown either by a plot of stable ESR versus load current, or a limit statement in the datasheet.

Some ceramic capacitors exhibit large capacitance and ESR variations in temperature. Z5U and Y5V capacitors may be required to ensure stability at temperatures below $T_{AMB} = -10°C$. With X7R or X5R capacitors, a 1.0µF capacitor should be sufficient at all operating temperatures.

Larger output capacitor values (>10µF) help to further reduce noise and improve load transient-response, stability and power-supply rejection.

Input Capacitor

An input capacitor at V_{IN} is required for stability. It is recommended that a 1.0µF capacitor be connected between the AS1370 power supply input pin V_{IN} and ground (capacitance value may be increased without limit subject to ESR limits). This capacitor must be located at a distance of not more than 1cm from the V_{IN} pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Noise

The regulator output is a DC voltage with superimposed noise on the output. The noise comes from three sources: the reference, the error amplifier input stage and the output voltage setting resistors. Noise is a random fluctuation: if noise is not minimized in some applications, it will produce system problems.

Load Transient Response

The series regulator is a negative feedback system: therefore any change at the output will take a finite time to be corrected by the error loop. This "propagation time" is related to the bandwidth of the error loop. The initial response to an output transient comes from the output capacitance; during this time, ESR is the dominant mechanism causing voltage transients at the output. More generally:

(EQ14)
$$\delta V_{TRANSIENT} = \delta I_{OUT} \times ESR \quad [V]$$

Thus an initial +50mA change of output current will produce a -12mV transient when the ESR=240mΩ. Remember to keep the ESR within stability recommendations when reducing ESR by adding multiple parallel output capacitors.

After the initial ESR transient, there follows a voltage drop during the time that the LDO feedback loop takes to respond to the output change. This drift is approximately linear in time and sums with the ESR contribution to make a total transient variation at the output of:

(EQ15)
$$\delta V_{TRANSIENT} = \delta I_{OUT} \times \left(ESR + \frac{T}{C_{LOAD}} \right) \quad [V]$$

Where:

C_{LOAD} = load capacitor [F];

T = propagation delay of the LDO [s].

This shows why it is convenient to increase the output capacitor value for a better support for fast load changes. Of course the formula holds for t < "propagation time", so that a faster LDO needs a smaller cap at the load to achieve a similar transient response. For instance, 50mA load current step produces 50mV output drop if the LDO response is 1µs and the load cap is 1µF.

There is also a steady state error caused by the finite output impedance of the regulator. This is derived from the load regulation specification discussed above.

Turn On Time

This specification defines the time taken for the LDO to awake from shutdown. The time is measured from the release of the shutdown pin to the time that the output voltage is within 5% of the final value. It assumes that the voltage at V_{IN} is stable and within the regulator min and max limits. Shutdown reduces the quiescent current to very low, mostly leakage values (<1µA typ.).

Thermal Protection

To prevent operation under extreme fault conditions, such as a permanent short circuit at the output, thermal protection is built into the device. Die temperature is measured, and when a 170°C threshold is reached, the device enters shutdown. When the die cools sufficiently, the device will restart (assuming input voltage exists and the device is enabled). Hysteresis of 15°C prevents low frequency oscillation between start-up and shutdown around the temperature threshold.

Package Drawings & Markings

The device is available in a 8-Pin MLPD 3mm x 3mm package.

Figure 18:
Drawings and Dimensions

Symbol	Min	Nom	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20 REF	
L	0.30	0.40	0.50
b	0.23	0.30	0.38
D		3.00 BSC	
E		3.00 BSC	
D2	2.23	2.38	2.48
E2	1.49	1.64	1.74
e		0.65 BSC	
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
N		8	
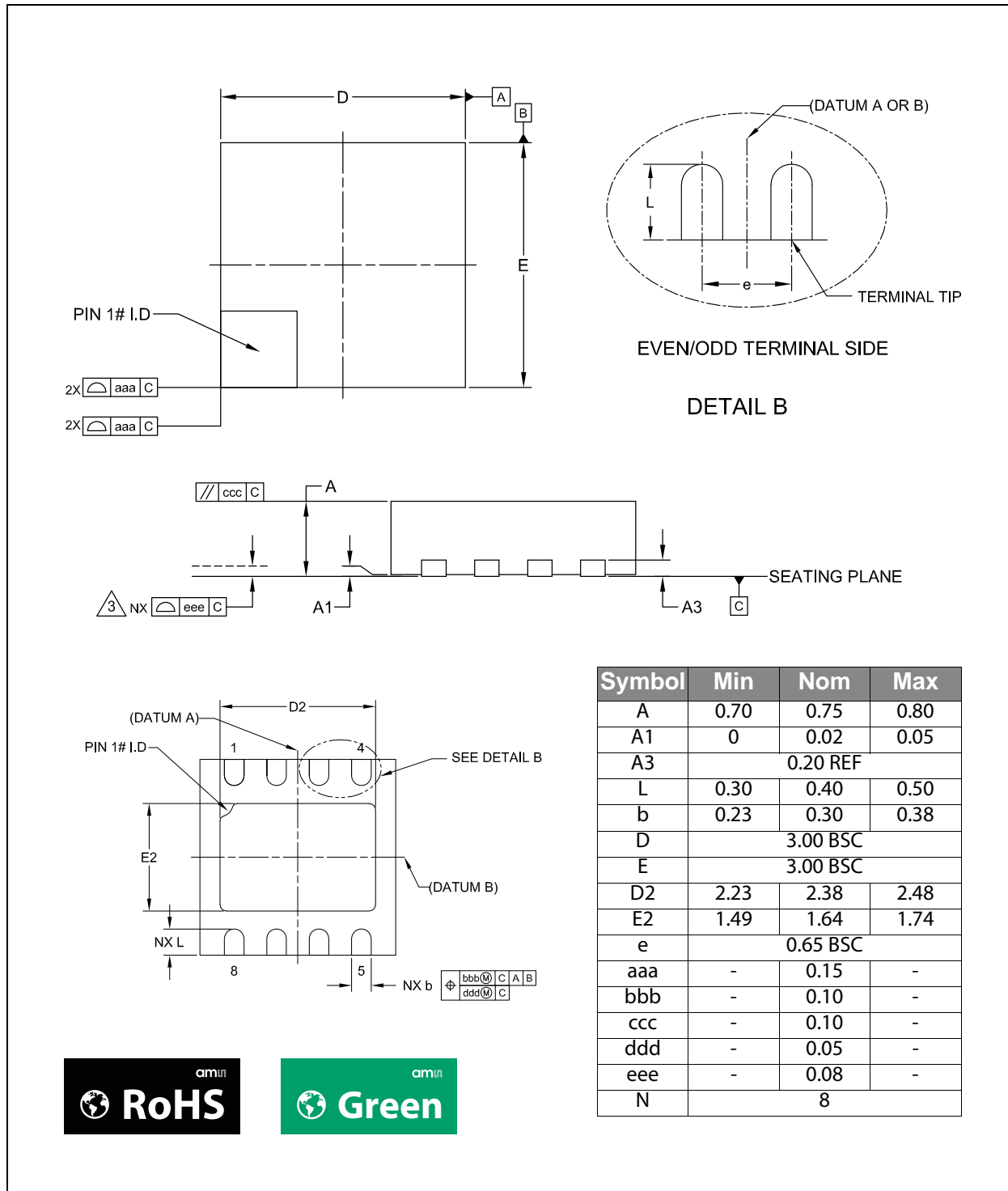
Note(s):

1. Dimensions and tolerancing conform to *ASME Y14.5M-1994*.

2. All dimensions are in millimeters. Angles are in degrees.

3. Coplanarity applies to the exposed heat slug as well as the terminal.

4. Radius on terminal is optional.

5. N is the total number of terminals.

Figure 19:
8-Pin MLPD 3mm x 3mm Marking
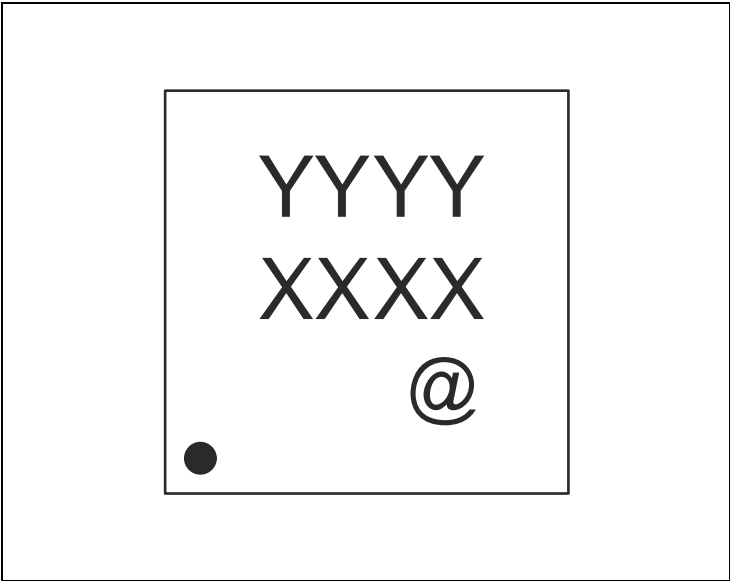
YYYY
XXXX
@

Figure 20:
Packaging Code

YYYY	XXXX	@
Marking Code	Tracecode	Sublot Identifier

Ordering & Contact Information

The device is available as the standard products listed in Figure 21.

Figure 21:
Ordering Information

Ordering Code	Output Voltage	Package	Marking Code	Delivery Form	Delivery Quantity
AS1370-ATDT-27	2.7V	8-Pin MLPD 3mm x 3mm	ASV1	Tape & Reel	1000 pcs/reel
AS1370-ATDT-28	2.8V	8-Pin MLPD 3mm x 3mm	ASV2	Tape & Reel	1000 pcs/reel
AS1370-ATDT-33	3.3V	8-Pin MLPD 3mm x 3mm	ASQA	Tape & Reel	1000 pcs/reel
AS1370-ATDT-SAMPLE[1]	XX[1]	8-Pin MLPD 3mm x 3mm	ASQK	Tape & Reel	1000 pcs/reel

Note(s):

1. Non-standard devices are available between 1.2V and 5.5V in 100mV steps.

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Revision Information

Changes from1.11 (2014-Jan-04) to current revision 2-00 (2016-Jun-01)	Page
Content was updated to the latest **ams** design	
Added benefits to Key Features	1
Updated Package Drawings & Markings section	21

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.

2. Correction of typographical errors is not explicitly mentioned.

Content Guide