LIN SBC with Voltage Regulator and Watchdog E520.34 / .35

PRODUCTION DATA – May 20, 2015

RoHS compliant

Features

- System basis chip (SBC) for LIN applications LIN transceiver V2.1, V2.2, SAE-J2602, ISO9141
- Operating range 5V up to 28V, limited operating range 3.8V up to 40V
- typ. 10µA sleep current consumption
- 3.3V or 5.0V 2% in active mode, 5% in standby
- Peripheral Supply up to 100mA
- Flash mode
- TXD permanent dominant timeout
- Configurable µC window watchdog
- Very low bus leakage current in case of short to GND in sleep mode
- Edge triggered LIN remote wake-up
- VBAT 6:1 voltage divider
- BUS pin ESD-protected > 8 kV (IEC-61000-4-2)

Applications

Smart applications connected to the LIN bus

General Description

The LIN-SBC with voltage regulator provides a LIN transceiver, the peripheral supply, reset generation for the µC and a watchdog.

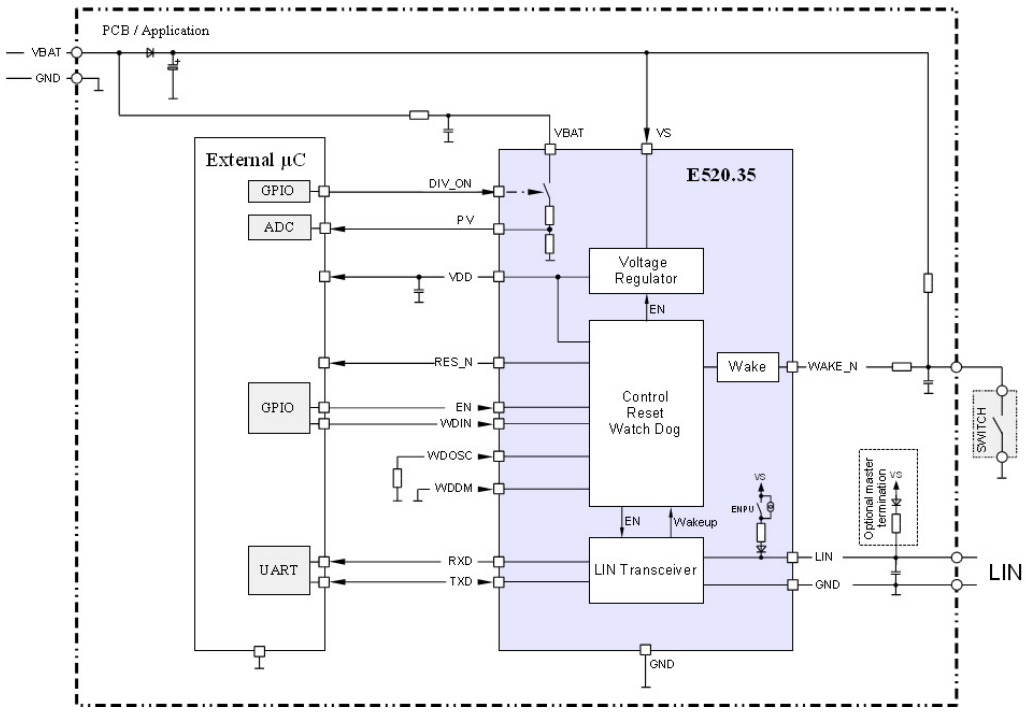
The LIN SBC can be switched into standby- and sleep-mode which provides very low current consumption.

The device is capable to detect local and remote wake-up events to enable the voltage regulator.
A flash mode provides higher data rate for end of line flashing.

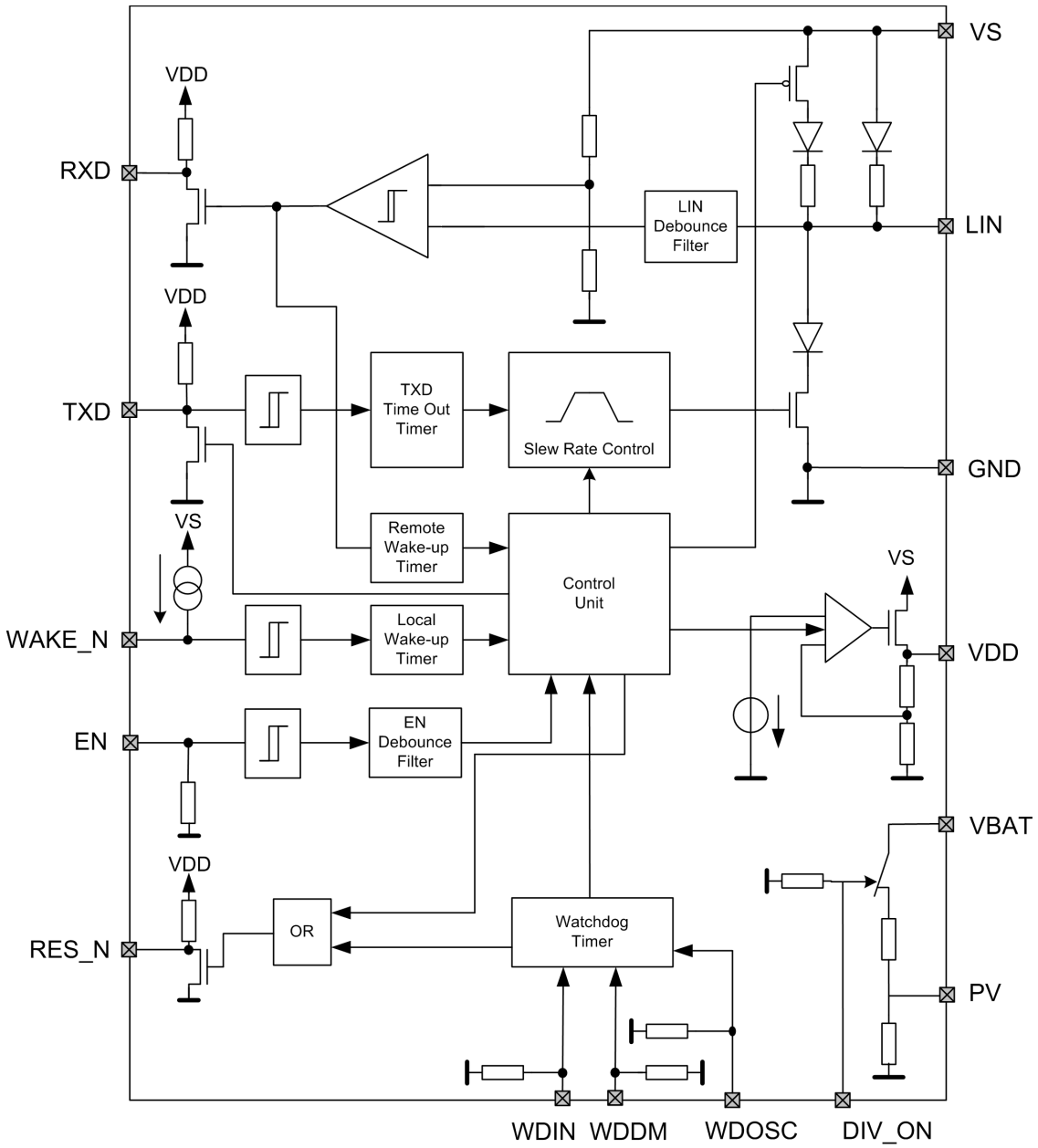
Ordering Information

Ordering No.:	VDD voltage	*Temp. Range*	Package
E52034C62C	3.3V	-40°C to +125°C	QFN20L5
E52035B62C	5.0V	-40°C to +125°C	QFN20L5

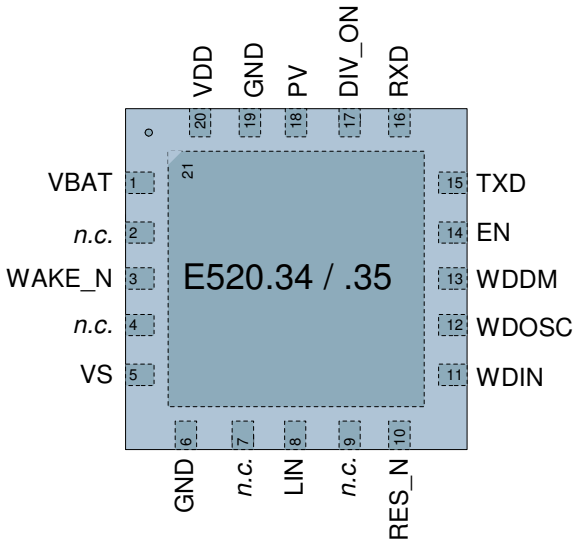
Typical Application Circuit



Functional Diagram



Pin Configuration



Note: Top view, not to scale.

Pin Description

Pin	*Name*	*Type*	*Description*
1	VBAT	HV_S	Battery supply sense input for the voltage divider
2	n.c.		not connected
3	WAKE_N	A_I	local wake up input, low active
4	n.c.		not connected
5	VS	HV_S	battery supply voltage
6	GND	HV_S	ground
7	n.c.		not connected
8	LIN	HV_A_IO	LIN bus terminal
9	n.c.		not connected
10	RES_N	D_O	reset output, low active
11	WDIN	D_I	watchdog trigger input
12	WDOSC	A_I	watchdog cycle time configuration
13	WDDM	D_I	watchdog debug mode
14	EN	D_I	enable input
15	TXD	D_IO	data transmit input
16	RXD	D_O	receive data output
17	DIV_ON	D_I	input to switch on the internal voltage divider, active high
18	PV	A_O	voltage divider output
19	GND	S	ground
20	VDD	S	peripheral voltage supply

Note: A = Analog, D = Digital, S = Supply, I = Input, O = Output, B = Bidirectional, HV = High Voltage

1 Absolute Maximum Ratings

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. **These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied.** Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltages with respect to ground. Currents flowing into terminals are positive, those drawn out of a terminal are negative.

Description	Condition	Symbol	Min	Max	Unit
DC voltage at pin VS	continuous	$V_{S,DC}$	-0.3	40	V
Junction temperature	continuous	T_{JUNC}	-40	150	℃
Storage temperature	continuous	T_{STG}	-55	165	℃
DC voltage at pin WAKE_N	continuous, with external R_{WAKE_N}=3.3 kΩ, C_{WAKE_N}=22nF	$V_{WAKE\_N,DC}$	-2	V_S + 0.3	V
DC current at pin WAKE_N	continuous	$I_{WAKE\_N,DC}$	-10	10	mA
DC voltage at pin VDD E520.35 (5.0V device)	continuous	$V_{DD,DC5.0}$	-0.3	5.5	V
DC voltage at pin VDD E520.34 (3.3V device)	continuous	$V_{DD,DC3.3}$	-0.3	3.6	V
DC current at pin VDD	continuous	$I_{DD,DC}$	-130	1	mA
DC input voltage at pin LIN, VBAT	continuous	$V_{LIN,DC}$, $V_{VBAT,DC}$	-24	40	V
TRAN input voltage at pin LIN, VBAT	pulse for max. 500ms	$V_{LIN,TRAN}$ $V_{VBAT,TRAN}$	-27	40	V
DC Voltage Level for pin EN,RES_N,RXD,TXD,WDIN,WDOSC, WDDM, DIV_ON	continuous	$V_{IO,DC}$	-0.3	$V_{DD,DC}$+0.3	V
DC Current Level for pin EN,RES_N,RXD,TXD,WDIN,WDOSC, WDDM, DIV_ON	continuous	$I_{IO,DC}$	-10	1	mA

2 ESD Protection

Description	Condition	Symbol	Min	Max	Unit
ESD protection at pin LIN	AEC-Q100-002 (HBM), C=100pF, R=1.5kΩ chip level	$V_{LIN,ESDHBM}$ to GND	-8	+8	kV
ESD protection at pin VS	AEC-Q100-002 (HBM), C=100pF, R=1.5kΩ chip level	$V_{VSUP,ESDHBM}$ to GND	-8	+8	kV
ESD protection at pin LIN [1)]	IEC 61000-4-2 C=150 pF, R=330Ω	$V_{LIN,ESD}$ to GND	-8	+8	kV
ESD protection at pin VS [1)]	IEC 61000-4-2 C=150 pF, R=330Ω with external $C_{VS,RF}$=100nF	$V_{VSUP,ESD}$ to GND	-8	+8	kV
ESD protection at all pins	AEC-Q100-002 (HBM), C=100pF, R=1.5kΩ chip level	$V_{PIN,ESDHBM}$	-2	+2	kV
ESD protection at pin WAKE_N	AEC-Q100-002 (HBM), C=100pF, R=1.5kΩ chip level	V_{WAKE_N} to GND	-8	+8	kV
ESD protection at pin WAKE_N [1)]	IEC 61000-4-2 with external R_{WAKE_N}=3.3 kΩ, C_{WAKE_N}=22nF	V_{WAKE_N} to GND	-8	+8	kV
ESD protection at all pins	AEC-Q100-011 (CDM), R=1 Ω chip level	$V_{PIN,ESDCDM}$	-500	+500	V
ESD protection at all pins	AEC-Q100-003 (MM), C=200 pF chip level	$V_{PIN,ESDMM}$	-200	+200	V

[1)] verified with capacitor of C_{LIN}=0pF, C_{LIN}=220pF at pin LIN,
$C_{VS,RF}$=100nF at pin VS and
C_{WAKE_N}=22nF, R_{WAKE_N}=3.3kΩ at pin WAKE_N

3 Recommended Operating Conditions

Description	Condition	Symbol	Min	Typ	Max	Unit
Full functional range VDD and LIN within limits		$V_{S,FUNC}$	5	-	18	V
limited functional range, VDD keeps active	I_{DD} > -60mA	$V_{S,FL,LR}$	3.8	-	5	V
limited functional range due to power dissipation and LIN conformity		$V_{S,FL,HR}$	18	-	40	V
ambient temperature		T_{AMB}	-40	-	125	℃
maximum IO current at each pin, if not specified otherwise		$I_{IO,LUP}$	-10	-	10	mA

4 Thermal Characteristics

Description	Condition	Symbol	Min	Typ	Max	Unit
Thermal resistance junction to ambient QFN20L5 package [1)]	according to JEDEC standard JESD-51-5	R_{TJA}	-	22	-	K/W

[1)] Values are based on method according to JEDEC JESD-51-5.

5 Electrical Characteristics

(V_S = +5V to +28V, T_{amb} = -40°C to +125°C, unless otherwise noted.
Typical values are at V_S = +12.0V and T_{amb} = +25°C. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Power Supply and References						
current consumption in active mode	LIN dominant, I_{DD}=0mA	$I_{S,ACT,DOM}$	-	2.5	5	mA
current consumption in active mode	LIN recessive, I_{DD}=0mA	$I_{S,ACT,REC}$	-	1.2	2	mA
standby current	standby mode, $V_S = V_{LIN} = V_{WAKE\_N}$ =13.5V, I_{DD}=0mA, T_J < 85°C	$I_{S,STBY}$	-	70	98	µA
sleep current	sleep mode, LIN recessive, $V_S = V_{LIN} = V_{WAKE\_N}$ =13.5V, $T_J \leq 40$°C	$I_{S,SLEEP,40}$	-	10	20	µA
sleep current	sleep mode, LIN recessive, $V_S = V_{LIN} = V_{WAKE\_N}$ =13.5V, $T_J > 40$ °C	$I_{S,SLEEP}$	-	-	25	µA
sleep current, LIN is neither recessive nor dominant [1)]	sleep mode, LIN is floating $V_S = V_{WAKE\_N}$ =13.5V	$I_{S,SLEEP,LIN}$	-	-	60	µA
SBC Operating Modes						
debounce filter for active mode transition		t_{2AM}	23	25	44	µs
debounce filter for standby mode transition		t_{2STBY}	23	25	44	µs
debounce filter for sleep mode transition		t_{2SLEEP}	23	25	44	µs
debounce filter for flash mode transition		t_{2FM}	2	4	6	µs
flash mode acknowledge pulsewidth		t_{FMACK}	3			µs
flash mode time out		t_{FMTO}	1.2	-	2	ms
delay for switching off the VDD regulator after entering sleep mode		$t_{DD,OFFDEL}$	64	128	-	µs

[1)] not production tested

Electrical Characteristics (continued)

(V_S = +5V to +28V, Tamb = -40°C to +125°C, unless otherwise noted.
Typical values are at V_S = +12.0V and Tamb = +25°C. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Reset Parameters						
power on reset according to pin VS		$V_{S,POR}$	4.0	-	5.0	V
power down threshold according to pin VS		$V_{S,PD}$	3.0	-	3.8	V
reset assert level at pin VDD E520.34 (3.3V device)		$V_{DD,RSTA3.3}$	2.4	-	2.8	V
reset assert level at pin VDD E520.35 (5.0V device)		$V_{DD,RSTA5.0}$	4.2	-	4.6	V
reset release level at pin VDD E520.34 (3.3V device)		$V_{DD,RSTD3.3}$	2.6	-	3.0	V
reset release level at pin VDD E520.35 (5.0V device)		$V_{DD,RSTD5.0}$	4.4	-	4.8	V
reset hysteresis at pin VDD [1] E520.34 (3.3V device)	$V_{DD,RSTD3.3}$ - $V_{DD,RSTA3.3}$	$V_{DD,HYST3.3}$	100	-	400	mV
reset hysteresis at pin VDD [1] E520.35 (5.0V device)	$V_{DD,RSTD5.0}$ - $V_{DD,RSTA5.0}$	$V_{DD,HYST5.0}$	100	-	400	mV
RES_N activation time		t_{RES_N}	2	3	5	ms
under-voltage debounce time		$t_{RES\_N,\ RSTA}$	60	-	90	µs
Monitor Parameters						
thermal shutdown flag threshold		T_{SHDN}	150	-	180	°C
thermal shutdown flag hysteresis [1]		T_{HYST}	5	-	22	K
voltage regulator shut down debounce time		$t_{DD,SHDN}$	-	50	-	µs
Local Wake Up						
leakage current	V_{WAKE_N}=V_S=18V	$I_{WAKE\_N,LEAK}$	-5	-	5	µA
input low level		$V_{WAKE\_N,INL}$	2.5	3.0	3.5	V
input high level		$V_{WAKE\_N,INH}$	3.0	3.5	4.0	V
input hysteresis [1]		$V_{WAKE\_N,HYST}$	0.2	0.5	0.8	V
pull up current	V_S < 28 V, V_{WAKE_N} = 0 V	$I_{WAKE\_N,PU}$	-30	-10	-	µA
input debouncing filter time		$t_{WAKE\_N,DB}$	-	-	25	µs

[1] not production tested

Electrical Characteristics (continued)

(V_S = +5V to +28V, Tamb = -40°C to +125°C, unless otherwise noted.
Typical values are at V_S = +12.0V and Tamb = +25°C. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Voltage Regulator						
output voltage range E520.35 (5.0V device)	active mode VS > 7V, I_{VDD} > -60mA	$V_{DD,ACT5.0}$	4.9	5.0	5.1	V
output voltage range E520.34 (3.3V device)	active mode I_{VDD} > -60mA	$V_{DD,ACT3.3}$	3.23	3.3	3.37	V
output current range	VDD accuracy 2%	$I_{DD,ACT}$	-60	-	-	mA
output current range	VDD accuracy 5%	$I_{DD,ACT}$	-100	-	-	mA
output current limitation		$I_{DD,LIM}$	-230	-	-130	mA
voltage drop between pin VS and pin VDD E520.35 (5.0V device)	3.8V < V_S < ($V_{DD,ACTXX}$+ 300mV), -60mA < I_{DD}	$V_{DD,LD60m}$	-	-	300	mV
voltage drop between pin VS and pin VDD E520.35 (5.0V device)	3.8V < V_S < ($V_{DD,ACTXX}$+50mV), -5mA < I_{DD}	$V_{DD,LD5m}$	-	-	50	mV
power supply ripple rejection ratio [1]	10 Hz to 100 Hz 10 µF capacitor at pin VDD, V_S = 14V, I_{VDD} = -15 mA	PSRR	50	-	-	dB
output voltage range [1] E520.35 (5.0V device)	standby mode	$V_{DD,STBY5.0}$	4.75	5.0	5.25	V
output voltage range [1] E520.34 (3.3V device)	standby mode	$V_{DD,STBY3.3}$	3.135	3.3	3.465	V
output current range	standby mode	$I_{DD,STBY}$	-60	-	-	mA
LIN Transceiver						
functional range LIN transceiver		$V_{LIN,VS}$	7	-	18	V
recessive output voltage	TXD=high	$V_{LIN,REC}$	V_S -1V	-	V_S	V
dominant output voltage	TXD=low, V_S=7.0V, R_{LIN}=0.5kΩ to V_S	$V_{LIN,DOM}$	-	-	1.2	V
dominant output voltage	TXD=low, V_S=18V, R_{LIN}=0.5kΩ to V_S	$V_{LIN,DOM1}$	-	-	2.0	V
receiver dominant level		$V_{LIN,THDOM}$	-	-	0.4*V_S	V
receiver recessive level		$V_{LIN,THREC}$	0.6*V_S	-	-	V
LIN bus center voltage	$V_{LIN,BUSCNT}$= ($V_{LIN,THDOM}$+ $V_{LIN,THREC}$)/2	$V_{LIN,BUSCNT}$	0.475*V_S	-	0.525*V_S	V
receiver hysteresis	$V_{LIN,THREC}$- $V_{LIN,THDOM}$	$V_{LIN,HYS}$	-	-	0.175*V_S	V

[1] not production tested

Electrical Characteristics (continued)

(V_S = +5V to +28V, Tamb = -40°C to +125°C, unless otherwise noted.
Typical values are at V_S = +12.0V and Tamb = +25°C. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
output current limitation	$V_{LIN} = V_{VS,MAX}$ = 18 V	$I_{LIN,LIM}$	40	-	200	mA
pull up resistance		$R_{LIN,SLAVE}$	20	33	60	kΩ
leakage current flowing into pin LIN	transmitter passive, 7V<V_S<18V, 7V<V_{LIN}<18V, V_{LIN}>V_S	$I_{LIN,BUSREC}$	-	8	20	µA
pull up current flowing out of pin LIN	transmitter passive, 7V<V_S<18V, V_{LIN}=0V	$I_{LIN,BUSDOM}$	-1	-	-	mA
leakage current, loss of ground (GND device = VS)	V_S=13.5V, 0V<V_{LIN}<18V	$I_{LIN,NOGND}$	-1		0.1	mA
LIN leakage current, unsupplied node	V_S=0V, 0V<V_{LIN}<18V	I_{LIN}	-	8	20	µA
LIN leakage current [1], unsupplied node, T = 85 °C	V_S=0V, 0V<V_{LIN}<18V	$I_{LIN,85}$	-	-	15	µA
clamping voltage [1]	V_S=0V, I_{LIN}=1mA	$V_{LIN,CLAMP}$	40		-	V
input capacitance [1]	7V < V_S < 18V	$C_{LIN,PIN}$	-	-	30	pF
output slew rate	C_{LIN}=1-10nF, R_{LIN}=0.5-1kΩ, 1µs<τ_{LIN}<5µs, V_S=18V	$SR_{LIN,OUT}$	1	-	3	V/µs
output slew rate	C_{LIN}=1-10nF, R_{LIN}=0.5-1kΩ, 1µs<τ_{LIN}<5µs, V_S=7.0V	$SR_{LIN,OUT1}$	0.5	-	3	V/µs
symmetry of rising and falling edge	V_S=18V	$t_{LIN,SYM}$	-5	-	5	µs
receive propagation delay		$t_{RXD,PDR}$	-	-	6	µs
receive propagation delay symmetry		$t_{RXD,SYM}$	-2	-	2	µs
LIN bus receiver debounce time		$t_{LIN,DB}$	0.3	-	6	µs
wake-up debounce time		$t_{LIN,WU}$	70	-	150	µs

[1] not production tested

Electrical Characteristics (continued)

(V_S = +5V to +28V, Tamb = -40°C to +125°C, unless otherwise noted.
Typical values are at V_S = +12.0V and Tamb = +25°C. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Duty cycle 1 [1)]	$V_{LIN,THREC}$(max) =0.744*V_S, $V_{LIN,THDOM}$(max) =0.581*V_S, V_S=7-18V, t_{BIT}=50us, $D_{LIN,1}$=t_{BUSREC}(min)/(2*t_{BIT})	$D_{LIN,1}$	0.396	-	-	-
Duty cycle 2 [1)]	$V_{LIN,THREC}$(min) =0.422*V_S, $V_{LIN,THDOM}$(min) =0.284*V_S, V_S=7-18V, t_{BIT}=50us, $D_{LIN,2}$=t_{BUSREC}(max)/(2*t_{BIT})	$D_{LIN,2}$	-	-	0.581	-
Duty cycle 3 [1)]	$V_{,LIN,THREC}$(max) =0.778*V_S, $V_{LIN,THDOM}$(max) =0.616*V_S, V_S=7-18V, t_{BIT}=96us, $D_{LIN,3}$=t_{BUSREC}(min)/(2*t_{BIT})	$D_{LIN,3}$	0.417	-	-	-
Duty cycle 4 [1)]	$V_{LIN,THREC}$(min) =0.389*V_S, $V_{LIN,THDOM}$(min) =0.251*V_S, V_S=7-18V, t_{BIT}=96us, $D_{LIN,4}$=t_{BUSREC}(max)/(2*t_{BIT})	$D_{LIN,4}$	-	-	0.590	-
receive data baud rate	flash mode, V_S=13V	$B_{LIN,RXD}$	-	-	250	kBaud
transmit data baud rate	flash mode, V_S=13V	$B_{LIN,TXD}$	-	-	115	kBaud

[1)] Bus load conditions (C_{LIN},R_{LIN}): 1nF, 1kΩ/6.8nF, 660Ω/10nF, 500Ω

Electrical Characteristics (continued)

(V_S = +5V to +28V, Tamb = -40°C to +125°C, unless otherwise noted.
Typical values are at V_S = +12.0V and Tamb = +25°C. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
EN						
input low level range		$V_{EN,INL}$	-	-	$0.25*V_{DD}$	V
input high level range		$V_{EN,INH}$	$0.75*V_{DD}$	-	-	V
pull down resistor	V_{EN}=5.0V	$R_{EN,PD}$	80	150	220	kΩ
input leakage	V_{EN}=0V	$I_{EN,LEAK}$	-5	-	5	µA
TXD						
input low voltage range		$V_{TXD,INL}$	-	-	$0.25*V_{DD}$	V
input high voltage range		$V_{TXD,INH}$	$0.75*V_{DD}$	-	-	V
output low level range	I_{TXD}=1mA	$V_{TXD,OUT}$	-0.3	-	0.6	V
TXD pull up resistor	V_{TXD}=0V	$R_{TXD,PU}$	80	150	220	kΩ
TXD dominant detection	TXD = low, active mode	$t_{TXD,TO}$	6	10	14	ms
RXD						
output low level range	I_{RXD}=1mA	$V_{RXD,OUT}$	-0.3	-	0.6	V
pull up resistance (E520.35 5V device)	V_{RXD}=0V	$V_{RXD,PU}$	3	4	6	kΩ
pull up resistance (E520.34 3.3V device)	V_{RXD}=0V	$V_{RXD,PU}$	3	5	10	kΩ
Reset						
output low level range	I_{RES_N}=1mA	$V_{RES\_N,OUT}$	-0.3	-	0.6	V
pull up resistance (E520.35 5V device)	V_{RES_N}=0V	$R_{RES\_N,PU}$	3	4	6	kΩ
pull up resistance (E520.34 3.3V device)	V_{RES_N}=0V	$R_{RES\_N,PU}$	3	5	10	kΩ
Watchdog						
input low level range at pins WDIN, WDDM		$V_{WDIN,INL}$	-	-	$0.25 * V_{DD}$	V
input high level at pins WDIN, WDDM		$V_{WDIN,INH}$	$0.75 * V_{DD}$	-	-	V
pull down resistor at pins WDIN, WDDM	V_{WDIN}=5.0V	$R_{WDIN,PD}$ $R_{WDDM,PD}$	80	150	220	kΩ
reference current	V_{WDOSC}=1V	$I_{WDOSC,REF}$	-	14	-	µA
External reference resistor		$R_{WD,OSC}$	10		100	kΩ
watchdog cycle time for MIN/MAX limits see chapter 6.5 Watchdog	R_{WDOSC}=10kΩ	$T_{WD,CYC10k}$		10.2		ms
watchdog cycle time for MIN/MAX limits see chapter 6.5 Watchdog	R_{WDOSC}=100kΩ	$T_{WD,CYC100k}$		100.2		ms

Electrical Characteristics (continued)

(V_S = +5V to +28V, Tamb = -40°C to +125°C, unless otherwise noted.
Typical values are at V_S = +12.0V and Tamb = +25°C. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
first trigger open window	open window after RES_N is released	$t_{WD,FIRST}$	91	110	135	ms
open window time		$d_{WD,OW}$	-	0.5 * *$T_{WD,CYC}$	-	ms
closed window time		$t_{WD,CW}$	-	0.5 * $T_{WD,CYC}$	-	ms
watchdog reset time		$t_{WD,RES}$	414	512	645	µs
watchdog trigger pulse width		$t_{WD,CMD}$	8	-	-	µs
VBAT Voltage divider						
Voltage divider [1] E520.34 (3.3V device)	$V_{S,PD} < V_{BAT} < 18V$	$DR_{PV,3.3V}$	5.86	5.95	6.04	-
Voltage divider [1] E520.35 (5V device)	$5V < V_{BAT} < 28V$	$DR_{PV,5V}$	5.86	5.95	6.04	-
V_{BAT} input current	V_{BAT} = 13.8 V	I_{VBAT}	-	150	-	µA
reverse current	V_{BAT} = -24 V	I_{VBAT_REV}	-1		-	mA
Maximum output Voltage at PV E520.34 (3.3V device)	$18 V < V_{BAT} < 40 V$	$V_{PV,MAX,3.3V}$	-	$1*V_{DD}$	-	V
Maximum output Voltage at PV E520.35 (5V device)	$28 V < V_{BAT} < 40 V$	$V_{PV,MAX,5V}$	-	$1*V_{DD}$	-	V
input low level range		$V_{DIV\_ON,INL}$	-	-	$0.25*V_{DD}$	V
input high level range		$V_{DIV\_ON,INH}$	$0.75*V_{DD}$	-	-	V
input pull down resistance	V_{DIV_ON} = 5 V	$R_{DIV\_ON,PD}$	80	150	220	kΩ

[1] not production tested, at higher V_{BAT} input voltage the output voltage at pin PV is limited to V_{DD} level.

6 Functional Description

The E520.34 /.35 is the interface between the physical bus in a Local Interconnect Network (LIN) and the LIN master / slave protocol controller according to LIN V2.1 / V2.2 specification. The device provides local and remote wake-up capability in sleep and standby mode. A wake-up source flag can be evaluated by the microcontroller. The integrated TXD dominant clamp timeout prevents the LIN network from permanent distortion in case of hardware failure. The flash mode provides higher data rates on the LIN pin for end-of-line or in-car flashing up to 115 kBaud.

The integrated voltage regulator supplies the microcontroller and peripheral blocks with current up to 60mA (2% accuracy). A higher current up to 100mA can be supplied with lower accuracy. For applications with a permanent supplied microcontroller a standby mode with active voltage regulator and low quiescent current consumption is implemented.

The cycle time of the integrated window watchdog can be configured by external resistor. For software development purpose the watchdog can be disabled.

The integrated reverse polarity protected 6:1 voltage divider can be connected to the battery supply to measure the supply voltage with fast response time. To limit the output voltage in case of VBAT over-voltage a clamping to the microcontroller supply voltage is integrated.

6.1 Operating Modes

The E520.34 /.35 provides the following operation modes:

6.1.1 Power-off mode

The device enters Power-off mode in case the battery voltage is lower than $V_{S,PD}$ voltage level. In Power-off mode the voltage regulator is switched off. If the battery voltage rises above the power on reset threshold level $V_{S,POR}$ the device resets the system via activating pin RES_N. The device enters mode Power-On.

6.1.2 Power-on mode

When the voltage at pin VS exceeds the Power-on-reset threshold voltage $V_{S,POR}$, the device enters power-on mode. In that mode the voltage regulator is switched on. After pin VDD exceeds $V_{DD,RSTD}$, RES_N is held low for t_{RES_N}.
Setting pin EN to active HIGH level for a time period of at least t_{2AM} the device enters active mode.
Any wake-up request from mode SLEEP is indicated by setting the pin RXD to LOW level.
The wake-up source can be recognized by the microcontroller by reading the level at pin TXD. A weak pull up indicates a remote wake-up request and strong pull down indicates a local wake-up request.
Note: The voltage regulator over temperature shut down results in a transition to Power-on mode and the regulator is switched off. The voltage regulator will be switched on if the junction temperature cools down by T_{HYST}.

6.1.3 Active mode

In Active mode the device is able to transmit and receive data via the LIN bus line. The receiver transfers the detected LIN bus data via pin RXD to the microcontroller: HIGH at a recessive level and LOW at a dominant level on the bus. The receiver has a debounced VS supply related threshold with hysteresis. The transmit data at the TXD input is converted by the transmitter into a LIN bus signal. The LIN bus slew rate is optimized to minimize electromagnetic emission. The LIN bus output pin is pulled HIGH via an internal slave termination resistor. For a master application an external termination network is needed.
The device enters active mode from:

- standby mode whenever a HIGH level on pin EN is maintained for a time of at least t_{2AM}
- flash mode after a time out of t_{FMTO}
- power ON mode in case of a HIGH-level on pin EN, maintained for a time of at least t_{2AM}.

6.1.4 Standby mode

In standby mode the voltage regulator is activated. Also the slave termination resistor at pin LIN is enabled. The watch dog is running.
Any wake-up request is indicated by setting the pin RXD to LOW level.
The wake-up source can be recognized by the microcontroller by reading the level at pin TXD. A weak pull up indicates a remote wake-up request and strong pull down indicates a local wake-up request.

6.1.5 Sleep mode

The sleep mode is a very low power mode of the device. After entering standby mode a TXD LOW level for at least t_{2SLEEP} changes to sleep mode. The transition to sleep mode can be performed independently from the actual level on pin LIN or pin WAKE_N. In Sleep mode the voltage regulator is deactivated and becomes high omic after a delayed time of $t_{DD,OFFDEL}$.
The transition into mode sleep is prohibited if a wake-up request is pending. The request must be cleared via a transition to mode Active. In sleep mode the internal slave resistor termination at LIN bus pin is switched off. A power-saving weak pull-up between pins LIN and VS is still present. The device can be woken up remotely via pin LIN or locally via pin WAKE_N. Debounce filters prevent unwanted wake-up events due to EMI at the inputs of the wake-up sources.

6.1.6 Flash mode

The flash mode allows a higher transmit baud rate up to 115 kBd and the receive baud rate up to 250 kBd. For further information see chapter „LIN flash mode“.

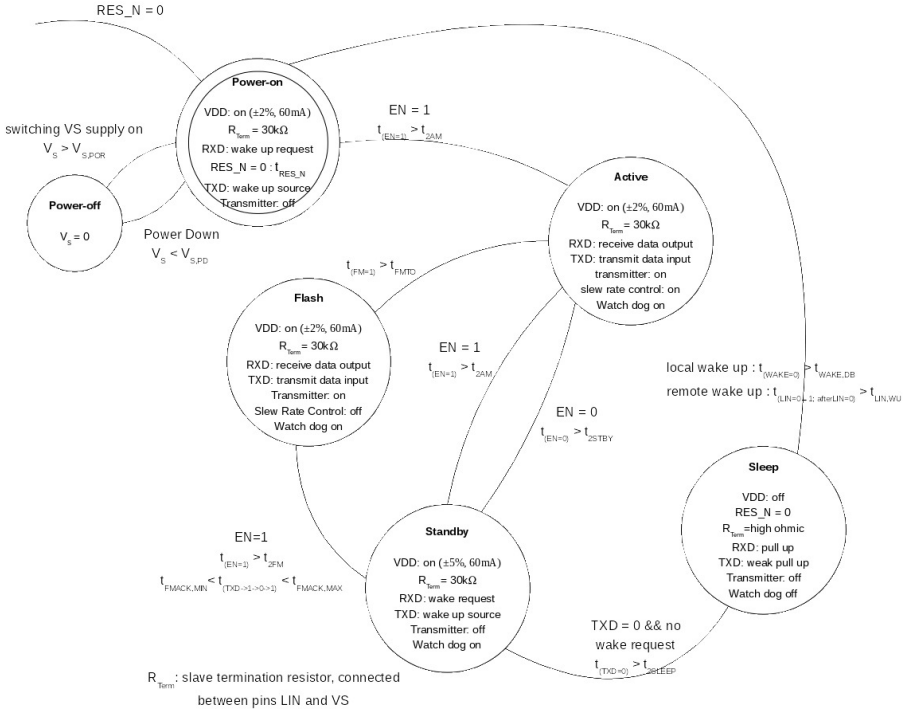


Fig. 1: SBC State Diagram

Mode	***EN***	***VDD***	***RXD***	***TXD***	***LIN***	***Watch Dog***
Power-off	high ohmic	off	high ohmic	high ohmic	high ohmic	off
Power-on	low	on	strong pull down output for wake-up request	weak pull up output if remote wake-up; strong pull down output if local wake-up	off	on after RES_N is high
Active	high	on	pull up for LIN recessive; strong pull down output for LIN dominant	high level input for LIN recessive; low level input for LIN dominant	on; slew rate control activated	on
Standby	low	on	strong pull down output for wake-up request	weak pull up output if remote wake-up; strong pull down output if local wake-up	transmitter off termination on	on
Sleep	low	off	pull up	pull down	off	off
Flash	high	on	pull up for LIN recessive; strong pull down output for LIN dominant	high level input for LIN recessive; low level input for LIN dominant	on; slew rate control deactivated	on

Table 1: Pin Functionality

6.2 Voltage Regulator

The on chip low drop voltage regulator provides the voltage V_{DD} (typ. 3.3V or 5.0V depending on version E520.34 or E520.35) at pin VDD. It supplies the peripheral circuitry of the SBC and the host MCU chip with typical 60mA (2%) or up to 100mA with lower accuracy.

The voltage regulator is activated in all operating modes except in sleep mode. In sleep mode the voltage regulator is switched off.

The voltage regulator output current is limited to $I_{DD,LIM}$. The current limitation is always activated.

6.3 LIN Transceiver

6.3.1 LIN physical layer

The LIN BUS Interface is conform to LIN Physical Layer Specification Revision V2.1 / V2.2 and can be used for master or slave applications. The device has an internal slave termination implemented. Master termination has to be applied externally.

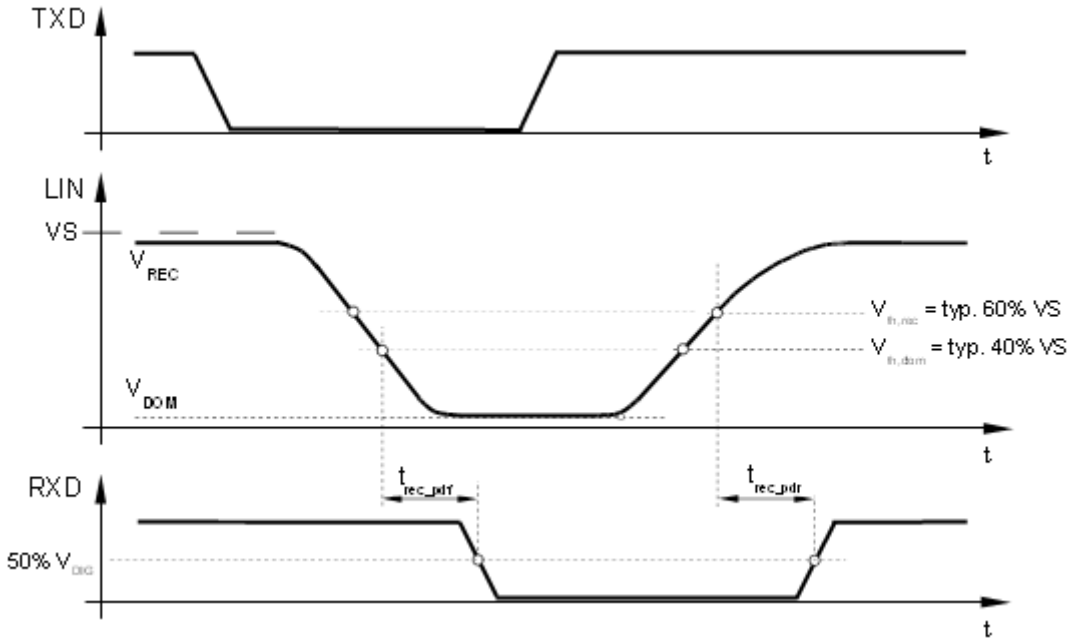


Fig. 2: LIN transceiver physical layer timing

6.3.2 LIN flash mode

In flash mode LIN bus slew rate control is disabled to support high baud rate for microcontroller flashing purposes via LIN bus. Flash mode is entered from standby mode by a rising edge on pin EN followed by a LOW pulse at pin TXD for t_{FMACK} within the time period t_{2AM}. The flash mode must be re-triggered within the time out t_{FMTO} otherwise the mode is left to active mode.

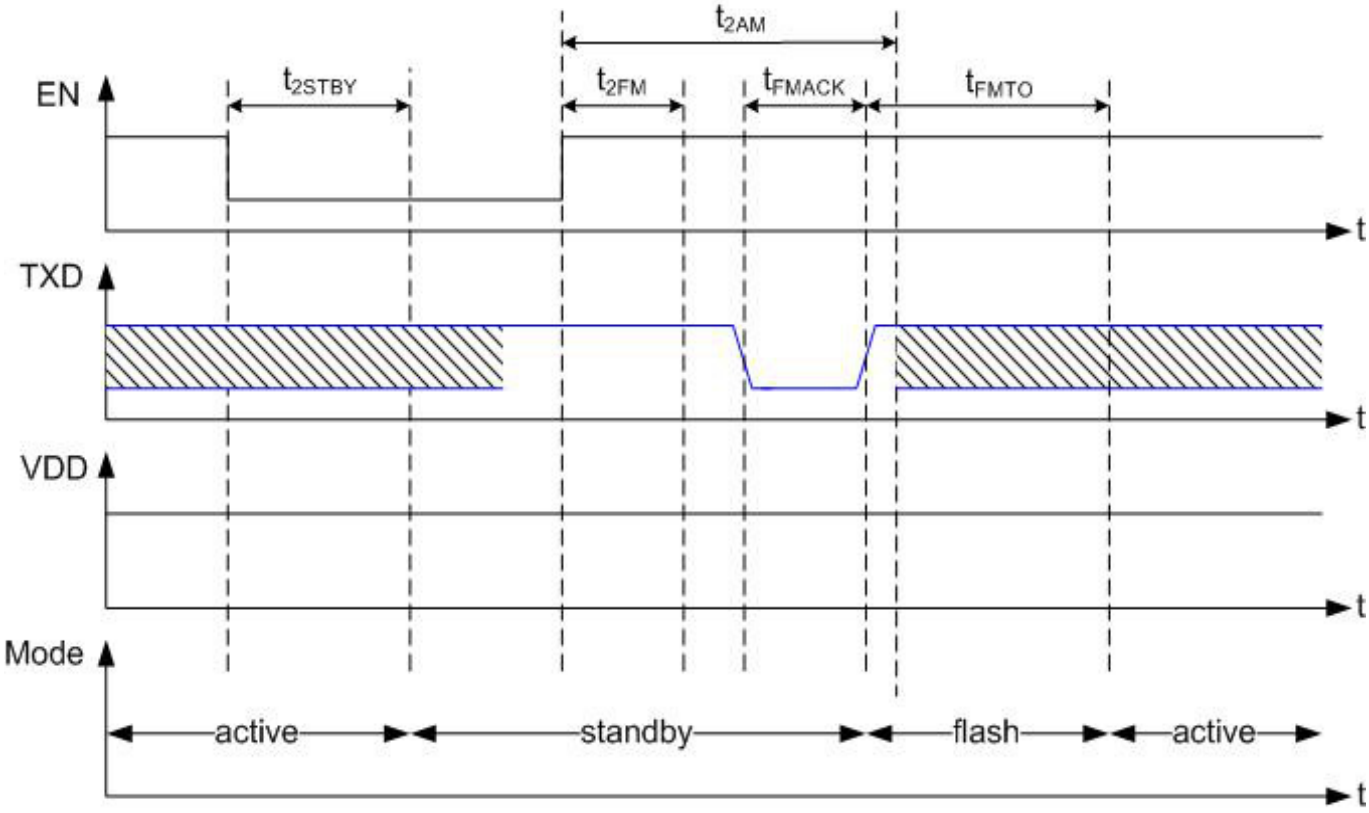


Fig. 3: Flash mode transition timing with TXD acknowledge pulse.

6.3.3 LIN TXD dominant time out

In order to prevent the LIN bus from being permanent dominant in case of permanent LOW level at pin TXD a time-out is implemented. The LIN transmitter is disabled after $t_{TXD,TO}$. The timer is triggered by a negative edge on pin TXD and reset by a positive edge on pin TXD.

6.4 Wake-Up

In case the device is in sleep or standby mode there are 2 events to wake-up the device:

1. Local wake-up with low level at pin WAKE_N.
2. Remote wake-up by LIN

Any of these wake-up events changes the device mode from sleep mode to power-on mode.
If a remote or local wake-up occurs in standby mode the device remains in this mode and a wake-up event is signalized at pin RXD. A transition to sleep mode is prohibited.

6.4.1 Local wake-up

The device can be woken up from sleep mode via pin WAKE_N. Pulling pin WAKE_N below $V_{WAKE\_N,INL}$ level results in a local wake-up request. The wake-up event is falling edge triggered. This allows the device to enter sleep mode with pin WAKE_N pulled to low.

The pin WAKE_N is an high voltage input with pull up current source $I_{WAKE\_N,PU}$ and an input debounce filter. If the local wake-up is not used in application, the pin WAKE_N has to be connected to pin VS.

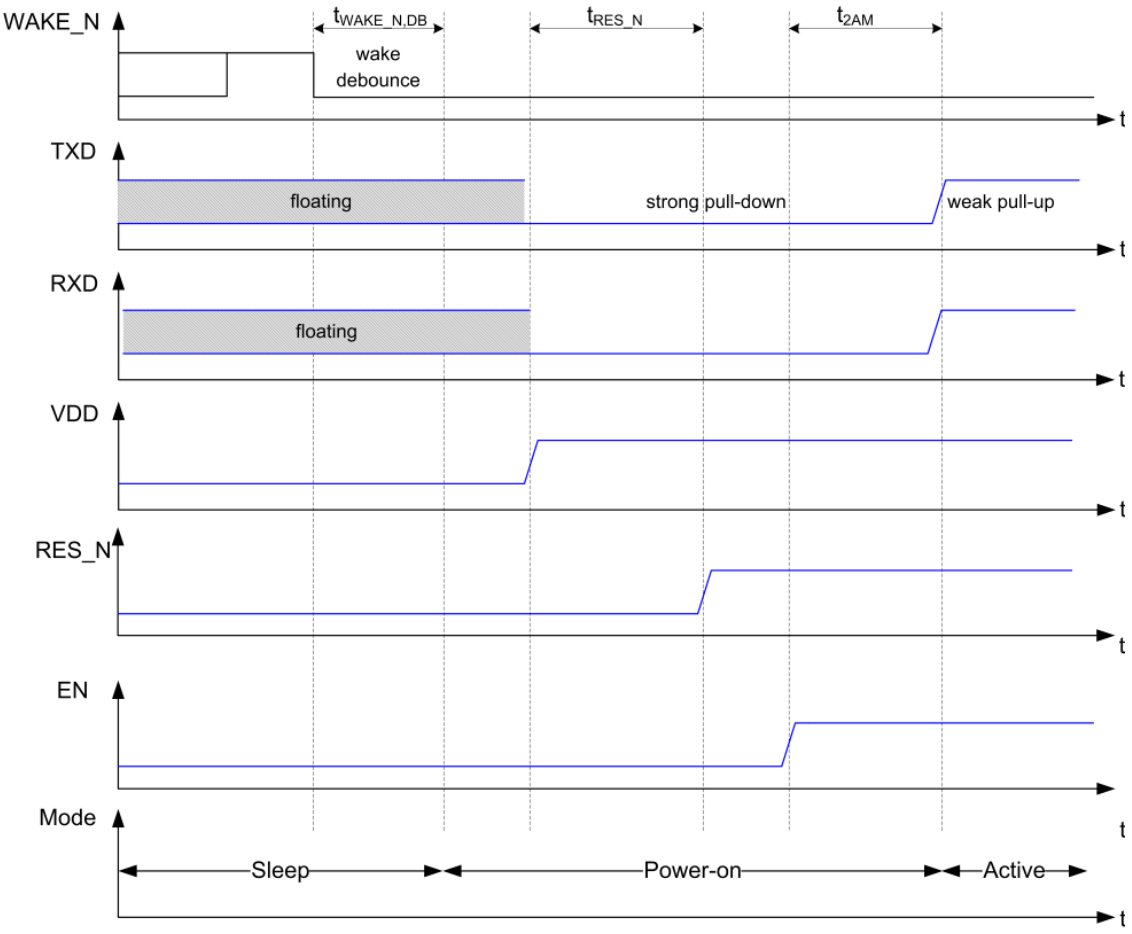


Fig. 4: Local wake-up in mode Sleep

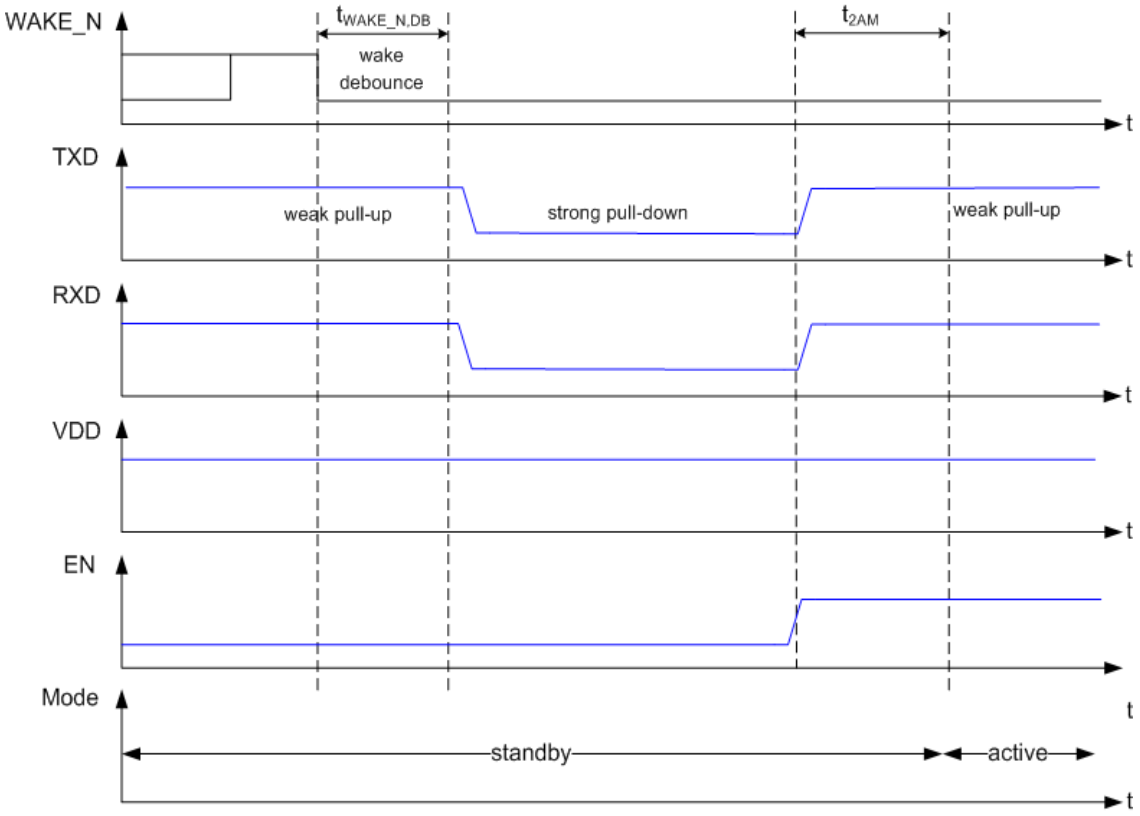


Fig. 5: Local wake-up in mode Standby and Flash

6.4.2 Remote wake-up

The device can be woken up remotely from sleep and standby mode via pin LIN.

A falling edge at the LIN pin followed by a dominant bus level $V_{LIN,DOM}$ maintained for a time period $t_{LIN,WU}$ with a following rising edge results in a remote wake-up. The wake-up request is signalized to microcontroller by a low state at pin RXD.

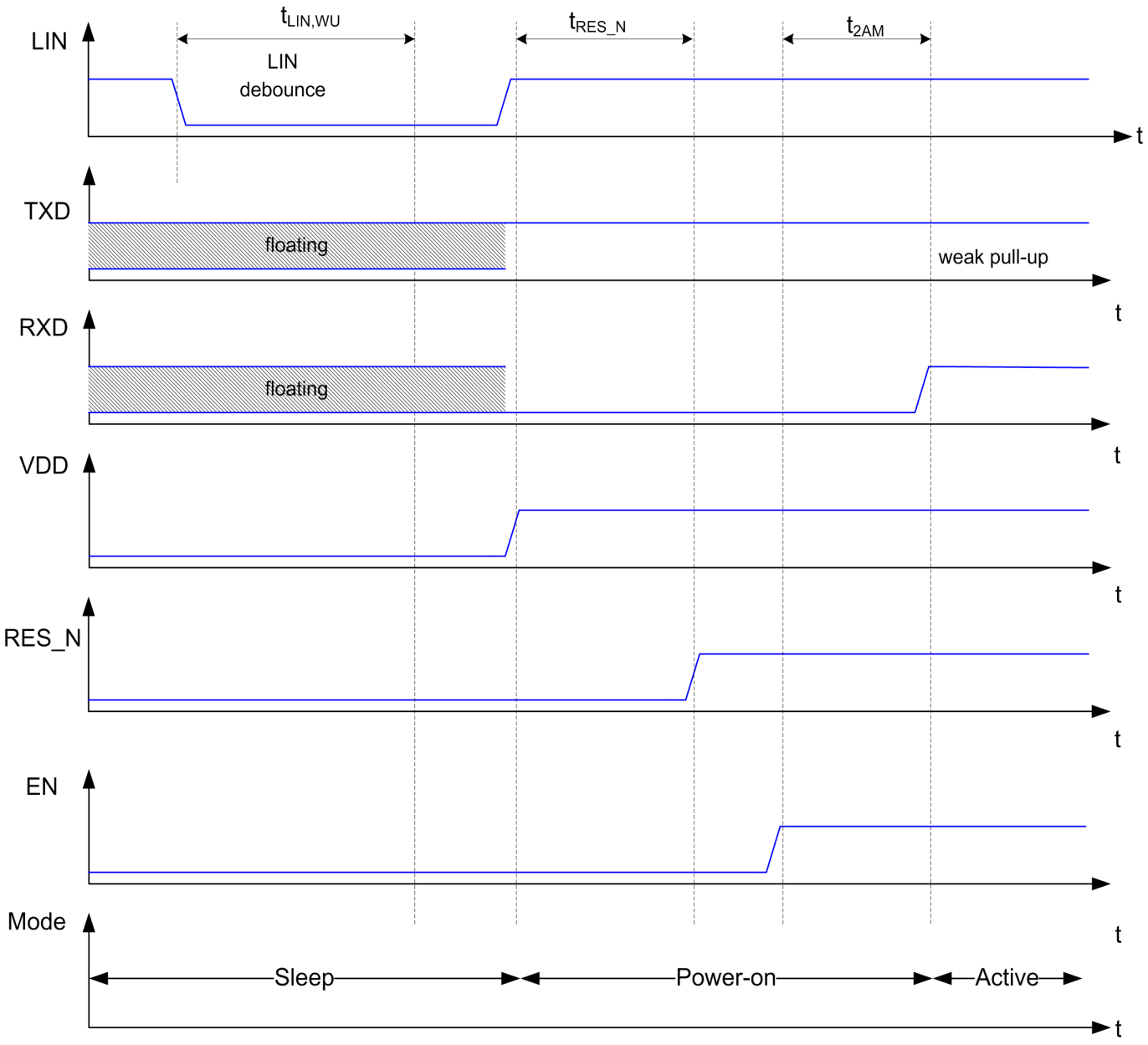


Fig. 6: Remote wake-up in mode Sleep

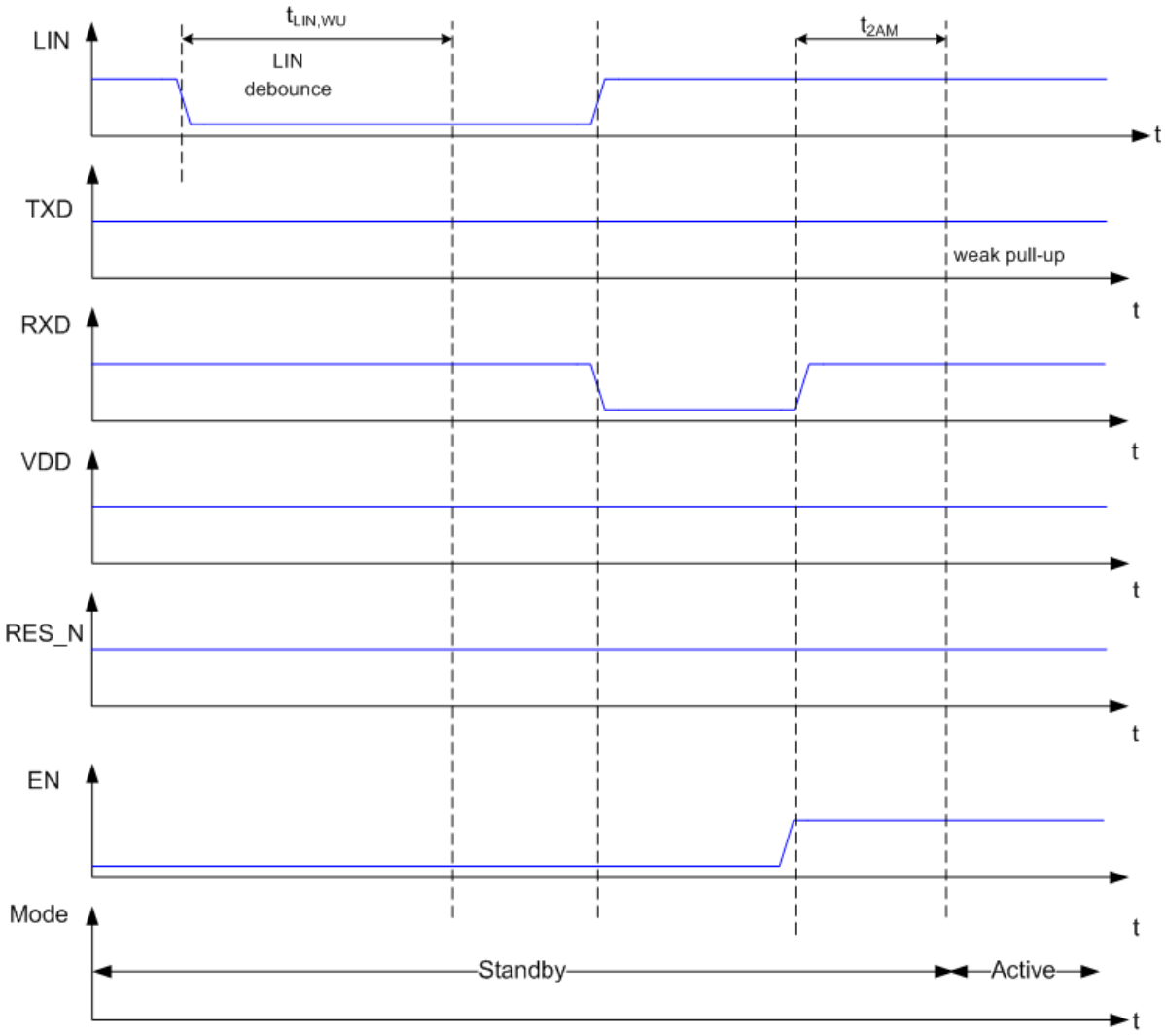


Fig. 7: Remote wake-up in mode Standby

6.4.3 Wake-up source signalization

The device latches the information of the wake-up source to distinguish between a remote wake-up request via LIN bus and local wake-up via pin WAKE_N. The wake-up source can be read on pin TXD in the mode Standby and Power-on.
A HIGH level at pin TXD indicates a remote wake-up request (weak pull-up at pin TXD) and a LOW level indicates a local wake-up request (strong pull-down at pin TXD).

6.4.4 Wake-up flag reset

The wake-up request flag and the wake-up source flag are reset after entering active mode. The wake-up source signal at TXD and RXD is interrupted while pin EN is set to high in order to check flash mode request at TXD.

6.5 Watchdog

The watchdog has to be triggered by high pulses at WDIN in the open window time $t_{WD,OW}$. A correct WD-trigger pulse in the open window starts the next closed window. Any WD-trigger pulse in the closed window resets the watchdog and a reset will be activated on pin RES_N for $t_{WD,RES}$.

There is an enlarged first open window after a high transition at RES_N. The first WDIN trigger pulse is allowed to appear latest at $t_{WD,FOW}$.

The watchdog starts with first open window after reentering active- or power-on mode.

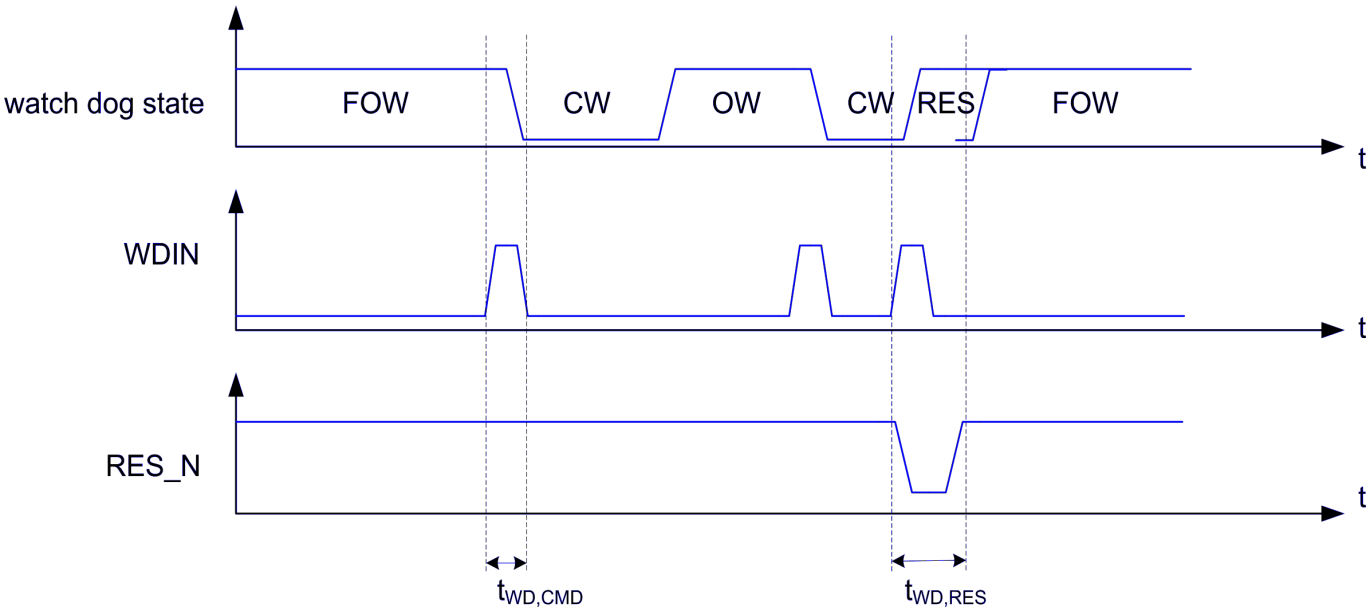


Fig. 8: Watchdowg triggger in closed window (CW)

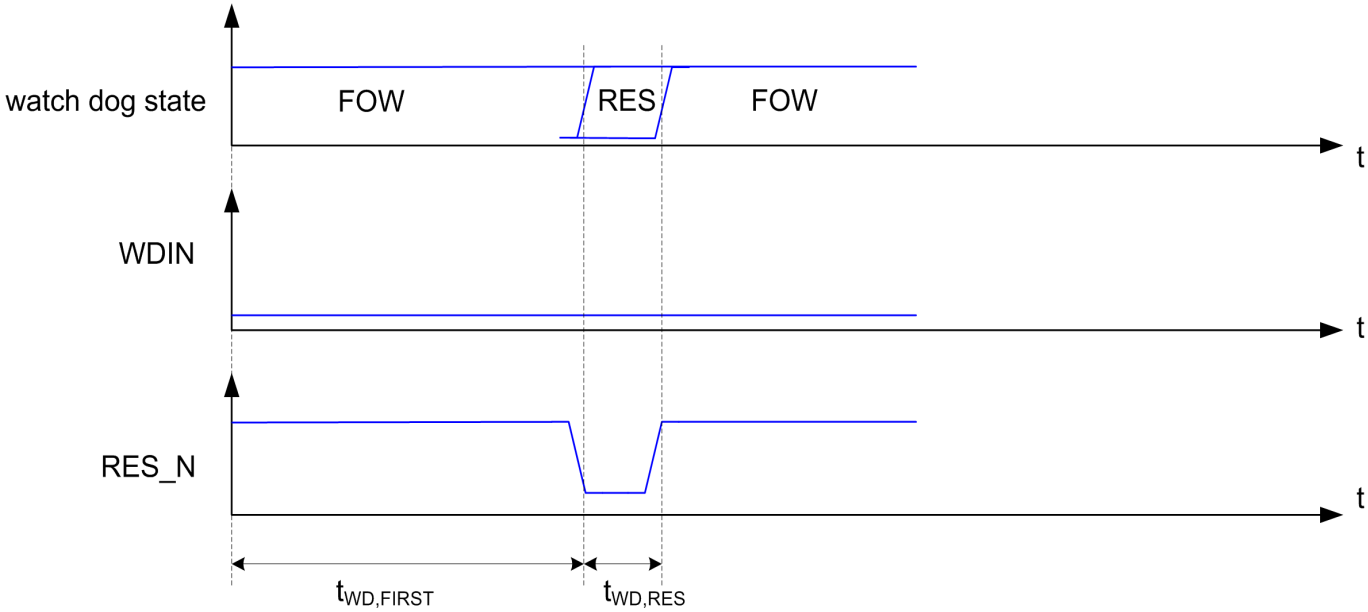


Fig. 9: No watchdog trigger in first open window (FOW)

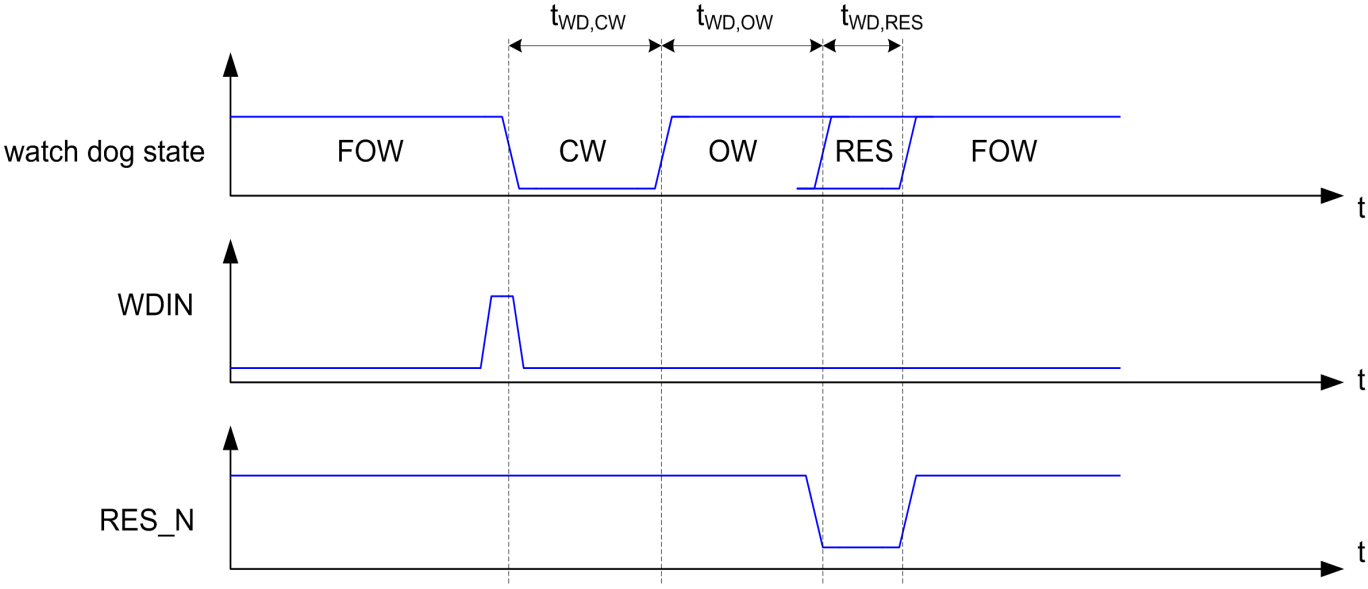


Fig. 10: No watchdog trigger in open window (OW)

6.5.1 Watchdog cycle time configuration

The watchdog cycle time can be configured via the external resistor at pin WDOSC. The watchdog cycle period $T_{WD,CYC}$ is defined by the external resistance $R_{WD,OSC}$ by:

$T_{WD,CYC,MIN} = 0.9 * (R_{WD,OSC} - 2k\Omega)* ms/k\Omega$
$T_{WD,CYC,MAX} = 1.1 * (R_{WD,OSC} + 2k\Omega)* ms/k\Omega$
$T_{WD,CYC,TYP} = (T_{WD,CYC,MAX}+T_{WD,CYC,MIN}) / 2$

$R_{WD,OSC}$ / kΩ	$T_{WD,CYC,typ}$ in ms
10	10.2
22	22.2
47	47.2
100	100.2

Table 2: Typical watchdog configuration examples

Watchdog safe area calculation:

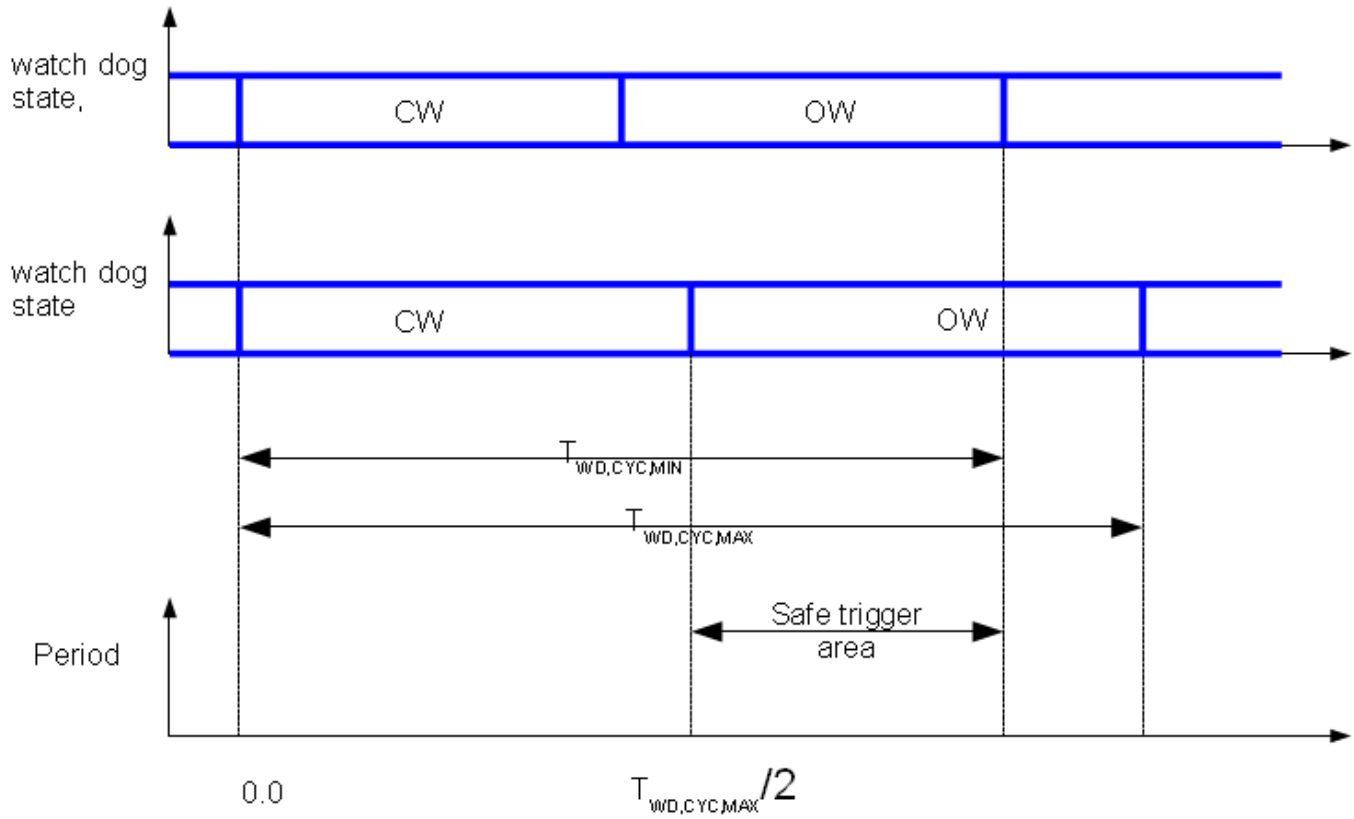


Fig. 11: Watchdog safe trigger area

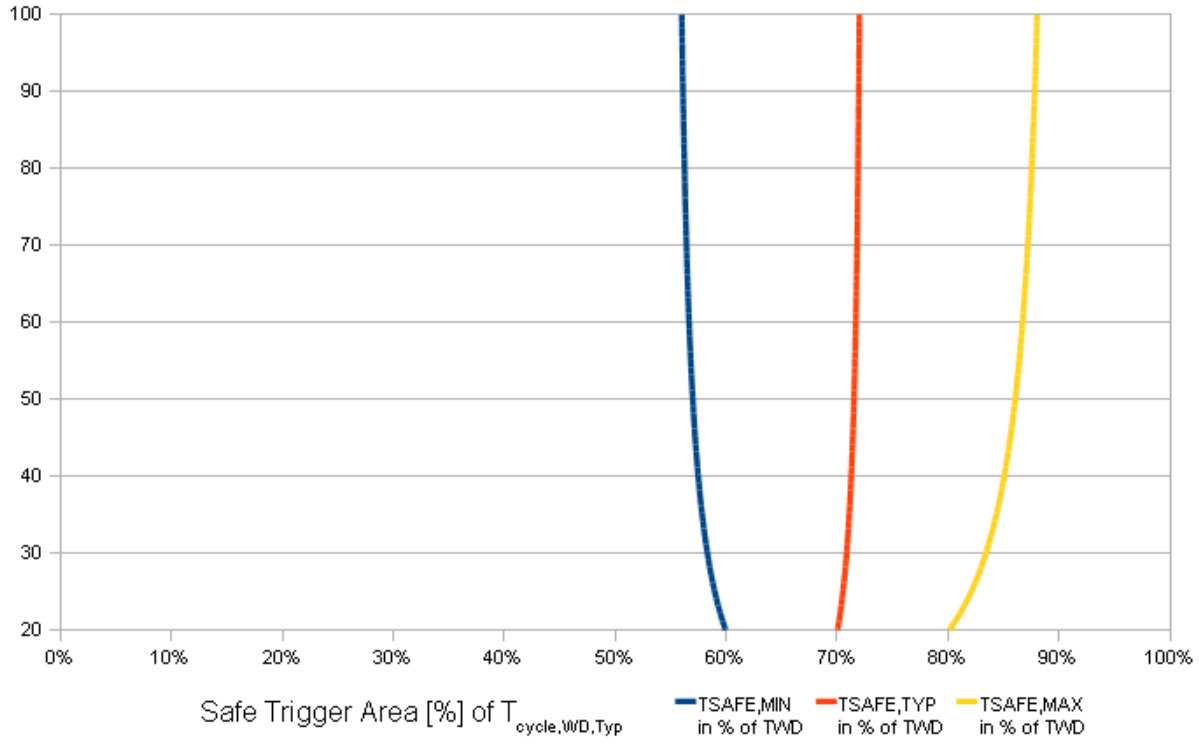


Fig. 12: Watchdog safe area depending on watchdog cycle-time – Range 20ms up to 100ms

6.5.2 Watchdog debug mode

For debugging purposes the watchdog can be stopped by pulling pin WDDM to HIGH. In this case the watchdog timer stops and the actual state remains. After setting pin WDDM to low level the watchdog keeps on running.

6.6 VBAT voltage divider

The integrated reverse polarity protected 6:1 voltage divider can be connected to the battery supply to measure the supply voltage with fast response time. To limit the output voltage in case of VBAT overvoltage a clamping to the microcontroller supply voltage is integrated.

The voltage divider is activated by the digital pin DIV_ON. The divided input voltage is available at pin PV. In Sleep and Standby Mode the DIV_ON functionality is disabled and PV is off. An internal pull-down resistor is implemented.

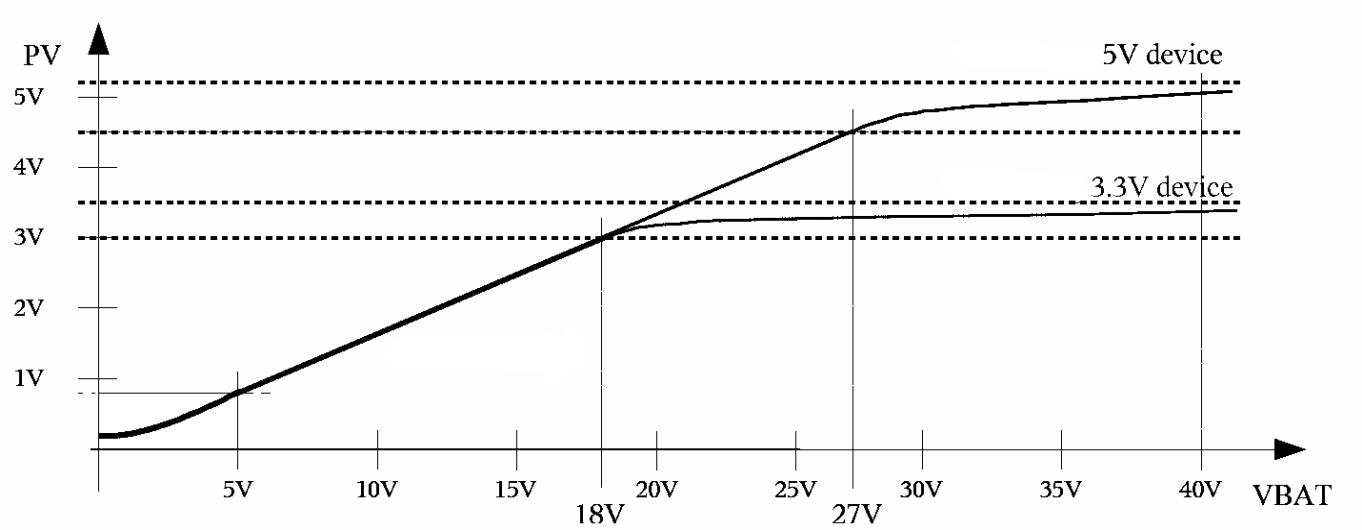


Fig. 13: Typical characteristic of the voltage divider

6.7 Fail Safe Behavior

6.7.1 Reset parameters

The regulator is switched on if the supply input voltage VS exceeds $V_{S,POR}$ threshold and is switched off if the voltage at pin VS falls below $V_{S,PD}$ threshold. The slope of the falling edge after VDD regulator shutdown at pin VDD depends on the external buffer capacitance and the load current. The device enters power-off mode. The device powers up again if the battery voltage exceeds $V_{S,POR}$ level again.

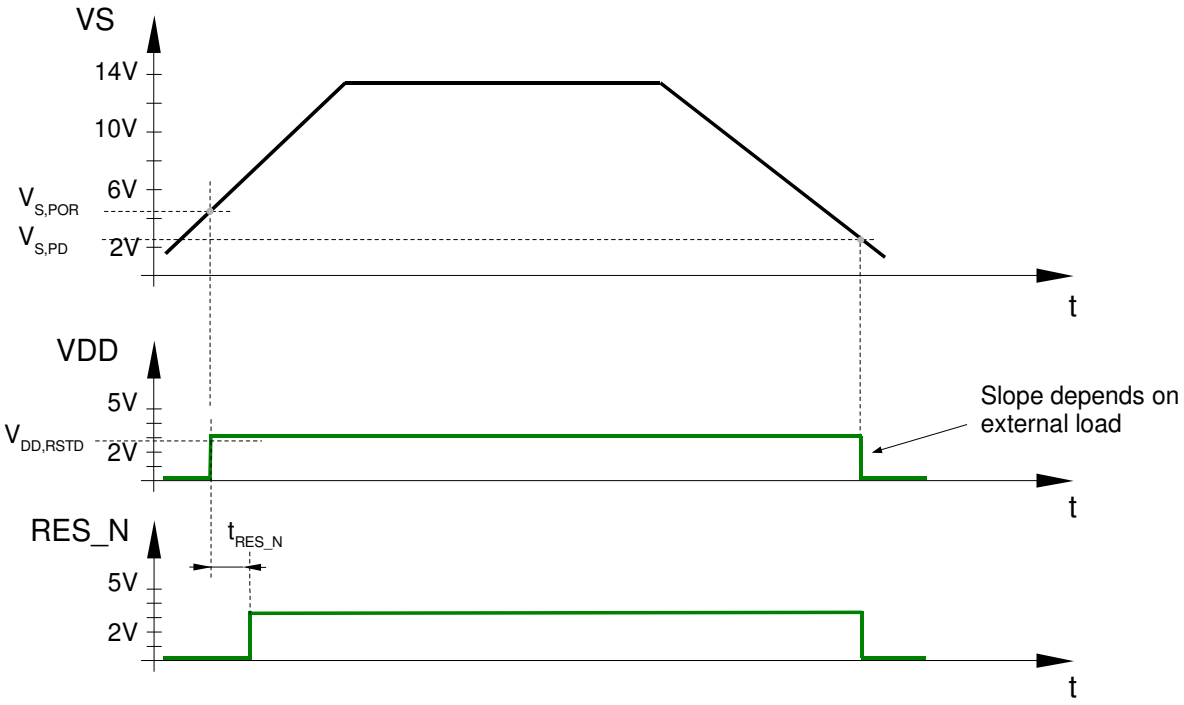


Fig. 14: Power up and power down behavior for 3.3 V device

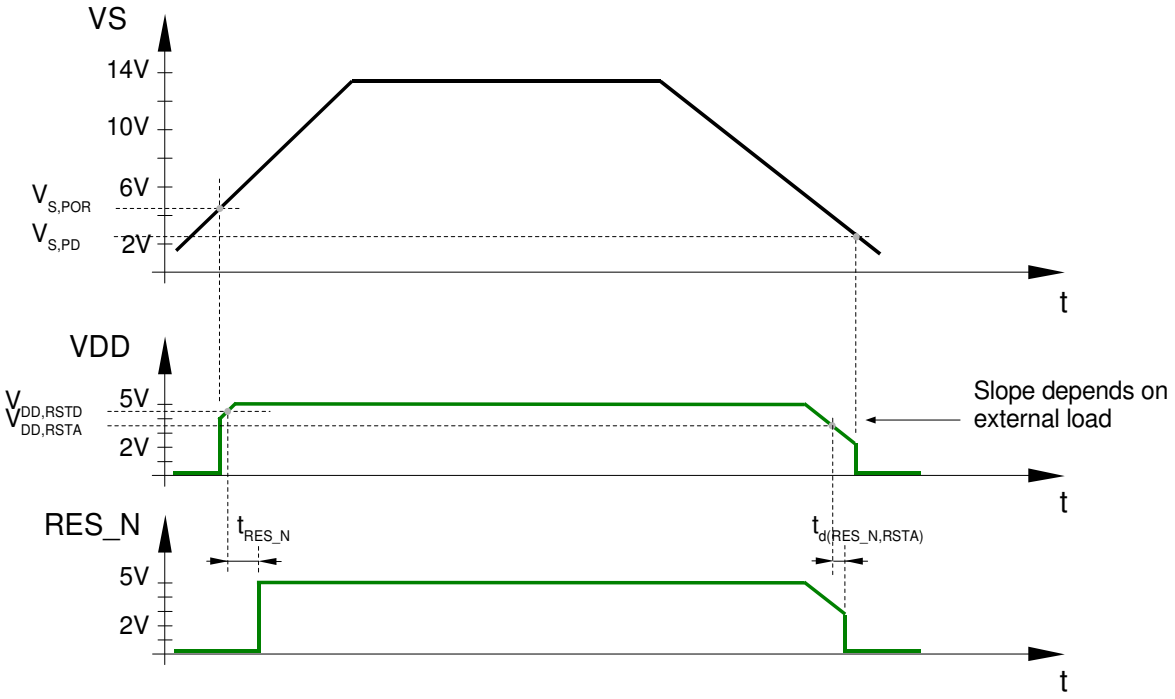


Fig. 15: Power up and power down behavior for 5 V device

6.7.2 Digital input pull-up / pull-down

The digital input pins have internal pull-up or pull-down sources for fail-safe operating conditions according to the following table:

Pin	Termination	Reason
WDDM	weak pull-down	set WD active in case of floating pin WDDM
TXD	weak pull-up	set TXD input to defined level in case of floating pin TXD
EN	weak pull-down	force SBC in Sleep mode in case of floating pin EN
WDIN	weak pull-down	terminates WD trigger input in case of floating pin WDIN; results in activating RES_N

Table 3: Fail-Save Pin-Termination Table.

6.7.3 Thermal shutdown

The LIN-SBC is protected against thermal stress. In case the junction temperature exceeds the shutdown temperature T_{SHDN}, the internal SBC thermal shutdown flag is set. The flag is reset in case the junction temperature cools down by T_{HYST} .

Depending on the cause for the over temperature (voltage regulator or LIN transmitter) the SBC behaves different. In any case it shut down the detected heat source to reduce power dissipation of the SBC.

6.7.4 LIN over current protection

The output current of the LIN transmitter is limited to $I_{LIN,LIM}$ in order to protect the transmitter against short circuit to pin VS .

In case the SBC thermal shutdown flag is caused by the LIN transceiver the transmitter is disabled and the LIN over temperature flag is set.

The over temperature flag is reset and the LIN transmitter is enabled in case the junction temperature cools down by T_{HYST} . The LIN shut down does not result in any state change.

6.7.5 LIN TXD dominant timeout

In case of TXD dominant clamping the LIN transmitter is disabled after a dominant detection timeout. For details see chapter 6.3.3 LIN TXD dominant time out.

6.7.6 Voltage regulator over current protection

In case of shorts at pin VDD the output current of the voltage regulator is limited to $I_{DD,LIM}$. In order to limit power dissipation of the device the voltage regulator is shut down if the thermal shutdown flag is caused by by the voltage regulator. A debounce filter of $t_{DD,SHDN}$ is implemented.

The voltage regulator is switched on again in case the junction temperature cools down by T_{HYST} independently of pin EN. The VDD shut down causes a mode change, if the pin VDD voltage drops below the VDD reset threshold level $V_{DD,RSTAXX}$. In this case the device enters power-on mode.

6.7.7 LIN loss of ground

In case of battery voltage loss (pin VS) and ground loss (pin GND) reverse current from the LIN bus line is limited.

6.7.8 Microcontroller reset

In case the voltage at pin VDD drops below the reset threshold $V_{DD,RSTAXX}$ the SBC reset pin RES_N is activated and pulled down to GND. The reset pin RES_N is released after t_{RES_N} if the VDD voltage exceeds the reset deactivation level $V_{DD,RSTDXX}$.

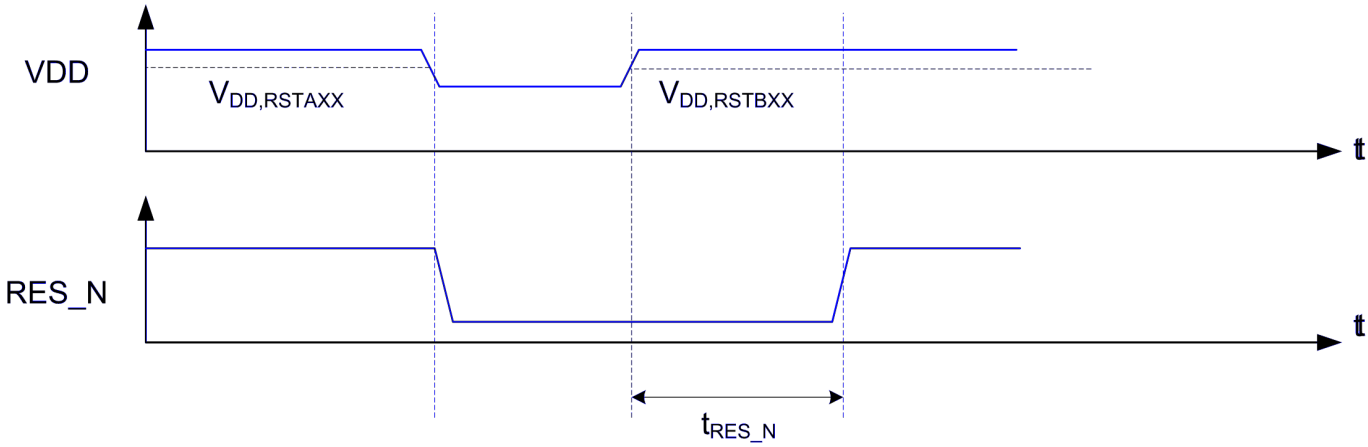
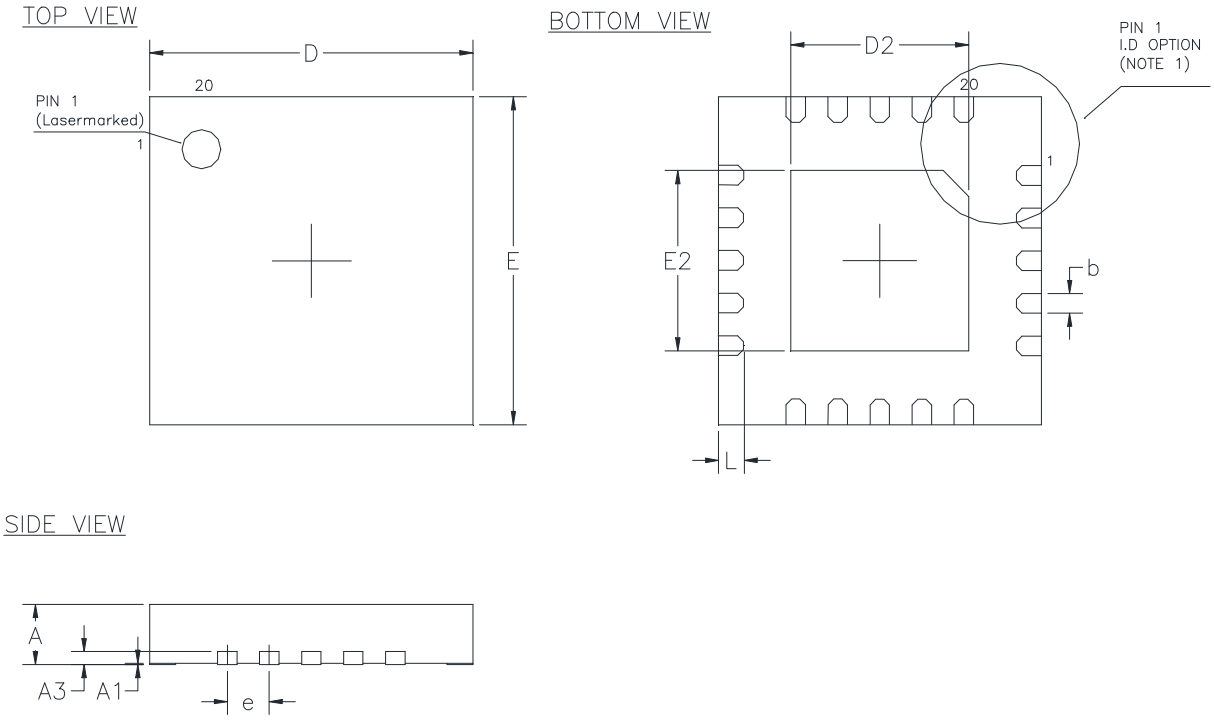


Fig. 16: RES_N in case of VDD UV events

7 Package Information

The device is assembled in a QFN20L5 package that is comparable to the variant VHHC-2 of JEDEC standard MO-220, Issue K. The deviation is the size of the die paddle (typ. 2.75mm x typ. 2.75mm).



Description	Symbol	mm			inch		
		min	typ	max	min	typ	max
Package height	A	0.80	0.90	1.00	0.031	0.035	0.039
Stand off	A1	0.00	0.02	0.05	0.000	0.00079	0.002
Thickness of terminal leads, including lead finish	A3	--	0.20 REF	--	--	0.0079 REF	--
Width of terminal leads	b	0.25	0.3	0.35	0.010	0.012	0.014
Package length / width	D / E	--	5.00 BSC	--	--	0.197 BSC	--
Length / width of exposed pad	D2 / E2	2.60	2.75	2.90	0.102	0.108	0.114
Lead pitch	e	--	0.65 BSC	--	--	0.026 BSC	--
Length of terminal for soldering to substrate	L	0.35	0.40	0.45	0.014	0.016	0.018
Number of terminal positions	N		20			20	

Note: the mm values are valid, the inch values contains rounding errors

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