Data Sheet

CDK8307

12/13-bit, 20/40/50/65/80MSPS, Eight Channel, Ultra Low Power ADC with LVDS

FEATURES

- 20/40/50/65/80MSPS max sampling rate
- Low Power Dissipation
  - 23mW/channel at 20MSPS
  - 35mW/channel at 40MSPS
  - 41mW/channel at 50MSPS
  - 51mW/channel at 65MSPS
  - 59mW/channel at 80MSPS
- 72.2dB SNR at 8MHz F_{IN}
- 0.5µs startup time from Sleep
- 15µs startup time from Power Down
- Internal reference circuitry requires no external components
- Internal offset correction
- Reduced power dissipation modes available
  - 34mW/channel at 50MSPS
  - 71.5dB SNR at 8MHz F_{IN}
- Coarse and fine gain control
- 1.8V supply voltage
- Serial LVDS output
  - 12- and 14-bit output available
- Package alternatives
  - TQFP-80
  - QFN-64

APPLICATIONS

- Medical Imaging
- Wireless Infrastructure
- Test and Measurement
- Instrumentation

General Description

The CDK8307 is a high performance low power octal analog-to-digital converter (ADC). The ADC employs internal reference circuitry, a serial control interface and serial LVDS output data, and is based on a proprietary structure.

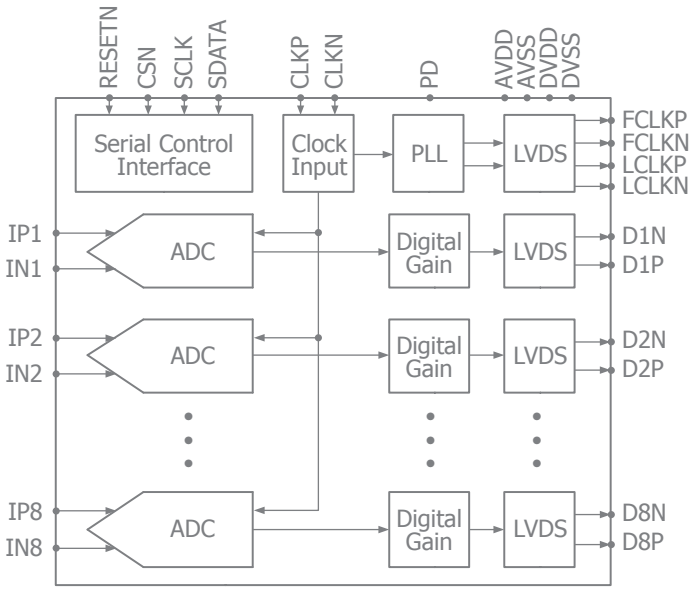
An integrated PLL multiplies the input sampling clock by a factor of 12 or 14, according to the LVDS output setting. The multiplied clock is used for data serialization and data output. Data and frame synchronization output clocks are supplied for data capture at the receiver.

Various modes and configuration settings can be applied to the ADC through the serial control interface (SPI). Each channel can be powered down independently and data format can be selected through this interface. A full chip idle mode can be set by a single external pin. Register settings determines the exact function of this external pin.

The CDK8307 is designed to easily interface with field-programmable gate arrays (FPGAs) from several vendors.

The very low startup times of the CDK8307 allow significant power reduction in duty-cycled systems, by utilizing the Sleep Mode or Power Down Mode when the receive path is idle.

Block Diagram



Exar Corporation
48720 Kato Road, Fremont CA 94538, USA

www.exar.com
Tel. +1 510 668-7000 - Fax. +1 510 668-7001

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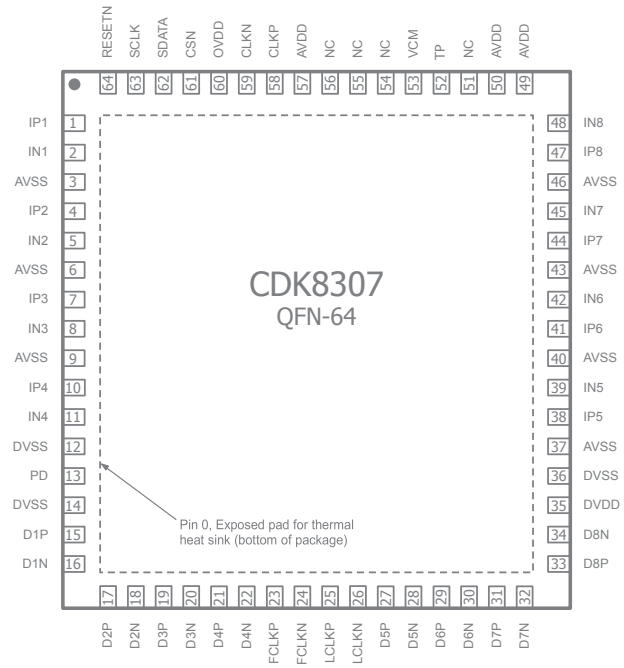
Ordering Information

Part Number	Speed	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CDK8307AITQ80	20MSPS	TQFP-80	Yes	Yes	-40°C to +85°C	Tray
CDK8307AILP64	20MSPS	QFN-64	Yes	Yes	-40°C to +85°C	Tray
CDK8307BITQ80	40MSPS	TQFP-80	Yes	Yes	-40°C to +85°C	Tray
CDK8307BILP64	40MSPS	QFN-64	Yes	Yes	-40°C to +85°C	Tray
CDK8307CITQ80	50MSPS	TQFP-80	Yes	Yes	-40°C to +85°C	Tray
CDK8307CILP64	50MSPS	QFN-64	Yes	Yes	-40°C to +85°C	Tray
CDK8307DITQ80	65MSPS	TQFP-80	Yes	Yes	-40°C to +85°C	Tray
CDK8307DILP64	65MSPS	QFN-64	Yes	Yes	-40°C to +85°C	Tray
CDK8307EITQ80	80MSPS	TQFP-80	Yes	Yes	-40°C to +85°C	Tray
CDK8307EILP64	80MSPS	QFN-64	Yes	Yes	-40°C to +85°C	Tray

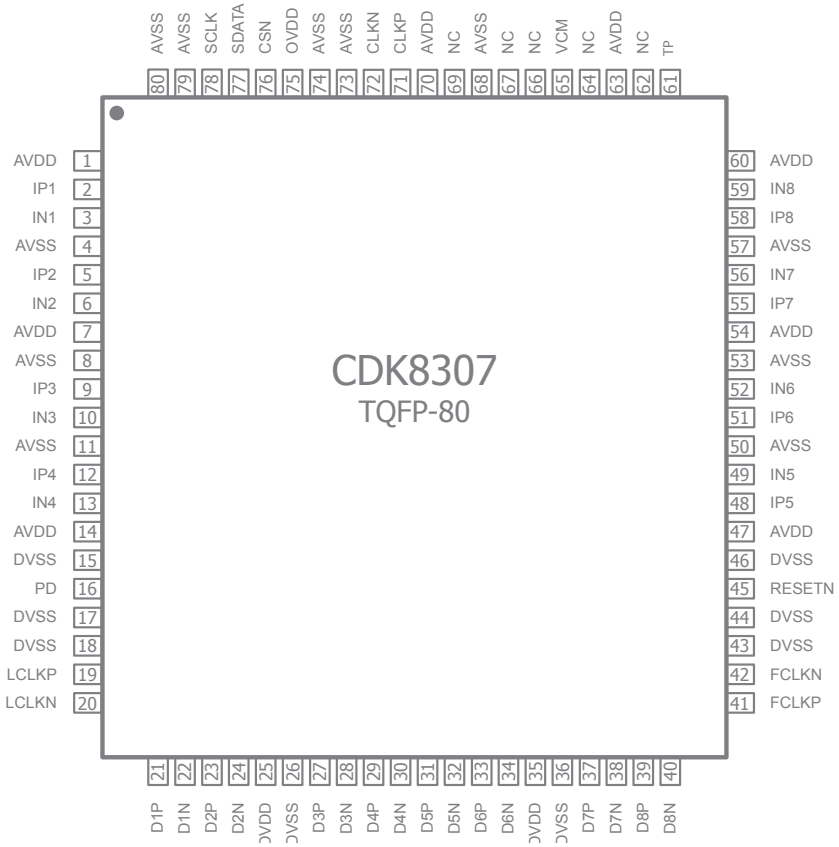
Moisture sensitivity level for QFN package is MSL-2A, for TQFP package is MSL-3.

Pin Configurations

QFN-64



TQFP-80



Pin Assignments - QFN

Pin No.	Pin Name	Description
QFN-64		
49, 50, 57	AVDD	Analog power supply, 1.8V
3, 6, 9, 37, 40, 43, 46	AVSS	Analog ground
1	IP1	Positive differential input signal, channel 1
2	IN1	Negative differential input signal, channel 1
4	IP2	Positive differential input signal, channel 2
5	IN2	Negative differential input signal, channel 2
7	IP3	Positive differential input signal, channel 3
8	IN3	Negative differential input signal, channel 3
10	IP4	Positive differential input signal, channel 4
11	IN4	Negative differential input signal, channel 4
38	IP5	Positive differential input signal, channel 5
39	IN5	Negative differential input signal, channel 5
41	IP6	Positive differential input signal, channel 6
42	IN6	Negative differential input signal, channel 6
44	IP7	Positive differential input signal, channel 7
45	IN7	Negative differential input signal, channel 7
47	IP8	Positive differential input signal, channel 8
48	IN8	Negative differential input signal, channel 8
12, 14, 36	DVSS	Digital ground
35	DVDD	Digital and I/O power supply, 1.8V
13	PD	Power-down input. Activate after applying power in order to initialize the ADC correctly. Alternatively use the SPI power down feature.
15	D1P	LVDS channel 1, positive output
16	D1N	LVDS channel 1, negative output
17	D2P	LVDS channel 2, positive output
18	D2N	LVDS channel 2, negative output
19	D3P	LVDS channel 3, positive output
20	D3N	LVDS channel 3, negative output
21	D4P	LVDS channel 4, positive output
22	D4N	LVDS channel 4, negative output
27	D5P	LVDS channel 5, positive output
28	D5N	LVDS channel 5, negative output
29	D6P	LVDS channel 6, positive output
30	D6N	LVDS channel 6, negative output
31	D7P	LVDS channel 7, positive output
32	D7N	LVDS channel 7, negative output
33	D8P	LVDS channel 8, positive output
34	D8N	LVDS channel 8, negative output
23	FCLKP	LVDS frame clock (1x), positive output
24	FCLKN	LVDS frame clock (1x), negative output
25	LCLKP	LVDS bit clock, positive output

Pin Assignments QFN *(Continued)*

Pin No.	Pin Name	Description
26	LCLKN	LVDS bit clock, negative output
51, 54, 55, 56	NC	Not connected
52	TP	Test pin. Leave open (un-connected) or connect to GND.
53	VCM	Common mode output pin, 0.5 AVDD
58	CLKP	Positive differential input clock
59	CLKN	Negative differential input clock.
60	OVDD	Digital CMOS inputs supply voltage (1.7V to 3.6V)
61	CSN	Chip select enable. Active low.
62	SDATA	Serial data input
63	SCLK	Serial clock input
64	RESETN	Reset SPI interface

Pin Assignments - TQFP

Pin No.	Pin Name	Description
TQFP		
1, 7, 14, 47, 54, 60, 63, 70	AVDD	Analog power supply, 1.8V
4, 8, 11, 50, 53, 57, 68, 73, 74, 79, 80	AVSS	Analog ground
2	IP1	Positive differential input signal, channel 1
3	IN1	Negative differential input signal, channel 1
5	IP2	Positive differential input signal, channel 2
6	IN2	Negative differential input signal, channel 2
9	IP3	Positive differential input signal, channel 3
10	IN3	Negative differential input signal, channel 3
12	IP4	Positive differential input signal, channel 4
13	IN4	Negative differential input signal, channel 4
48	IP5	Positive differential input signal, channel 5
49	IN5	Negative differential input signal, channel 5
51	IP6	Positive differential input signal, channel 6
52	IN6	Negative differential input signal, channel 6
55	IP7	Positive differential input signal, channel 7
56	IN7	Negative differential input signal, channel 7
58	IP8	Positive differential input signal, channel 8
59	IN8	Negative differential input signal, channel 8
15, 17, 18, 26, 36, 43, 44, 46	DVSS	Digital ground
25, 35	DVDD	Digital and I/O power supply, 1.8V
16	PD	Power-down input. Activate after applying power in order to initialize the ADC correctly. Alternatively use the SPI power down feature.
19	LCKP	LVDS bit clock, positive output
20	LCKN	LVDS bit clock, negative output
21	D1P	LVDS channel 1, positive output
22	D1N	LVDS channel 1, negative output
23	D2P	LVDS channel 2, positive output
24	D2N	LVDS channel 2, negative output
27	D3P	LVDS channel 3, positive output
28	D3N	LVDS channel 3, negative output
29	D4P	LVDS channel 4, positive output
30	D4N	LVDS channel 4, negative output
31	D5P	LVDS channel 5, positive output
32	D5N	LVDS channel 5, negative output
33	D6P	LVDS channel 6, positive output
34	D6N	LVDS channel 6, negative output
37	D7P	LVDS channel 7, positive output
38	D7N	LVDS channel 7, negative output
39	D8P	LVDS channel 8, positive output
40	D8N	LVDS channel 8, negative output

Pin Assignments - TQFP *(Continued)*

Pin No.	Pin Name	Description
41	FCLKP	LVDS frame clock (1x), positive output
42	FCLKN	LVDS frame clock (1x), negative output
45	RESETN	Reset SPI interface
61	TP	Test pin. Leave open (un-connected) or connect to GND.
62, 64, 66, 67, 69	NC	Not connected
65	VCM	Common mode output pin, 0.5 AVDD
71	CLKP	Positive differential input clock
72	CLKN	Negative differential input clock.
75	OVDD	Digital CMOS inputs supply voltage (1.7V to 3.6V)
76	CSN	Chip select enable. Active low.
77	SDATA	Serial data input
78	SCLK	Serial clock input

Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Reference Pin	Min	Max	Unit
AVDD	AVSS	-0.3	+2.3	V
DVDD	DVSS	-0.3	+2.3	V
OVDD	AVSS	-0.3	+3.9	V
AVSS, DVSS	DVSS / AVSS	-0.3	+0.3	V
Analog inputs and outpts (IPx, INx)	AVSS	-0.3	+2.3	V
CLKx	AVSS	-0.3	+3.9	V
LVDS outputs	DVSS	-0.3	+2.3	V
Digital inputs	DVSS	-0.3	+3.9	V

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			TBD	°C
Storage Temperature Range	-60		+150	°C
Lead Temperature (Soldering, 10s)		J-STD-020		

ESD Protection

Product	QFN-64
Human Body Model (HBM)	2kV
Charged Device Model (CDM)	500V

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C

This device can be damaged by ESD. Even though this product is protected with state-of-the-art ESD protection circuitry, damage may occur if the device is not handled with appropriate precautions. ESD damage may range from device failure to performance degradation. Analog circuitry may be more susceptible to damage as vary small parametric changes can result in specification noncompliance.

Electrical Characteristics

(AVDD = 1.8V, DVDD = 1.8V, OVDD = 1.8V, 50MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 14-bit output, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy						
	No Missing Codes			Guaranteed		
	Offset Error	Offset error after digital offset cancellation		1		LSB
	Gain Error				±6	%FS
	Gain Matching	Gain matching between channels. ±3sigma value at worst case conditions.		±0.5		%FS
DNL	Differential Non-Linearity	12-bit level		±0.2		LSB
INL	Integral Non-Linearity	12-bit level		±0.6		LSB
V_{CMO}	Common Mode Voltage Output			$V_{AVDD}/2$		V
Analog Input						
V_{CMI}	Input Common Mode	Analog input common mode voltage	V_{CM} -0.1		V_{CM} +0.2	V
V_{FSR}	Full Scale Range	Differential input voltage range		2.0		V_{pp}
	Input Capacitance	Differential input capacitance		2		pF
	Bandwidth	Input bandwidth	500			MHz
Power Supply						
AVDD	Analog Supply Voltage		1.7	1.8	2.0	V
DVDD	Digital Supply Voltage (up to 65MSPS)	Digital and output driver supply voltage	1.7	1.8	2.0	V
	Digital Supply Voltage (above 65MSPS)	Digital and output driver supply voltage	1.8	1.9	2.0	V
OVDD	Digital CMOS Input Supply Voltage		1.7	1.8	3.6	V

Electrical Characteristics - CDK8307A

(AVDD = 1.8V, DVDD = 1.8V, OVDD = 1.8V, 20MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 14-bit output, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Performance						
SNR	Signal to Noise Ratio	F_{IN} = 8MHz	70	72.2		dBFS
		F_{IN} = 30MHz		71.5		dBFS
SINAD	Signal to Noise and Distortion Ratio	F_{IN} = 8MHz	69	71.5		dBFS
		F_{IN} = 30MHz		70.7		dBFS
SFDR	Spurious Free Dynamic Range	F_{IN} = 8MHz	75	82		dBc
		F_{IN} = 30MHz		77		dBc
HD2	Second order Harmonic Distortion	F_{IN} = 8MHz	85	95		dBc
		F_{IN} = 30MHz		95		dBc
HD3	Third order Harmonic Distortion	F_{IN} = 8MHz	75	82		dBc
		F_{IN} = 30MHz		77		dBc
ENOB	Effective number of Bits	F_{IN} = 8MHz		11.6		bits
		F_{IN} = 30MHz		11.5		bits
Crosstalk		See note (1) on page 13		95		dBc
Power Supply						
	Analog supply current			47		mA
	Digital supply current	Digital and output driver supply		54		mA
	Analog power Dissipation			84		mW
	Digital power Dissipation			97		mW
	Total power Dissipation			180		mW
	Power Down Dissipation	Power down mode		10		µW
	Sleep Mode Dissipation	Deep sleep mode		30		mW

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Sleep Channel Mode Dissipation	All channels. in sleep ch. mode (light sleep)		46		mW
	Sleep Channel Mode Savings	Power dissipation savings per channel off		17		mW
Clock Inputs						
	Maximum Conversion Rate		20			MSPS
	Minimum Conversion Rate				15	MSPS

Electrical Characteristics - CDK8307B

(AVDD = 1.8V, DVDD = 1.8V, OVDD = 1.8V, 40MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 14-bit output, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Performance						
SNR	Signal to Noise Ratio	F_{IN} = 8MHz	70	72.2		dBFS
		F_{IN} = 30MHz		71.5		dBFS
SINAD	Signal to Noise and Distortion Ratio	F_{IN} = 8MHz	69	71.5		dBFS
		F_{IN} = 30MHz		70.7		dBFS
SFDR	Spurious Free Dynamic Range	F_{IN} = 8MHz	75	82		dBc
		F_{IN} = 30MHz		77		dBc
HD2	Second order Harmonic Distortion	F_{IN} = 8MHz	85	95		dBc
		F_{IN} = 30MHz		95		dBc
HD3	Third order Harmonic Distortion	F_{IN} = 8MHz	75	82		dBc
		F_{IN} = 30MHz		77		dBc
ENOB	Effective number of Bits	F_{IN} = 8MHz		11.6		bits
		F_{IN} = 30MHz		11.5		bits
Crosstalk		See note (1) on page 13		95		dBc
Power Supply						
	Analog supply current			90		mA
	Digital supply current	Digital and output driver supply		67		mA
	Analog power Dissipation			162		mW
	Digital power Dissipation			120		mW
	Total power Dissipation			280		mW
	Power Down Dissipation	Power down mode		10		µW
	Sleep Mode Dissipation	Deep sleep mode		41		mW
	Sleep Channel Mode Dissipation	All channels. in sleep ch. mode (light sleep)		71		mW
	Sleep Channel Mode Savings	Power dissipation savings per channel off		26		mW
Clock Inputs						
	Maximum Conversion Rate		40			MSPS
	Minimum Conversion Rate				20	MSPS

Electrical Characteristics - CDK8307C

(AVDD = 1.8V, DVDD = 1.8V, OVDD = 1.8V, 50MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 14-bit output, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Performance						
SNR	Signal to Noise Ratio	F_{IN} = 8MHz	70	72.2		dBFS
		F_{IN} = 30MHz		71.5		dBFS
SINAD	Signal to Noise and Distortion Ratio	F_{IN} = 8MHz	69	71.5		dBFS
		F_{IN} = 30MHz		70.7		dBFS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SFDR	Spurious Free Dynamic Range	F_{IN} = 8MHz	75	82		dBc
		F_{IN} = 30MHz		77		dBc
HD2	Second order Harmonic Distortion	F_{IN} = 8MHz	85	95		dBc
		F_{IN} = 30MHz		95		dBc
HD3	Third order Harmonic Distortion	F_{IN} = 8MHz	75	82		dBc
		F_{IN} = 30MHz		77		dBc
ENOB	Effective number of Bits	F_{IN} = 8MHz		11.6		bits
		F_{IN} = 30MHz		11.5		bits
Crosstalk		See note (1) on page 13		95		dBc
Power Supply						
	Analog supply current			111		mA
	Digital supply current	Digital and output driver supply		73		mA
	Analog power Dissipation			200		mW
	Digital power Dissipation			132		mW
	Total power Dissipation			331		mW
	Power Down Dissipation	Power down mode		10		µW
	Sleep Mode Dissipation	Deep sleep mode		46		mW
	Sleep Channel Mode Dissipation	All channels. in sleep ch. mode (light sleep)		83		mW
	Sleep Channel Mode Savings	Power dissipation savings per channel off		31		mW
Clock Inputs						
	Maximum Conversion Rate		50			MSPS
	Minimum Conversion Rate				20	MSPS

Electrical Characteristics - CDK8307D

(AVDD = 1.8V, DVDD = 1.8V, OVDD = 1.8V, 65MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 14-bit output, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Performance						
SNR	Signal to Noise Ratio	F_{IN} = 8MHz	70	72.2		dBFS
		F_{IN} = 30MHz		71.5		dBFS
SINAD	Signal to Noise and Distortion Ratio	F_{IN} = 8MHz	69	71.5		dBFS
		F_{IN} = 30MHz		70.7		dBFS
SFDR	Spurious Free Dynamic Range	F_{IN} = 8MHz	75	82		dBc
		F_{IN} = 30MHz		77		dBc
HD2	Second order Harmonic Distortion	F_{IN} = 8MHz	85	95		dBc
		F_{IN} = 30MHz		95		dBc
HD3	Third order Harmonic Distortion	F_{IN} = 8MHz	75	82		dBc
		F_{IN} = 30MHz		77		dBc
ENOB	Effective number of Bits	F_{IN} = 8MHz		11.6		bits
		F_{IN} = 30MHz		11.5		bits
Crosstalk		See note (1) on page 13		95		dBc
Power Supply						
	Analog supply current			143		mA
	Digital supply current	Digital and output driver supply		83		mA
	Analog power Dissipation			257		mW
	Digital power Dissipation			149		mW
	Total power Dissipation			405		mW
	Power Down Dissipation	Power down mode		10		µW
	Sleep Mode Dissipation	Deep sleep mode		54		mW
	Sleep Channel Mode Dissipation	All channels. in sleep ch. mode (light sleep)		103		mW

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Sleep Channel Mode Savings	Power dissipation savings per channel off		38		mW
Clock Inputs						
	Maximum Conversion Rate		65			MSPS
	Minimum Conversion Rate				20	MSPS

Electrical Characteristics - CDK8307E

(AVDD = 1.8V, DVDD = 1.8V, OVDD = 1.8V, 80MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 12-bit output, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Performance						
SNR	Signal to Noise Ratio	F_{IN} = 8MHz	68.5	70.1		dBFS
		F_{IN} = 30MHz		70		dBFS
SINAD	Signal to Noise and Distortion Ratio	F_{IN} = 8MHz	68	69.6		dBFS
		F_{IN} = 30MHz		69.5		dBFS
SFDR	Spurious Free Dynamic Range	F_{IN} = 8MHz	74	77		dBc
		F_{IN} = 30MHz		76		dBc
HD2	Second order Harmonic Distortion	F_{IN} = 8MHz	85	90		dBc
		F_{IN} = 30MHz		90		dBc
HD3	Third order Harmonic Distortion	F_{IN} = 8MHz	75	77		dBc
		F_{IN} = 30MHz		76		dBc
ENOB	Effective number of Bits	F_{IN} = 8MHz		11.3		bits
		F_{IN} = 30MHz		11.3		bits
Crosstalk		See note (1) on page 13		95		dBc
Power Supply						
	Analog supply current			173		mA
	Digital supply current	Digital and output driver supply		88		mA
	Analog power Dissipation			312		mW
	Digital power Dissipation			158		mW
	Total power Dissipation			470		mW
	Power Down Dissipation	Power down mode		10		µW
	Sleep Mode Dissipation	Deep sleep mode		56		mW
	Sleep Channel Mode Dissipation	All channels. in sleep ch. mode (light sleep)		116		mW
	Sleep Channel Mode Savings	Power dissipation savings per channel off		44		mW
Clock Inputs						
	Maximum Conversion Rate		80			MSPS
	Minimum Conversion Rate				40	MSPS

Digital and Timing Electrical Characteristics

(AVDD = 1.8V, DVDD = 1.8V, OVDD = 1.8V, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Clock Inputs						
	Duty Cycle		20		80	%high
	Compliance		CMOS, LVDS, LVPECL			
	Input range, differential	Differential input swing	±200			mV_{pp}
	Input range, sine	Differential input swing, sine wave clock input	±800			mV_{pp}
	Input range, CMOS	CLKN connected to ground		V_{OVDD}		mV_{pp}
	Input common mode voltage	Keep voltages within gnd and voltage of OVDD	0.3		V_{OVDD} -0.3	V
	Input capacitance	Differential		2		pF

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Logic Inputs (CMOS)						
V_{IH}	High Level Input Voltage	$V_{OVDD} \geq 3.0V$	2			V
		$V_{OVDD} = 1.7V – 3.0V$	$0.8 \cdot V_{OVDD}$			V
V_{IL}	Low Level Input Voltage	$V_{OVDD} \geq 3.0V$	0		0.8	V
		$V_{OVDD} = 1.7V – 3.0V$	0		$0.2 \cdot V_{OVDD}$	V
I_{IH}	High Level Input Leakage Current				±10	µA
I_{IL}	Low Level Input Leakage Current				±10	µA
C_I	Input Capacitance			3		pF
Data Outputs (LVDS)						
	Compliance		LVDS			
V_{OUT}	Differential Output Voltage			350		mV
V_{CM}	Output Common Mode Voltage			1.2		V
	Output Coding	Default/Optional	Offset Binary/2's Complement			
Timing Characteristics						
T_{AP}	Aperture Delay			0.8		ns
ε_{RMS}	Aperture Jitter			<0.5		ps
T_{PD}	Start up Time from Power Down	Start up time from Power Down to Active Mode. References have reached 99% of final value. (See section Clock Frequency)	260		992	clock cycles
				15		µs
T_{SLP}	Startup Time from Sleep	Start up time from Sleep Mode to Active Mode		0.5		µs
T_{OVR}	Out Of Range Recovery Time			1		clk cycles
T_{LAT}	Pipeline Delay			14		clk cycles
LVDS Output Timing Characterisctics						
t_{data}	LCLK to Data Delay Time	Excluding programmable phase shift		250		ps
t_{PROP}	Clock Propogation Delay		$7 \cdot T_{LVDS}$ +2.6	$7 \cdot T_{LVDS}$ +3.5	$7 \cdot T_{LVDS}$ +4.2	ns
	LVDS Bit-Clock Duty-Cycle		45		55	% LCLK cycle
	Frame clock cycle-to-cycle jitter				2.5	% LCLK cycle
T_{EDGE}	Data Rise- and Fall Time	Calculated from 20% to 80%		0.4		ns
$T_{CLKEDGE}$	Clock Rise- and Fall Time	Calculated from 20% to 80%		0.4		ns

Note:

(1) Signal applied to 7 channels (F_{IN0}). Measurement taken on one channel with full scale at F_{IN1}. F_{IN1} = 8MHz, F_{IN0} = 9.9MHz

(2) The outputs will be functional with higher loads. However, it is recommended to keep the load on output data bits as low as possible to keep dynamic currents and resulting switching noise at a minimum.

LVDS Timing Diagrams

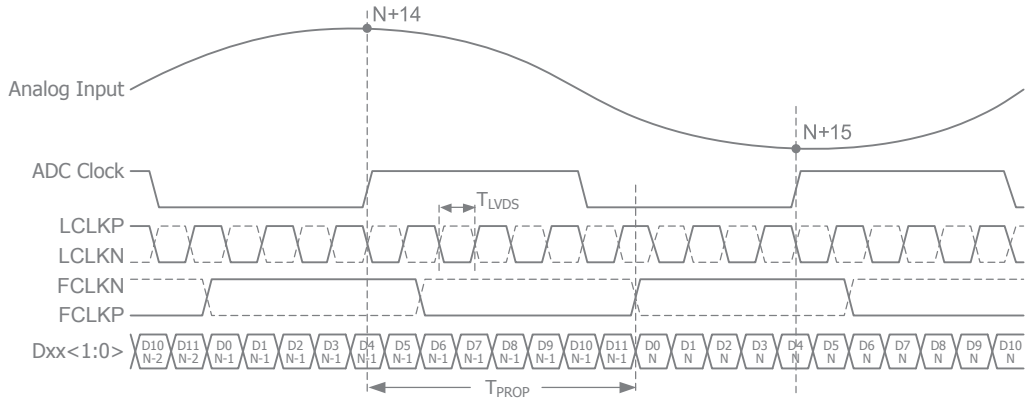


Figure 1. 12-bit Output, DDR Mode

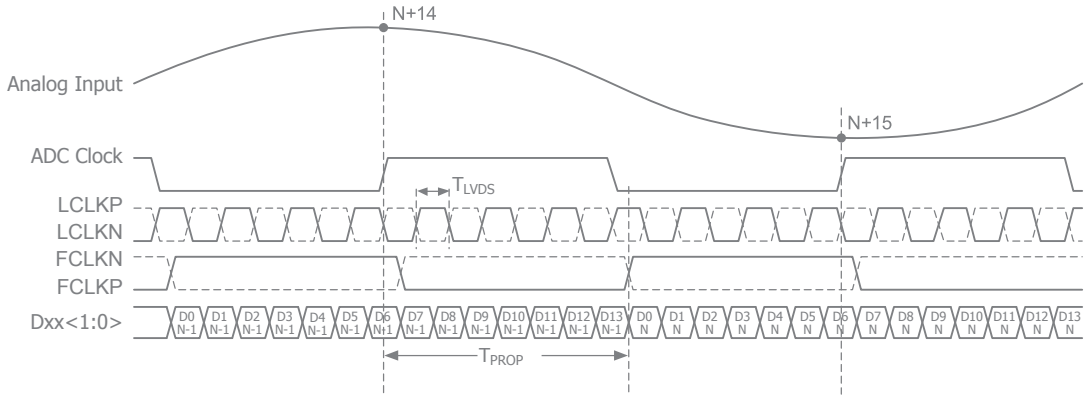


Figure 2. 14-bit Output, DDR Mode

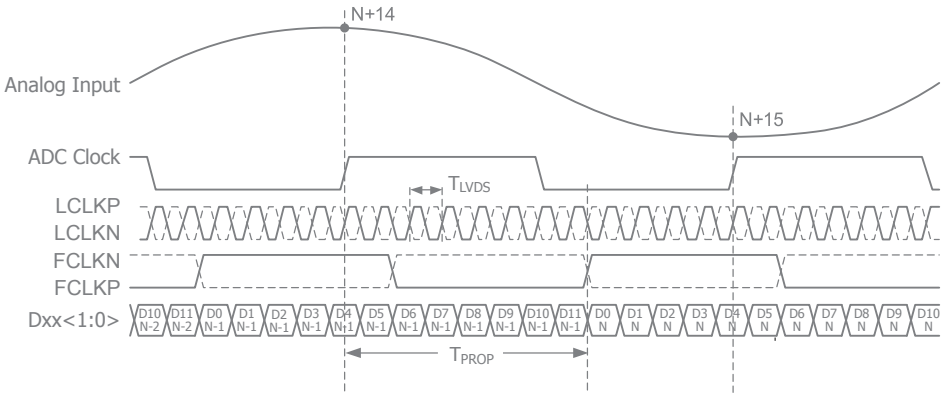


Figure 3. 12-bit Output, SDR Mode

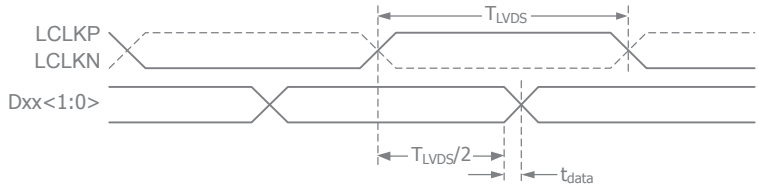


Figure 4. Data Timing

Serial Interface

The CDK8307 configuration registers can be accessed through a serial interface formed by the pins SDATA (serial interface data), SCLK (serial interface clock) and CSN (chip select, active low). The following occurs when CSN is set low:

- Serial data are shifted into the chip
- At every rising edge of SCLK, the value present at SDATA is latched
- SDATA is loaded into the register every 24th rising edge of SCLK

Multiples of 24-bit words data can be loaded within a single active CSN pulse. If more than 24 bits are loaded into SDATA during one active CSN pulse, only the first 24 bits are kept. The excess bits are ignored. Every 24-bit word is divided into two parts:

- The first eight bits form the register address
- The remaining 16 bits form the register data

Acceptable SCLK frequencies are from 20MHz down to a few hertz. Duty-cycle does not have to be tightly controlled.

Timing Diagram

Figure 5 shows the timing of the serial port interface. Table 1 explains the timing variables used in the Timing Diagram.

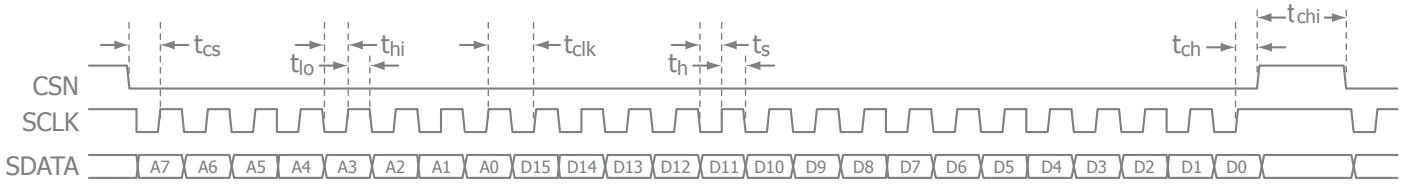


Figure 5. Serial Port Interface Timing Diagram

Table 1. Serial Port Interface Timing Definitions

Parameter	Description	Minimum Value	Unit
t_{cs}	Setup time between CSN and SCLK	8	ns
t_{ch}	Hold time between CSN and SCLK	8	ns
t_{hi}	SCLK high time	20	ns
t_{lo}	SCLK low time	20	ns
t_{clk}	SCLK period	50	ns
t_s	Data setup time	5	ns
t_h	Data hold time	5	ns

Register Initialization

Before CDK8307 can be used, the internal registers must be initialized to their default values and power down must be activated. This can be done immediately after applying supply voltage to the circuit. Register initialization can be done in one of two ways:

1. By applying a low-going pulse (minimum 20ns) on the RESETN pin (asynchronous).
2. By using the serial interface to set the RST bit high. Internal registers are reset to default values when this bit is set. The RST bit is self-reset to zero. When using this method, do not apply any low-going pulse on the RESETN pin.

Power down initialization can be done in one of two ways:

1. By applying a high-going pulse (minimum 20ns) on the PD pin (asynchronous).
2. By cycling the SPI register 0Fhex PD bit to high (reg value '0200'hex) and then low (reg value '0000'hex).

Serial Register Map

Table 2. Summary of Functions Supported by the Serial Interface

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
rst	Software reset. This bit is self-clearing	Inactive																X	00
pd_ch<8:1>	Channel-specific power-down	Inactive									X	X	X	X	X	X	X	X	0F
sleep	Go to sleep-mode	Inactive								X									
pd	Go to power-down	Inactive							X										
pd_pin_cfg<1:0>	Configures the PD pin for sleep-modes	PD pin configured for power-down mode					X	X											
ilvds_lclk<2:0>	LVDS current drive programmability for LCLKP and LCLKN pins	3.5mA drive														X	X	X	11
ilvds_frame<2:0>	LVDS current drive programmability for FCLKP and FCLKN pins	3.5mA drive										X	X	X					
ilvds_dat<2:0>	LVDS current drive programmability for output data pins	3.5mA drive						X	X	X									
en_lvds_term	Enables internal termination for LVDS buffers	Termination disabled		X															12
term_lclk<2:0>	Programmable termination for LCLKN and LCLKP buffers	Termination disabled		1												X	X	X	
term_frame<2:0>	Programmable termination for FCLKN and FCLKP buffers	Termination disabled		1								X	X	X					
term_dat<2:0>	Programmable termination for output data buffers	Termination disabled		1				X	X	X									
invert_ch<8:1>	Swaps the polarity of the analog input pins electrically	IPx is positive input									X	X	X	X	X	X	X	X	24
en_ramp	Enables a repeating full-scale ramp pattern on the outputs	Inactive										X	0	0					25
dual_custom_pat	Enable the mode wherein the output toggles between two defined codes	Inactive										0	X	0					
single_custom_pat	Enables the mode wherein the output is a constant specified code	Inactive										0	0	X					
bits_custom1<13:0>	Bits for the single custom pattern and for the first code of the dual custom pattern. <0> is the LSB	Inactive	X	X	X	X	X	X	X	X	X	X	X	X	X	X			26
bits_custom2<13:0>	Bits for the second code of the dual custom pattern	Inactive	X	X	X	X	X	X	X	X	X	X	X	X	X	X			27
gain_ch1<3:0>	Programmable gain for channel 1	0dB gain													X	X	X	X	2A
gain_ch2<3:0>	Programmable gain for channel 2	0dB gain									X	X	X	X					
gain_ch3<3:0>	Programmable gain for channel 3	0dB gain					X	X	X	X									
gain_ch4<3:0>	Programmable gain for channel 4	0dB gain	X	X	X	X													
gain_ch5<3:0>	Programmable gain for channel 5	0dB gain	X	X	X	X													2B
gain_ch6<3:0>	Programmable gain for channel 6	0dB gain					X	X	X	X									
gain_ch7<3:0>	Programmable gain for channel 7	0dB gain									X	X	X	X					
gain_ch8<3:0>	Programmable gain for channel 8	0dB gain													X	X	X	X	

Table 2. Summary of Functions Supported by the Serial Interface *(Continued)*

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
phase_ddr<1:0>	Controls the phase of LCLK output relative to data	90 degrees										X	X						42
pat_deskew	Enable deskew pattern mode	Inactive															0	X	45
pat_sync	Enable sync pattern mode	Inactive															X	0	
btc_mode	Binary two's complement format for ADC output data	Straight offset binary														X			46
msb_first	Serialized ADC output data comes out with MSB first	LSB-first output													X				
en_sdr	Enable SDR output mode. LCLK becomes a 12x input clock	DDR output mode												X					
fall_sdr	Controls whether the LCLK rising or falling edge comes in the middle of the data window when operating in SDR mode	Rising edge of LCLK comes in the middle of the data window			X									1					
perfm_cntrl<2:0>	ADC performance control	Nominal														X	X	X	50
ext_vcm_bc<1:0>	VCM buffer driving strength control	Nominal											X	X					
lvds_pd_mode	Controls LVDS power down mode	High z mode																X	52
lvds_num_bits	Sets the number of LVDS output bits	12-bit															X		53
lvds_advance	Advance LVDS data bits and frame clock by one clock cycle	Inactive											0	X					
lvds_delay	Delay LVDS data bits and frame clock by one clock cycle	Inactive											X	0					
fs_cntrl<5:0>	Fine adjust ADC full scale range	0% change											X	X	X	X	X	X	55
clk_freq<1:0>	Input clock frequency	65MHz															X	X	56

Description of Serial Registers

Table 3. Software Reset

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
rst	Self-clearing software reset	Inactive																X	00

Setting the *rst* register bit to '1', resets all internal registers including the *rst* register bit itself.

Table 4. Power-Down Modes

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
pd_ch<8:1>	Channel-specific power-down	Inactive									X	X	X	X	X	X	X	X	0F
sleep	Go to sleep-mode	Inactive								X									
pd	Go to power-down	Inactive							X										
pd_pin_cfg<1:0>	Configures the PD pin for sleep-mode	PD pin configured for power-down mode					X	X											
lvds_pd_mode	Controls LVDS power down mode	High z mode																X	52

Setting *pd_ch<n>* = '1', powers down channel *<n>* of the ADC. Setting *sleep* = '1', powers down the entire chip, except the band-gap reference circuit.

Setting *pd* = '1' completely powers down the chip, including the band-gap reference circuit. Start-up time from this mode is significantly longer than from the *sleep* and *pd_ch<n>* modes.

Setting *pdn_pin_cfg* = '1' configures the circuit to enter *sleep* mode when the PD pin is set high. When *pdn_pin_cfg* = '0', which is the default, the circuit enters power down mode when the PD pin is set high.

The *lvds_pd_mode* register configures whether the LVDS data output drivers are powered down or not in sleep and sleep channel modes. LCLK and FCLK drivers are not affected by this register, and are always on in sleep and sleep channel modes. If *lvds_pd_mode* is set low (default), the LVDS output is put in high Z, and the driver is completely powered down. If *lvds_pd_mode* is set high, the LVDS output is set to constant 0, and the driver is still on during sleep and sleep channel modes.

Table 5. LVDS Drive Strength Programmability

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
ilvds_lclk<2:0>	LVDS current drive programmability for LCLKP and LCLKN pins.	3.5mA drive														X	X	X	11
ilvds_ frame<2:0>	LVDS current drive programmability for FCLKP and FCLKN pins.	3.5mA drive										X	X	X					
ilvds_dat<2:0>	LVDS current drive programmability for output data pins.	3.5mA drive						X	X	X									

The current delivered by the LVDS output drivers can be configured as shown in Table 6. The default current is 3.5mA, which is what the LVDS standard specifies.

Setting the *ilvds_lclk<2:0>* register controls the current drive strength of the LVDS clock output on the LCLKP and LCLKN pins.

Setting the *ilvds_frame<2:0>* register controls the current drive strength of the frame clock output on the FCLKP and FCLKN pins.

Setting the *ilvds_dat<2:0>* register controls the current drive strength of the data outputs on the D[8:1]P and D[8:1] N pins.

Table 6. LVDS Output Drive Strength for LCLK, FCLK, and Data

ilvds_*<2:0>	LVDS Drive Strength
000	3.5 mA (default)
001	2.5 mA
010	1.5 mA
011	0.5 mA
100	7.5 mA
101	6.5 mA
110	5.5 mA
111	4.5 mA

Table 7. LVDS Internal Termination Programmability

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
en_lvds_term	Enables internal termination for LVDS buffers	Termination disabled		X															12
term_lclk<2:0>	Programmable termination for LCLKN and LCLKP buffers	Termination disabled		1												X	X	X	
term_ frame<2:0>	Programmable termination for FCLKN and FCLKP buffers	Termination disabled		1								X	X	X					
term_dat<2:0>	Programmable termination for DxP and DxN buffers	Termination disabled		1				X	X	X									

The off-chip load on the LVDS buffers may represent a characteristic impedance that is not perfectly matched with the PCB traces. This may result in reflections back to the LVDS outputs and loss of signal integrity. This effect can be mitigated by enabling an internal termination between the positive and negative outputs of each LVDS buffer. Internal termination mode can be selected by setting the *en_lvds_term* bit to '1'. Once this bit is set, the internal termination values for the bit clock, frame clock, and data buffers can be independently programmed using sets of three bits. Table 8 shows how the internal termination of the LVDS buffers are programmed. The values are typical values and can vary by up to ±20% from device to device and across temperature.

Table 8. LVDS Output INternal Termination for LCLK, FCLK, and Data

term_*<2:0>	LVDS Internal Termination
000	Termination Disabled
001	280Ω
010	165Ω
011	100Ω
100	125Ω
101	82Ω
110	67Ω
111	56Ω

Table 9. Analog Input Invert

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
invert_ch<8:1>	Swaps the polarity of the analog input pins electrically	IPx is positive input									X	X	X	X	X	X	X	X	24

The IPx pin represents the positive analog input pin, and INx represents the negative (complementary) input. Setting the bits marked *invert_ch* <8:1> (individual control for each channel) causes the inputs to be swapped. INx would then represent the positive input, and IPx the negative input.

Table 10. LVDS Test Patterns

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
en_ramp	Enables a repeating full-scale ramp pattern on the outputs	Inactive										X	0	0					25
dual_custom_pat	Enable the mode wherein the output toggles between two defined codes	Inactive										0	X	0					
single_custom_pat	Enables the mode wherein the output is a constant specified code	Inactive										0	0	X					
bits_custom1<13:0>	Bits for the single custom pattern and for the first code of the dual custom pattern. <0> is the LSB	Inactive	X	X	X	X	X	X	X	X	X	X	X	X	X	X			26
bits_custom2<13:0>	Bits for the second code of the dual custom pattern	Inactive	X	X	X	X	X	X	X	X	X	X	X	X	X	X			27
pat_deskew	Enable deskew pattern mode	Inactive															0	X	45
pat_sync	Enable sync pattern mode	Inactive															X	0	

To ease the LVDS synchronization setup of CDK8307, several test patterns can be set up on the outputs. Normal ADC data are replaced by the test pattern in these modes. Setting *en_ramp* to '1' sets up a repeating full-scale ramp pattern on all data outputs. The ramp starts at code zero and is increased 1LSB every clock cycle. It returns to zero code and starts the ramp again after reaching the full-scale code.

A constant value can be set up on the outputs by setting *single_custom_pat* to '1', and programming the desired value in *bits_custom1<13:0>*. In this mode, *bits_custom1<13:0>* replaces the ADC data at the output, and is controlled by LSB-first and MSB-first modes in the same way as normal ADC data are.

The device may also be made to alternate between two codes by programming *dual_custom_pat* to '1'. The two codes are the contents of *bits_custom1<13:0> and bits_custom2<13:0>.* Two preset patterns can also be selected:

1. Deskew pattern: Set using *pat_deskew,* this mode replaces the ADC output with '01010101010101' (two LSBs removed in 12 bit mode).
2. Sync pattern: Set using *pat_sync,* the normal ADC word is replaced by a fixed 1111110000000 word.

Note: Only one of the above patterns should be selected at the same time.

Table 11. Programmable Gain

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
gain_ch1<3:0>	Programmable gain for channel 1	0dB gain													X	X	X	X	2A
gain_ch2<3:0>	Programmable gain for channel 2	0dB gain									X	X	X	X					
gain_ch3<3:0>	Programmable gain for channel 3	0dB gain					X	X	X	X									
gain_ch4<3:0>	Programmable gain for channel 4	0dB gain	X	X	X	X													
gain_ch5<3:0>	Programmable gain for channel 5	0dB gain	X	X	X	X													2B
gain_ch6<3:0>	Programmable gain for channel 6	0dB gain					X	X	X	X									
gain_ch7<3:0>	Programmable gain for channel 7	0dB gain									X	X	X	X					
gain_ch8<3:0>	Programmable gain for channel 8	0dB gain													X	X	X	X	

CDK8307 includes a purely digital programmable gain option in addition to the Full-scale Control. The programmable gain of each channel can be individually set using a set of four bits, indicated as *gain_chn<3:0>* for Channel x. The gain setting is coded in binary from 0dB to 12dB, as shown in Table 12 on the following page.

Table 12. Gain Setting for Channels 1-8

gain_chx<3:0>	Channel x Gain Setting
0000	0dB
0001	1dB
0010	2dB
0011	3dB
0100	4dB
0101	5dB
0110	6dB
0111	7dB
1000	8dB
1001	9dB
1010	10dB
1011	11dB
1100	12dB
1101	Do not use
1110	Do not use
1111	Do not use

Table 13. LVDS Clock Programmability and Data Output Modes

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
phase_ddr<1:0>	Controls the phase of LCLK output relative to data	90 degrees										X	X						42
btc_mode	Binary two's complement format for ADC output data	Straight offset binary														X			46
msb_first	Serialized ADC output data comes out with MSB first	LSB-first output													X				
en_sdr	Enable SDR output mode. LCLK becomes a 12x input clock	DDR output mode												X					
fall_sdr	Controls whether the LCLK rising or falling edge comes in the middle of the data window when operating in SDR mode	Rising edge of LCLK comes in the middle of the data window			X									1					

The output interface of CDK8307 is normally a DDR interface, with the LCLK rising and falling edge transitions in the middle of alternate data windows. The phase for LCLK can be programmed relative to the output frame clock and data using bits *phase_ddr<1:0>.* The LCLK phase modes are shown in Figure 6. The default timing is identical to setting *phase_ddr<1:0>* = '10'.

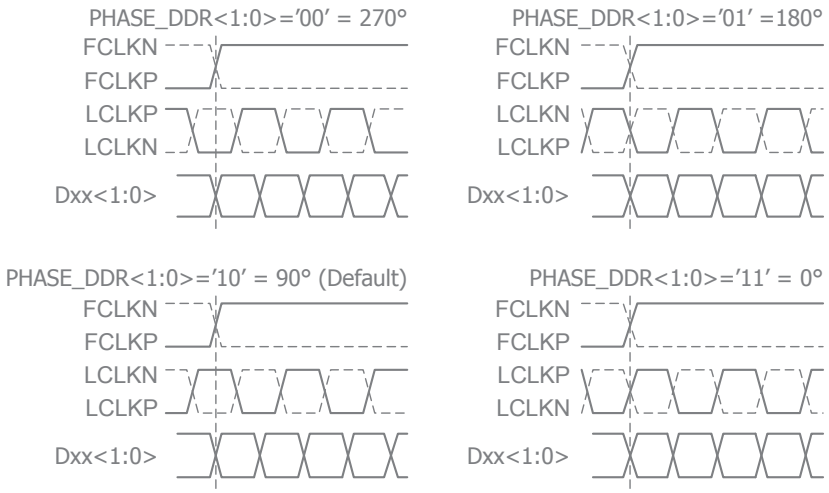


Figure 6. Phase Programmability Modes for LCLK

The device can also be made to operate in SDR mode by setting the *en_sdr* bit to '1'. The bit clock (LCLK) is output at 12x times the input clock in this mode, two times the rate in DDR mode. Depending on the state of *fall_sdr,* LCLK may be output in either of the two manners shown in Figure 7. As can be seen in Figure 7, only the LCLK rising (or falling) edge is used to capture the output data in SDR mode. The SDR mode is not recommended beyond 40MSPS because the LCLK frequency becomes very high.

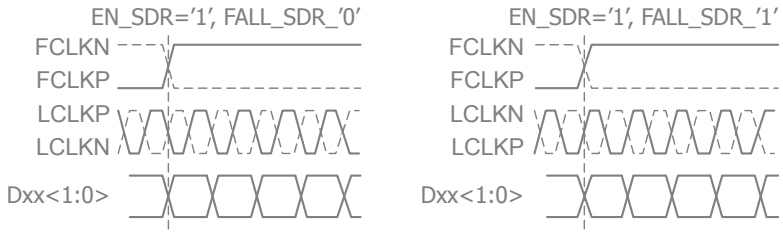


Figure 7. SDR Interface Modes

The default data output format is offset binary. Two's complement mode can be selected by setting the *btc_mode* bit to '1' which inverts the MSB.

The first bit of the frame (following the rising edge of FCLKP) is the LSB of the ADC output for default settings. Programming the *msb_first* mode results in reverse bit order, and the MSB is output as the first bit following the FCLKP rising edge.

Table 14. Number of Serial Output Bits

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
lvds_num_bits	Sets the number if LVDS output bits	12-bit															X		53
lvds_advance	Advance LVDS data bits and frame clock by one clock cycle	Inactive											0	X					
lvds_delay	Delay LVDS data bits and frame clock by one clock cycle	Inactive											X	0					

The ADC channels have 13 bits of resolution. There are two options for the serial LVDS outputs, 12 bits or 14 bits, selected by setting *lvds_num_bits* to '0' or '1', respectively. In 12-bit mode, the LSB bit from the ADCs are removed in the output stream. In 14-bit mode, a '0' is added in the LSB position. Power down mode must be activated after or during a change in the number of output bits.

To ease timing in the receiver when using multiple ADC chips, the CDK8307 has the option to adjust the timing of the output data and the frame clock. The propagation delay with respect to the ADC input clock can be moved one LVDS clock cycle forward or backward, by using *lvds_advance* and *lvds_delay*, respectively. See figure 8 for details. Note that LCLK is not affected by *lvds_delay* or *lvds_advance* settings.

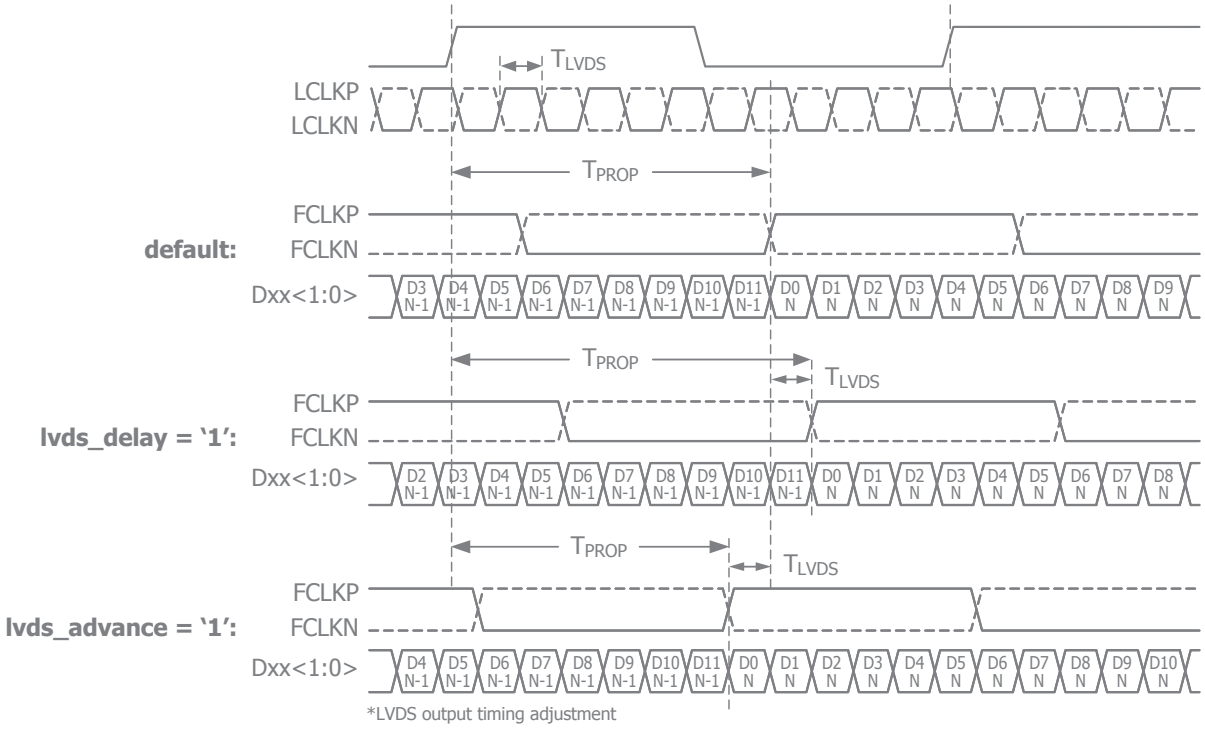


Figure 8: LVDS Output Timing Adjustment

Table 15. Full Scale Control

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
fs_cntrl<5:0>	Fine adjust ADC full scale range	0% change											X	X	X	X	X	X	55

The full-scale voltage range of CDK8307 can be adjusted using an internal 6-bit DAC controlled by the *fs_cntrl* register. Changing the value in the register by one step, adjusts the full-scale range approximately 0.3%. This leads to a maximum range of ±10% adjustment. Table 16 shows how the register settings correspond to the full-scale range. Note that the values for full-scale range adjustment are approximate. The DAC is, however, guaranteed to be monotonous.

The full-scale control and the programmable gain features differ in two major ways:

1. The full-scale control feature controls the full-scale voltage range in an analog fashion, whereas the programmable gain is a digital feature.
2. The programmable gain feature has much coarser gain steps and larger range than the full-scale control.

Table 16. Register Values with Corresponding Change in Full-Scale Range

fs_cntrl <5:0>	Full-Scale Range Adjustment
111111	+9.7%
...	...
100001	+0.3%
100000	+0%
011111	-0.3%
...	...
000000	-10%

Table 17. Clock Frequency

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
clk_freq<1:0>	Input clock frequency	50 - 80MHz															X	X	56

To optimize startup time a register is provided where the input clock frequency can be set. Some internal circuitry has startup times that are frequency independent. Default counter values are set to accommodate these startup times at the maximum clock frequency. This will lead to increased startup times at low clock frequency. Setting the value of this register to the nearest higher clock frequency will reduce the count values of the internal counters, to better fit the actual startup time, such that the startup time will be reduced. The start up times from Power Down mode and Deep Sleep mode are changed by this register setting.

Table 18. Clock Frequency Settings

clk_freq <1:0>	Clock Frequency (MHz)	Startup Delay (clock cycles)	Startup Delay (µs)
00	50 - 80	992	12.4 - 19.8
01	32.5 - 50	640	12.8 - 19.7
10	20 - 32.5	420	12.9 - 21
11	15 - 20	260	13 - 17.3

Table 19. Performance Control

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
perfm_ cntrl<2:0>	ADC performance control	Nominal														X	X	X	50
ext_vcm_ bc<1:0>	VCM buffer driving strength control	Nominal											X	X					

There are two registers that impact performance and power dissipation.

The *perfm_cntrl* register adjusts the performance level of the ADC core. If full performance is required, the nominal setting must be used. The lowest code can be used in situations where power dissipation is critical and performance is less important. For most conditions the performance at the minimum setting will be similar to nominal setting. However, only 10-bit performance can be expected at worst case conditions. The power dissipation savings shown in Table 20 are only approximate numbers for the ADC current alone.

Table 20. Performance Control Settings

performance_control <2:0>	Power Dissipation
100	-40% (lower performance)
101	-30%
110	-20%
111	-10%
000 (default)	Nominal
001	Do not use
010	Do not use
011	Do not use

The *ext_vcm_bc* register controls the driving strength in the buffer supplying the voltage on the VCM pin. If this pin is not in use, the buffer can be switched off. If current is drawn from the VCM pin, the driving strength can be increased to keep the voltage on this pin at the correct level.

Table 21. External Common Mode Voltage Buffer Driving Strength

ext_vcm_bc <1:0>	VCM Buffer Driving Strength
00	Off (VCM floating)
01 (default)	Low
10	High
11	Max

Therory of Operation

The CDK8307 is an 8-channel, high-speed, CMOS ADC. The 13-bits given out by each channel are serialized to 12, 13 or 14-bits and sent out on a single pair of pins in LVDS format. All eight channels of the CDK8307 operate from a single differential or single ended clock. The sampling clocks for each of the eight channels are generated from the clock input using a carefully matched clock buffer tree. The 12x/13x/14x clock required for the serializer is generated internally from FCLK using a phase-locked loop (PLL). A 6x/6.5x/7x and 1x clock are also output in LVDS format, along with the data to enable easy data capture. The CDK8307 uses internally generated references that can be shorted across several devices to improve gain-matching. The differential reference value is 1V. This results in a differential input of -1V to correspond to the zero code of the ADC, and a differential input of +1V to correspond to the full-scale code (code 8191).

The ADC employs a pipelined converter architecture. Each stage feeds its output data into the digital error correction logic, ensuring excellent differential linearity and no missing codes at 13-bit level.

The CDK8307 operates from two sets of supplies and grounds. The analog supply and ground set is identified as AVDD and AVSS, while the digital set is identified by DVDD and DVSS.

Recommended Usage

Analog Input

The analog input to the CDK8307 is a switched capacitor track-and-hold amplifier optimized for differential operation. Operation at common mode voltages at mid supply is recommended even if performance will be good for the ranges specified. The VCM pin provides a voltage suitable as common mode voltage reference. The internal buffer for the VCM voltage can be switched off, and driving capabilities can be changed programming the ext_vcm_bc<1:0> register.

Figure 9 shows a simplified drawing of the input network. The signal source must have sufficiently low output impedance to charge the sampling capacitors within one clock cycle. A small external resistor (e.g. 22Ω) in series with each input is recommended as it helps reducing transient currents and dampens ringing behavior. A small differential shunt capacitor at the chip side of the resistors may be used to provide dynamic charging currents and may improve performance. The resistors form a low pass filter with the capacitor, and values must therefore be determined by requirements for the application.

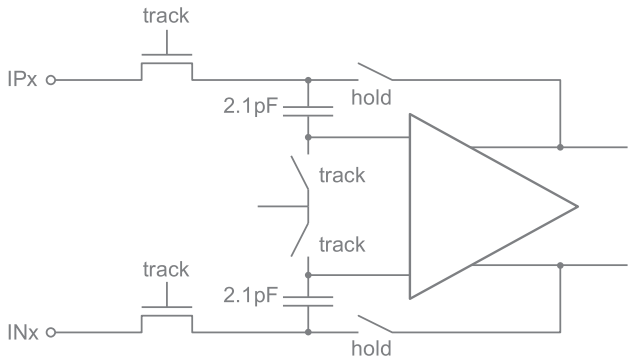


Figure 9. Input Configuration Diagram

DC-Coupling

Figure 10 shows a recommended configuration for DC-coupling. Note that the common mode input voltage must be controlled according to specified values. Preferably, the CM_EXT output should be used as a reference to set the common mode voltage.

The input amplifier could be inside a companion chip or it could be a dedicated amplifier. Several suitable single ended to differential driver amplifiers exist in the market. The system designer should make sure the specifications of the selected amplifier is adequate for the total system, and that driving capabilities comply with the CDK8307 input specifications.

Detailed configuration and usage instructions must be found in the documentation of the selected driver, and the values given in Figure 10 must be varied according to the recommendations for the driver.

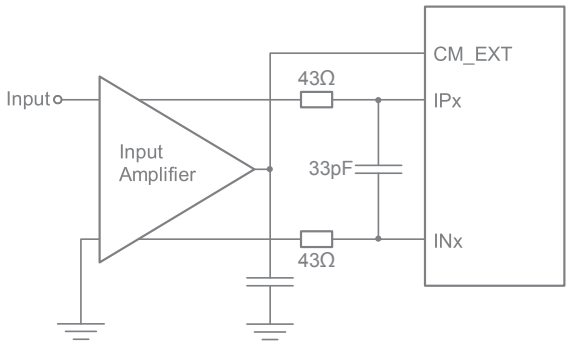


Figure 10. DC-Coupled Input

AC-Coupling

A signal transformer or series capacitors can be used to make an AC-coupled input network. Figure 11 shows a recommended configuration using a transformer. Make sure that a transformer with sufficient linearity is selected, and that the bandwidth of the transformer is appropriate. The bandwidth should exceed the sampling rate of the ADC with at least a factor of 10. It is also important to keep phase mismatch between the differential ADC inputs small for good HD2 performance. This type of transformer coupled input is the preferred configuration for high frequency signals as most differential amplifiers do not have adequate performance at high frequencies. Magnetic coupling between the transformers and PCB traces may impact channel crosstalk, and must hence be taken into account during PCB layout.

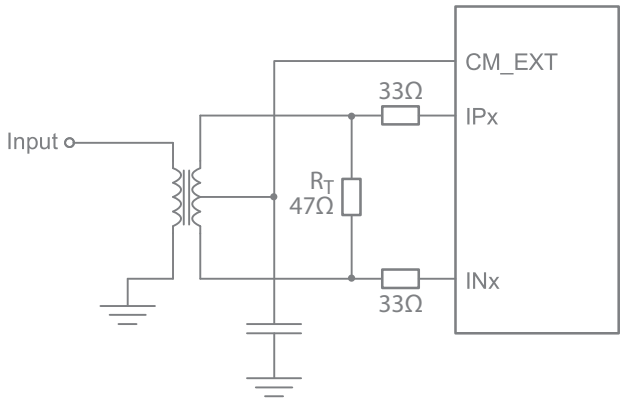


Figure 11. Transformer Coupled Input

If the input signal is traveling a long physical distance from the signal source to the transformer (for example a long cable), kick-backs from the ADC will also travel along this distance. If these kick-backs are not terminated properly at the source side, they are reflected and will add to the input signal at the ADC input. This could reduce the ADC performance. To avoid this effect, the source must effectively terminate the ADC kick-backs, or the traveling distance should be very short. If this problem could not be avoided, the circuit in Figure 10 can be used.

Figure 12 shows AC-coupling using capacitors. Resistors from the CM_EXT output, RCM, should be used to bias the differential input signals to the correct voltage. The series capacitor, CI, form the high-pass pole with these resistors, and the values must therefore be determined based on the requirement to the high-pass cut-off frequency.

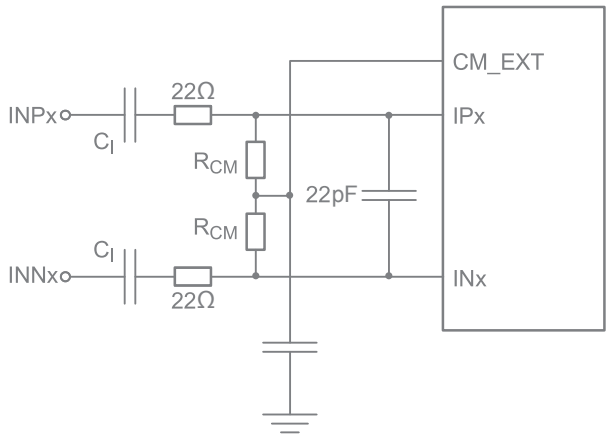


Figure 12. AC-Coupled Input

Note that startup time from Sleep Mode and Power Down Mode will be affected by this filter as the time required to charge the series capacitors is dependent on the filter cut-off frequency.

If the input signal has a long traveling distance, and the kick-backs from the ADC not are effectively terminated at the signal source, the input network of Figure 13 can be used. The configuration is designed to attenuate the kickback from the ADC and to provide an input impedance that looks as resistive as possible for frequencies below Nyquist.

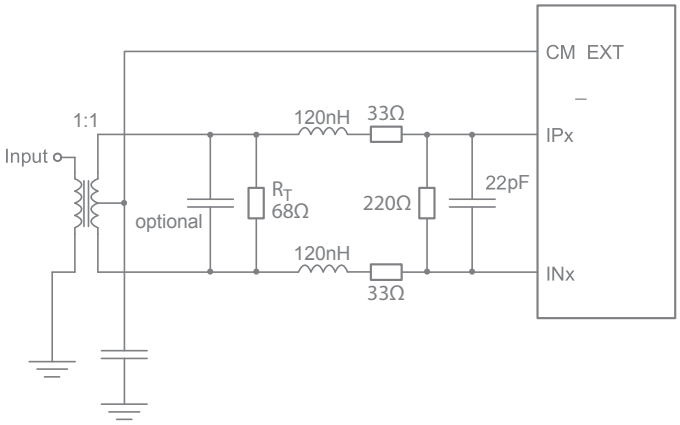


Figure 13: Alternative Input Network

Values of the series inductor will however depend on board design and conversion rate. In some instances a shunt capacitor in parallel with the termination resistor (e.g. 33pF) may improve ADC performance further. This capacitor attenuate the ADC kick-back even more, and minimize the kicks traveling towards the source. However the impedance match seen into the transformer becomes worse.

Clock Input and Jitter Considerations

Typically high-speed ADCs use both clock edges to generate internal timing signals. In the CDK8307 only the rising edge of the clock is used. Hence, input clock duty cycles between 20% and 80% is acceptable.

The input clock can be supplied in a variety of formats. The clock pins are AC-coupled internally, and hence a wide common mode voltage range is accepted. Differential clock sources as LVDS, LVPECL or differential sine wave can be connected directly to the input pins. For CMOS inputs, the CLKN pin should be connected to ground, and the CMOS clock signal should be connected to CLKP. For differential sine wave clock input the amplitude must be at least $\pm 0.8V_{pp}$.

The quality of the input clock is extremely important for high-speed, high-resolution ADCs. The contribution to SNR from clock jitter with a full scale signal at a given frequency is shown in equation below.

$$SNR_{jitter} = 20 \cdot \log (2 \cdot \pi \cdot F_{IN} \cdot \varepsilon_t)$$

where F_{IN} is the signal frequency, and ε_t is the total rms jitter measured in seconds. The rms jitter is the total of all jitter sources including the clock generation circuitry, clock distribution and internal ADC circuitry.

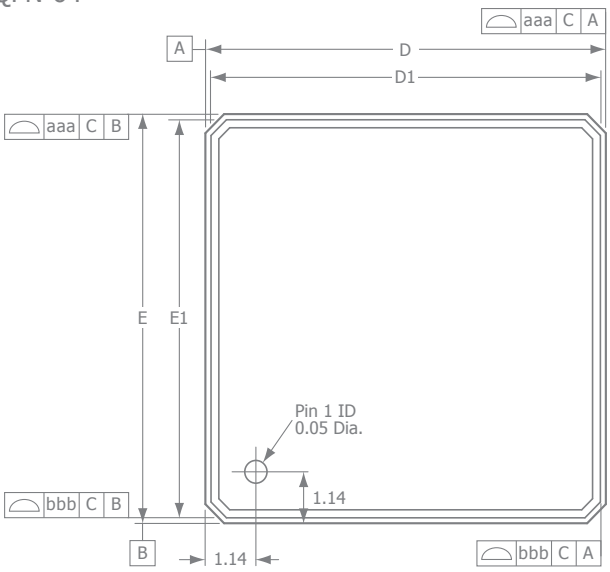
For applications where jitter may limit the obtainable performance, it is of utmost importance to limit the clock jitter. This can be obtained by using precise and stable clock references (e.g. crystal oscillators with good jitter specifications) and make sure the clock distribution is well controlled. It might be advantageous to use analog power and ground planes to ensure low noise on the supplies to all circuitry in the clock distribution. It is of utmost importance to avoid crosstalk between the ADC output bits and the clock and between the analog input signal and the clock since such crosstalk often results in harmonic distortion.

The jitter performance is improved with reduced rise and fall times of the input clock. Hence, optimum jitter performance is obtained with LVDS or LVPECL clock with fast edges. CMOS and sine wave clock inputs will result in slightly degraded jitter performance.

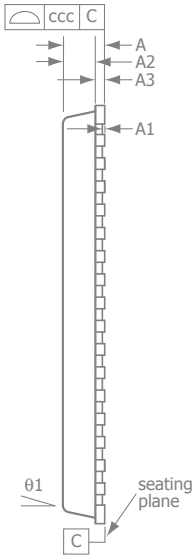
If the clock is generated by other circuitry, it should be retimed with a low jitter master clock as the last operation before it is applied to the ADC clock input.

Mechanical Dimensions

QFN-64



TOP VIEW

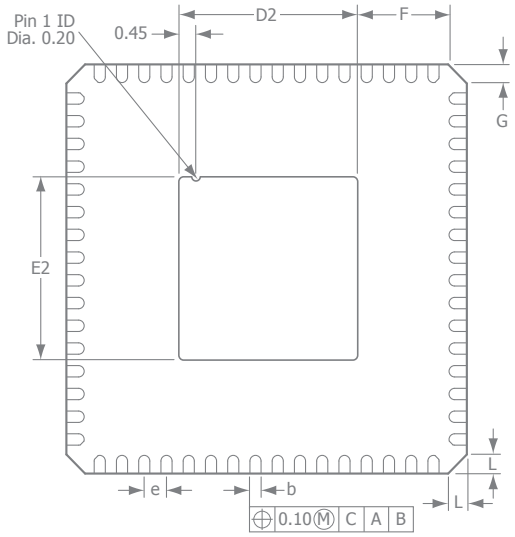


SIDE VIEW

	Inches			Millimeters		
Symbol	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
A	–	–	0.035	–	–	0.9
A_1	0.00	0.0004	0.002	0.00	0.01	0.05
A_2	–	0.026	0.028	–	0.65	0.7
A_3		0.008 REF			0.2 REF	
b	0.008	0.010	0.012	0.2	0.25	0.30
D		0.354 BSC			9.00 BSC	
D_1		0.354 BSC			8.75 BSC	
D_2	0.197	0.205	0.213	5.0	5.2	5.4
E		0.354 BSC			9.00 BSC	
E_1		0.344 BSC			8.75 BSC	
E_2	0.197	0.205	0.213	5.0	5.2	5.4
F	0.05	–	–	1.3	–	–
G	0.0096	0.0168	0.024	0.24	0.42	0.6
L	0.012	0.016	0.020	0.3	0.4	0.5
e		0.020 BSC			0.50 BSC	
θ_1	0°	–	12°	0°	–	12°
Tolerance of Form and Position						
aaa		0.10			0.004	
bbb		0.10			0.004	
ccc		0.05			0.002	

NOTES:

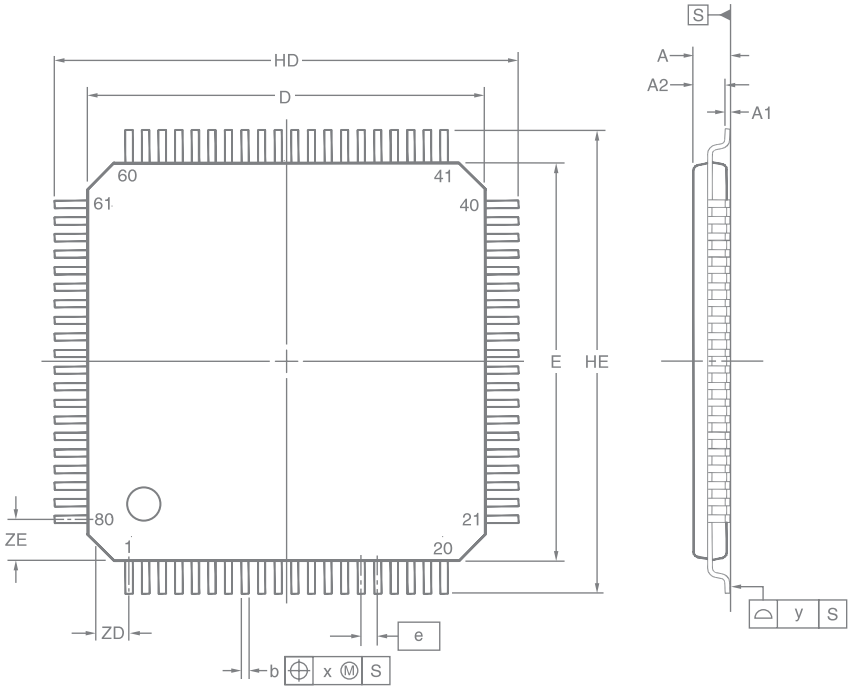
1. All dimensions are in millimeters.
2. Die thickness allowable is 0.305mm maximum (.012 inches maximum)
3. Dimensioning & tolerances conform to ASME y14.5m. -1994.
4. Dimension applies to plated terminal and is measured between 0.20 and 0.25mm from terminal tip.
5. The pin #1 identifier must be placed on the top surface of the package by using indentation mark or other feature of package body.
6. Exact shape and size of this feature is optional.
7. Package warpage max 0.08mm.
8. Applied for exposed pad and terminals. Exclude embedding part of exposed pad from measuring.
9. Applied only to terminals.
10. Package corners unless otherwise specipied are r0.175±0.025mm.



BOTTOM VIEW

Mechanical Dimensions *(Continued)*

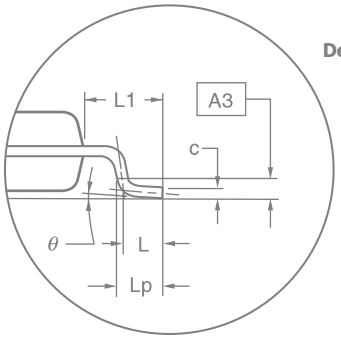
TQFP-80



TQFP-80	
Symbol	**Dimensions (mm)**
A	1.20
A_1	0.10 ±0.05
A_2	1.00 ±0.05
A_3	0.25
b	0.22 ±0.05
c	0.145 +0.055 0.145 -0.045
D	12.00 ±0.20
E	12.00 ±0.20
e	0.50
HD	14.00 ±0.20
HE	14.00 ±0.20
L	0.50
Lp	0.60 ±0.15
L_1	1.00 ±0.20
x	0.08
y	0.08
ZD	1.25
ZE	1.25
θ	3° +5° 3° -3°

NOTE:
Each lead centerline is located within 0.08mm of its true position at maximum material condition.

Detail of Lead End



For Further Assistance:

Exar Corporation Headquarters and Sales Offices
48720 Kato Road
Fremont, CA 94538 - USA

Tel.: +1 (510) 668-7000
Fax: +1 (510) 668-7001
www.exar.com

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