LDO Regulators with Voltage Detector

500 mA Output LDO Regulator with Voltage Detector

BD4275FP2-C BD4275FPJ-C

General Description

BD4275FP2-C and BD4275FPJ-C are automotive suited voltage regulator with 1ch Reset and offers the output current of 500mA while limiting the low quiescent current. These regulators are therefore ideal for applications requiring a direct connection to the battery and a low current consumption. A reset signal is generated for an output voltage VO of Typ 4.62 V.
The reset delay time can be programmed by the external capacitor.

Features

- AEC-Q100 qualified. (1)
- Low ESR ceramic capacitors applicable for output.
- Low drop voltage: PDMOS output transistor
- Power on and under-voltage reset
- Programmable reset delay time by external capacitor.

(1): Grade 1

Applications

- Onboard vehicle device (body-control, car stereos, satellite navigation system, etc)

Key Specifications

- Qualified for Automotive Applications
- Input Voltage Range: -0.3 V to +45 V
- Low Quiescent Current: 65 µA (Typ)
- Output Load Current: 500 mA
- Output Voltage: 5.0 V ±2 %
- Reset Detect Voltage : 4.50 V to 4.75 V
- Over Current Protection (OCP)
- Thermal Shut Down (TSD)

Package

W (Typ) × D (Typ) × H (Max)

- FP2: TO263-5F 10.16 mm × 15.10 mm × 4.70 mm

- FPJ: TO252-J5F 6.60 mm × 10.10 mm × 2.38 mm

Figure 1. Package Outlook

Typical Application Circuit

- VCC and VO pin capacitors: 0.1 µF ≤ C_{IN} (Typ), 6 µF ≤ C_O (Min)
  Please refer to the "Selection of Components Externally Connected".

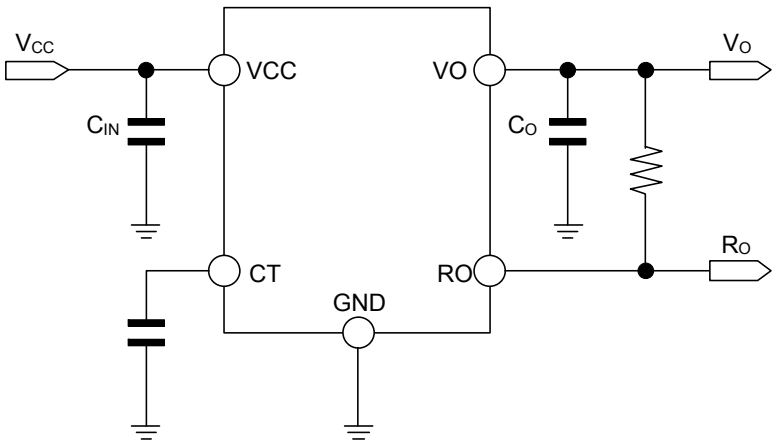


Figure 2. Typical Application Circuit

Pin Configurations

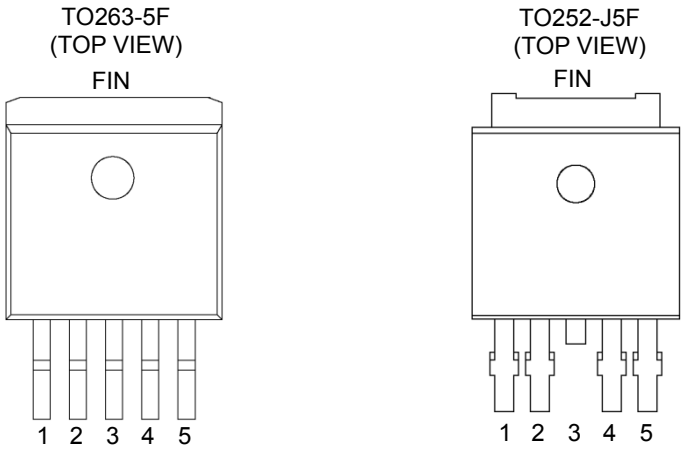


Figure 3. Pin configurations

Pin Descriptions

Pin No.	Pin Name	Function
1	VCC	Supply Voltage Input
2	RO	Reset Output; Open-Collector output.
3	GND	Ground; Pin3 internally connected to FIN.
4	CT	Reset Delay; connect capacitor to GND for setting delay time.
5	VO	5 V Output;
FIN	FIN	FIN; FIN internally connected to Pin3.

Block Diagram

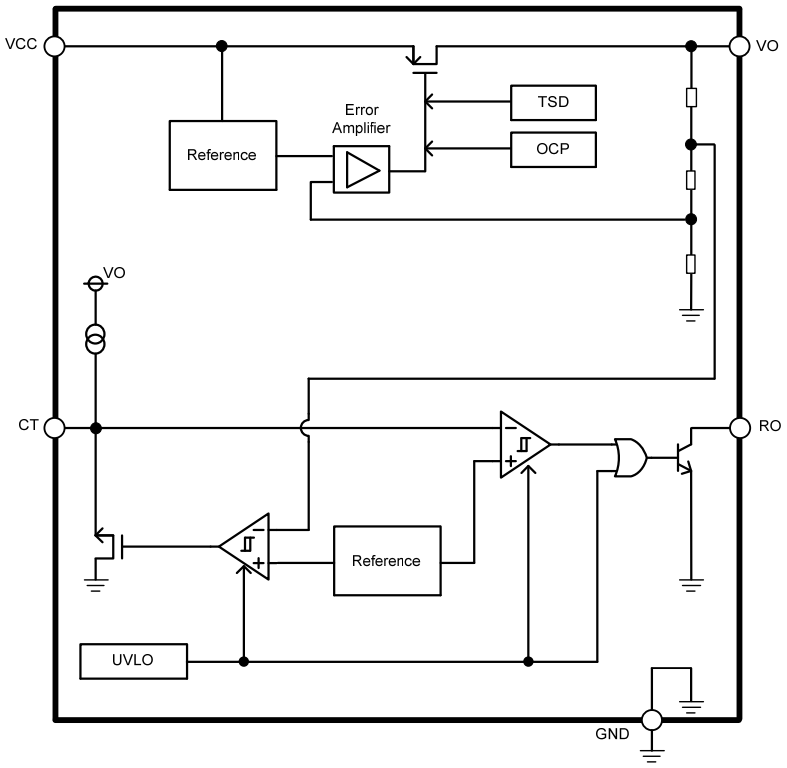


Figure 4. Block Diagram

Block Descriptions

Block Name	Function	Description of Blocks
Reference	Reference voltage	The Reference generates the Reference Voltage.
Error Amplifier	Error amplifier	The Error Amplifier amplifies the difference between the feed back voltage of the output voltage and the reference voltage.
TSD	Thermal shutdown protection	The TSD protects the device from overheating. If the chip temperature (Tj) reaches ca. 175 °C (Typ), the output is turned off.
OCP	Over current protection	The OCP protects the device from damage caused by over current.
UVLO	Under voltage lock out	The UVLO prevents malfunction of the reset block in case of very low output voltage.

Absolute Maximum Ratings

Parameter		Symbol	Limits	Unit
VCC Voltage (1)		V_{CC}	-0.3 to +45.0	V
RO Voltage		V_{RO}	-0.3 to +18.0	V
VO Voltage		V_O	-0.3 to +7.0	V
Power Dissipation	(TO263-5F) (2)	Pd	1.9	W
	(TO252-J5F) (3)	Pd	1.3	W
Junction Temperature Range		Tj	-40 to +150	°C
Storage Temperature Range		Tstg	-55 to +150	°C

(1) Not to exceed Pd.

(2) Reduced by 15.2 mW / °C over Ta = 25 °C, when mounted on glass epoxy board: 114.3 mm × 76.2 mm × 1.6 mm.

(3) Reduced by 10.4 mW / °C over Ta = 25 °C, when mounted on glass epoxy board: 114.3 mm × 76.2 mm × 1.6 mm.

Recommended Operating Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage ($I_O \leq 300mA$) (1)	V_{CC}	5.5	45.0	V
Supply Voltage ($I_O \leq 500mA$) (1)	V_{CC}	5.9	45.0	V
Start -Up Voltage	V_{CC}	3.0	—	V
Output Current	I_O	0	500	mA
Operating Ratings Temperature	Ta	-40	125	°C

(1) Not to exceed Pd.

Thermal Resistance

Parameter	Symbol	Min	Max	Unit
TO263-5F Package				
Junction to Ambient (1)	θja	15.6	—	°C / W
Junction to Case (bottom) (1)	θjc	1	—	°C / W
TO252-J5F Package				
Junction to Ambient (2)	θja	19.2	—	°C / W
Junction to Case (bottom) (2)	θjc	1	—	°C / W

(1) TO263-5F mounted on 114.3 mm × 76.2 mm × 1.6 mmt 4-Layer Glass-Epoxy PCB.
(Top copper foil: ROHM recommended footprint + wiring to measure /
Copper foil on 2 inner layers and the reverse side of PCB:74.2 mm × 74.2 mm)

(2) TO252-J5F mounted on 114.3 mm × 76.2 mm × 1.6 mmt 4-Layer Glass-Epoxy PCB.
(Top copper foil: ROHM recommended footprint + wiring to measure /
Copper foil on 2 inner layers and the reverse side of PCB:74.2 mm × 74.2 mm)

Electrical Characteristics

(Unless otherwise specified , Tj = -40 °C to +150 °C, V_{CC} = 13.5 V)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Circuit Current	I_{CC}	—	65	150	μA	I_O = 0 mA
Output Voltage 1	V_O	4.90	5.00	5.10	V	5 mA ≤ I_O ≤ 400 mA 6 V ≤ V_{CC} ≤ 28 V
Output Voltage 2	V_O	4.90	5.00	5.10	V	5 mA ≤ I_O ≤ 200 mA 6 V ≤ V_{CC} ≤ 40 V
Dropout Voltage	ΔVd	—	0.25	0.5	V	V_{CC} = 4.75 V, I_O = 300 mA
Load Regulation	Reg.L	—	10	30	mV	I_O = 10 mA to 250 mA
Line Regulation	Reg.I	-15	—	15	mV	V_{CC} = 8 V to 16 V, I_O = 5 mA
Current Limit	I_{OCP}	500	—	—	mA	—
Ripple Rejection	R.R.	—	60	—	dB	f = 120 Hz, ein = 1 Vrms, I_O = 100 mA
Thermal Shut Down Temperature	T_{TSD}	—	175	—	°C	

Electrical Characteristics (Reset Function)

(Unless otherwise specified , Tj = -40 °C to +150 °C, V_{CC} = 13.5 V)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Switching Threshold	V_{RT}	4.50	4.62	4.75	V	—
Switching Hysteresis	V_{RHY}	20	60	100	mV	—
Upper Delay Switching Threshold	V_{CTH}	—	1.18	—	V	—
Lower Delay Switching Threshold	V_{CTL}	—	0.25	—	V	—
Charge Current	I_{CT}	—	8.8	—	μA	V_{CT} = 0.5 V
Delay time L→H	T_{POR}	10	14	18	ms	C_{CT} = 0.1 μF (1)
RO L Voltage	V_{ROL}	—	—	0.4	V	RO pull-up resister ≥ 4.7 kΩ V_O ≥1V

(1) T_{POR} can be varied by changing the CT capacitance value. (0.001μF to 10 μF available)

T_{POR} (ms) ≈ T_{POR0} (the reset delay time at C_{CT} = 0.1 μF) × C_{CT} (μF) / 0.1 CT capacitor : 0.1μF ≤ C_{CT} ≤ 10 μF
example: When C_{CT}= 1μF, 100ms ≤ T_{POR} ≤ 180 ms

T_{POR} (ms) ≈ T_{POR0} (the reset delay time at C_{CT} = 0.1 μF) × C_{CT} (μF) / 0.1 ±0.1 CT capacitor : 0.001μF ≤ C_{CT} < 0.1 μF
example: When C_{CT}= 0.01μF, 0.9ms ≤ T_{POR} ≤ 1.9 ms

Typical Performance Curves (Unless otherwise specified , Tj = 25 °C, V_{CC} = 13.5 V)

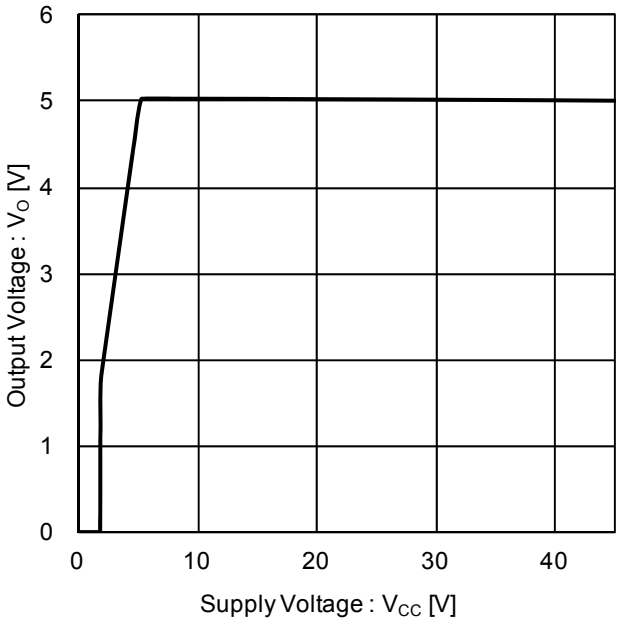


Figure 5. Output Voltage vs Supply Voltage
(R_L = 25 Ω)

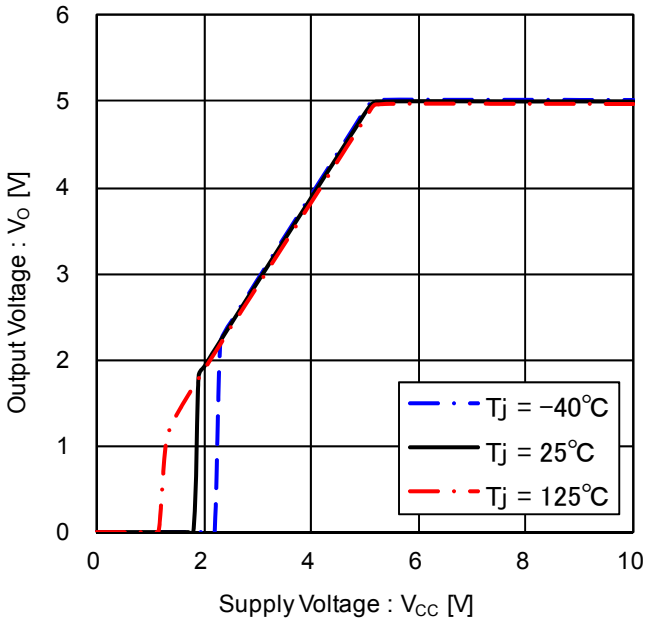


Figure 6. Output Voltage vs Supply Voltage
(at Low supply voltage, R_L = 25 Ω)

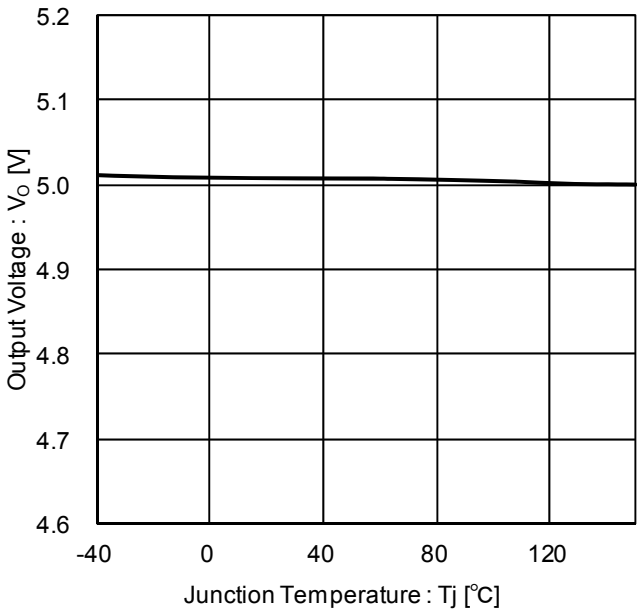


Figure 7. Output Voltage vs Temperature
(R_L = 1 kΩ)

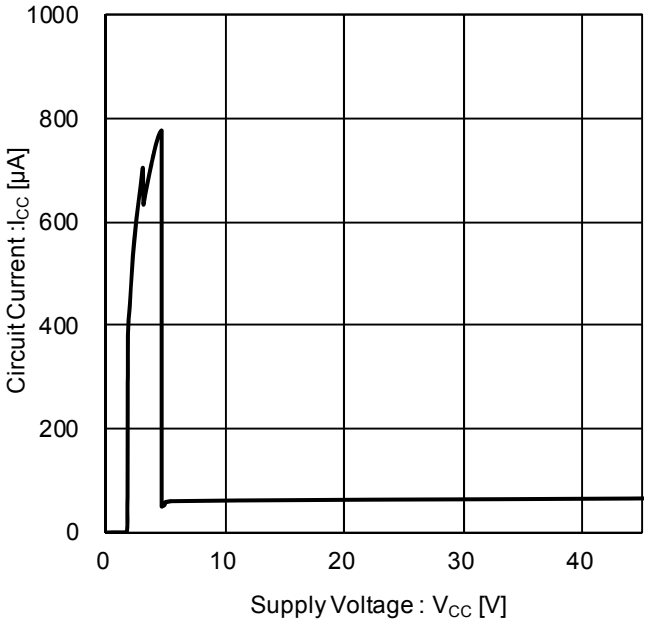


Figure 8. Circuit Current vs Supply voltage

Typical Performance Curves (Unless otherwise specified , Tj = 25 °C, V_{CC} = 13.5 V) -Continued

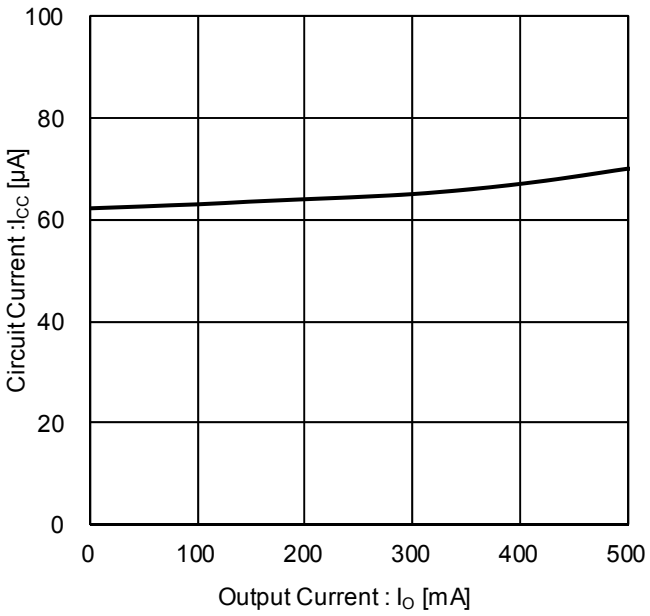


Figure 9. Circuit Current vs Output Current

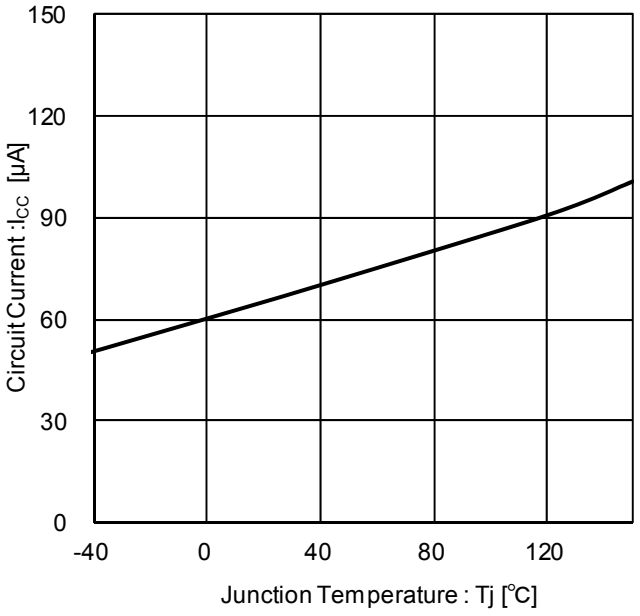


Figure 10. Circuit Current vs Temperature

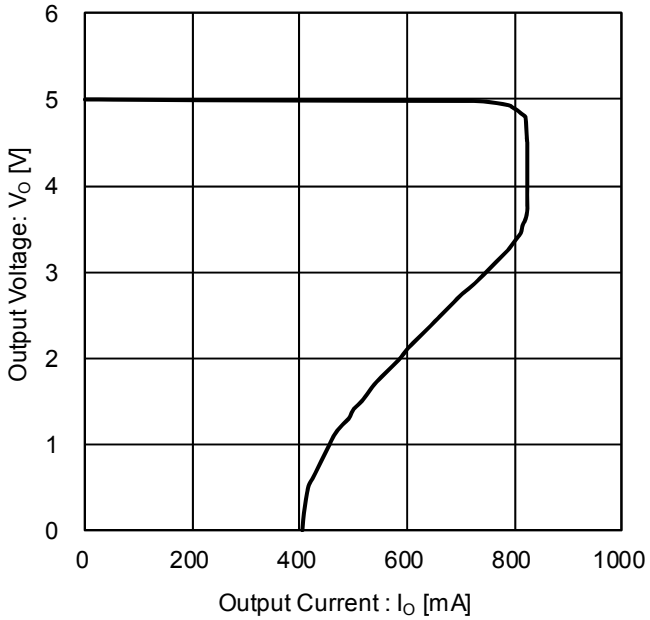


Figure 11. Output Voltage vs Output Current
(Over Current Protection)

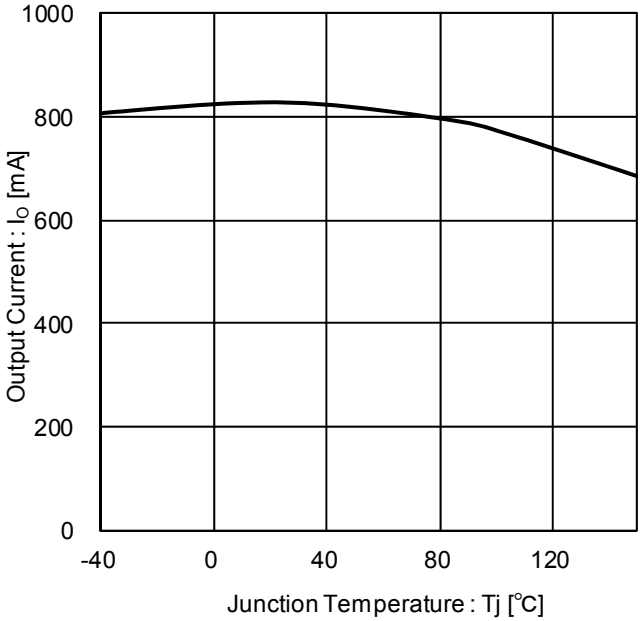


Figure 12. Output Current vs Temperature

Typical Performance Curves (Unless otherwise specified , Tj = 25 °C, V_{CC} = 13.5 V) -Continued

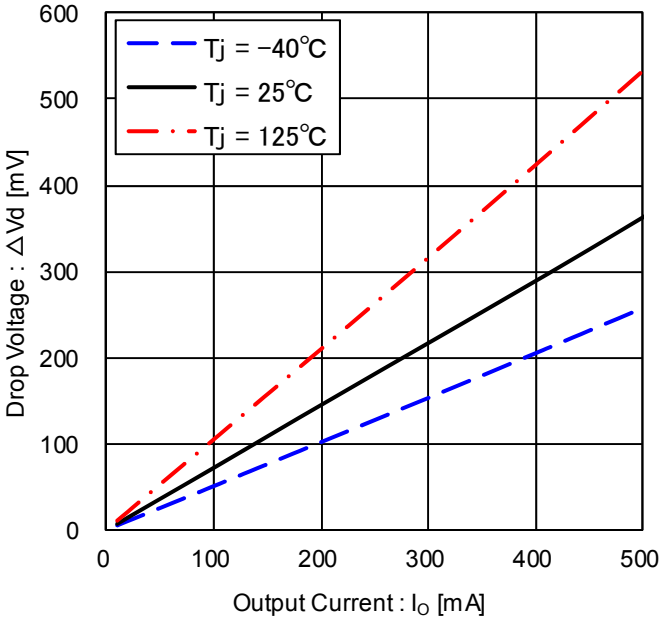


Figure 13. Drop voltage vs Output Current
(V_{CC} = 4.75 V)

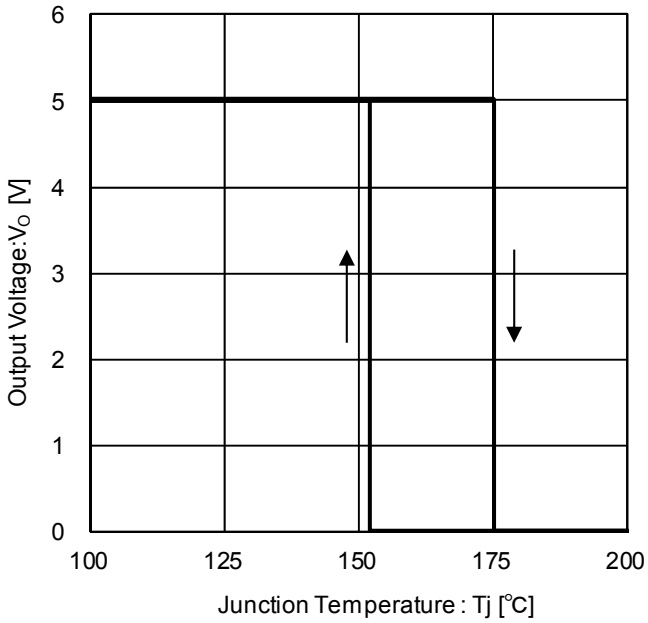


Figure 14. Output Voltage vs Temperature
(Thermal Shut Down)

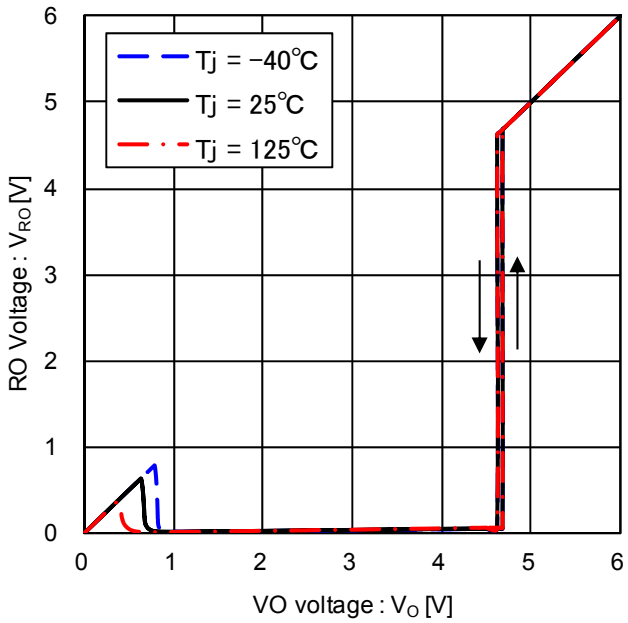


Figure 15. RO Voltage vs VO Voltage
(RO: 10 kΩ pull-up to VO)

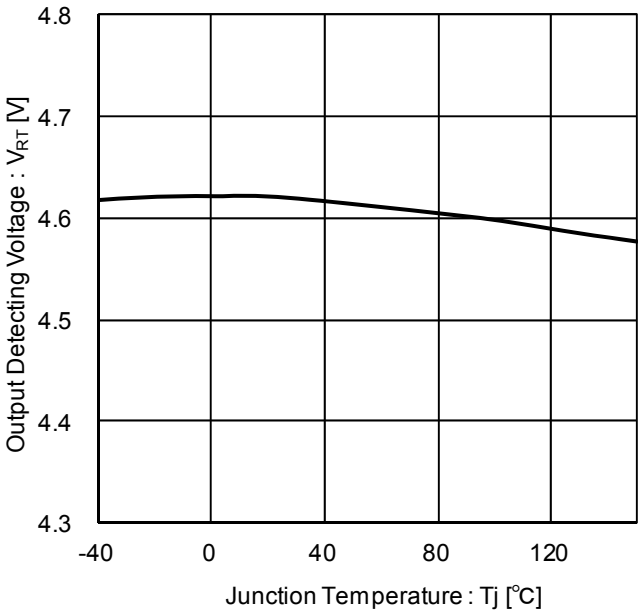


Figure 16. Output Detecting Voltage vs Temperature
(RO: 10 kΩ pull-up to VO)

Typical Performance Curves (Unless otherwise specified , Tj = 25 °C, V_{CC} = 13.5 V) -Continued

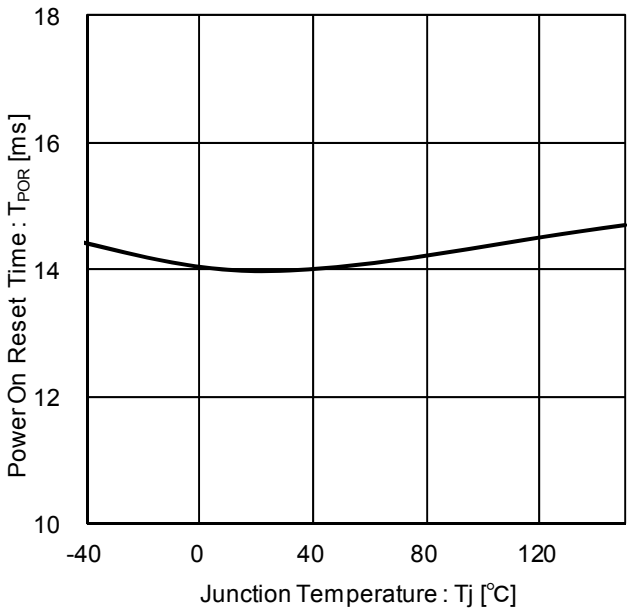


Figure 17. Power on Reset Time vs Temperature
(C_{CT} = 0.1 µF)

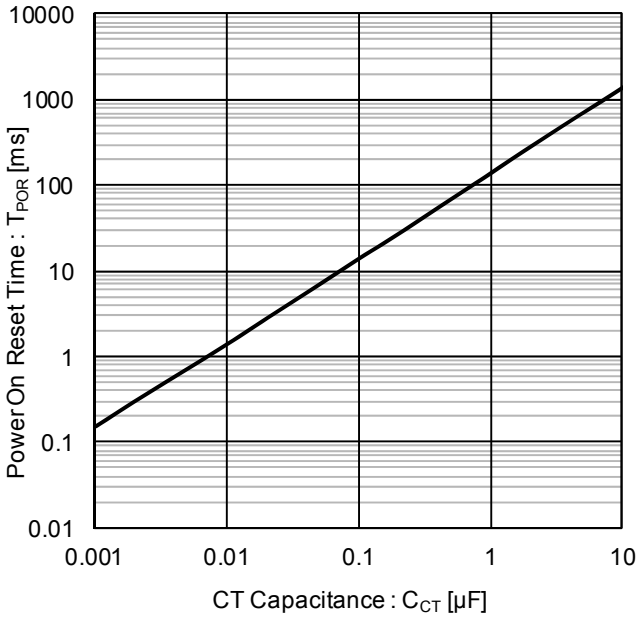
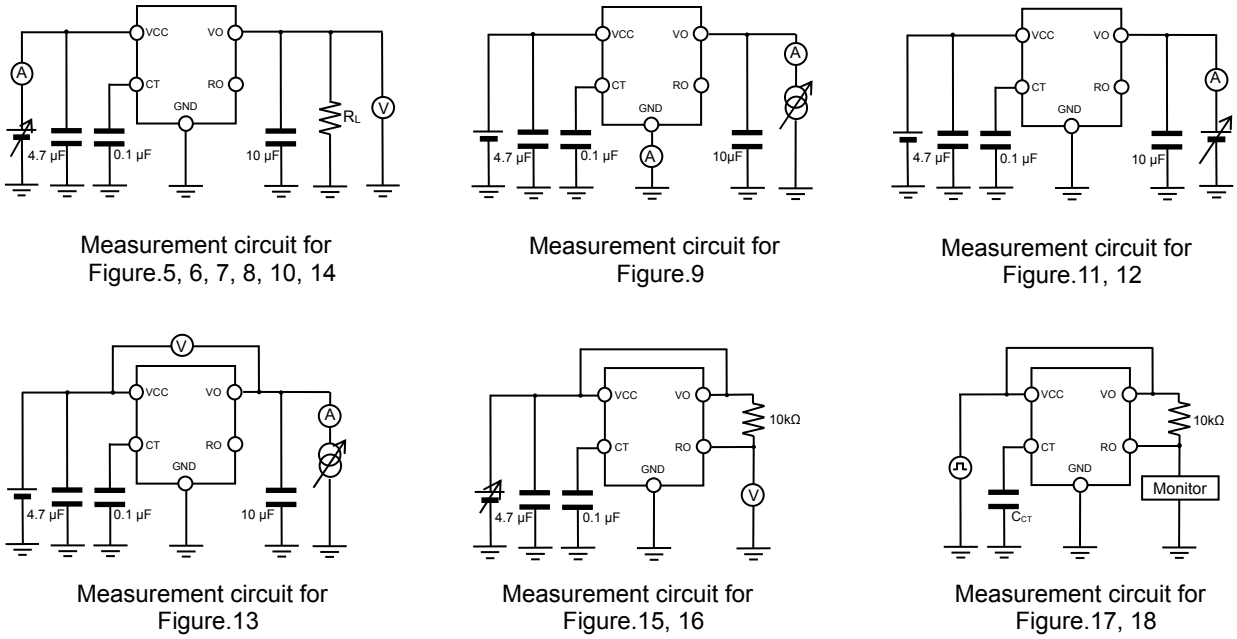


Figure 18. Power on Reset Time vs CT Capacitance

Measurement circuit for Typical Performance Curves



Measurement circuit for Figure.5, 6, 7, 8, 10, 14

Measurement circuit for Figure.9

Measurement circuit for Figure.11, 12

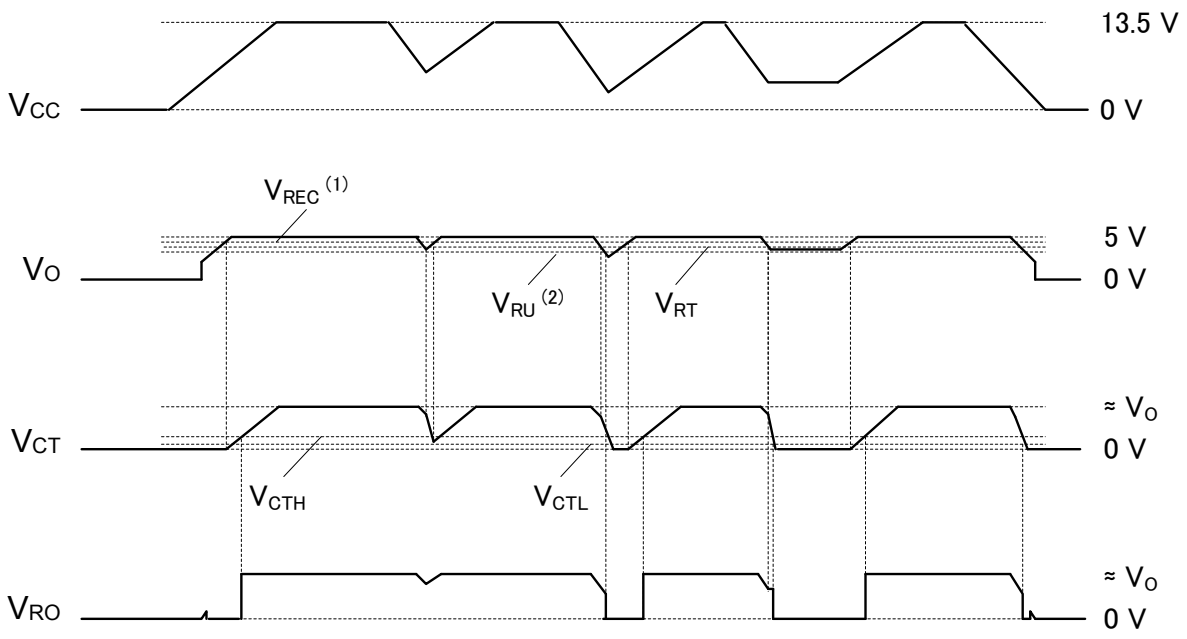
Measurement circuit for Figure.13

Measurement circuit for Figure.15, 16

Measurement circuit for Figure.17, 18

Figure 19. Measurement circuit for Typical Performance Curves

Timing Chart



(1) $V_{REC} = V_{RT} + V_{RHY}$
(2) V_{RU} = 2V to 3.5 V

Figure 20. Timing Chart

Power Dissipation

■TO263-5F

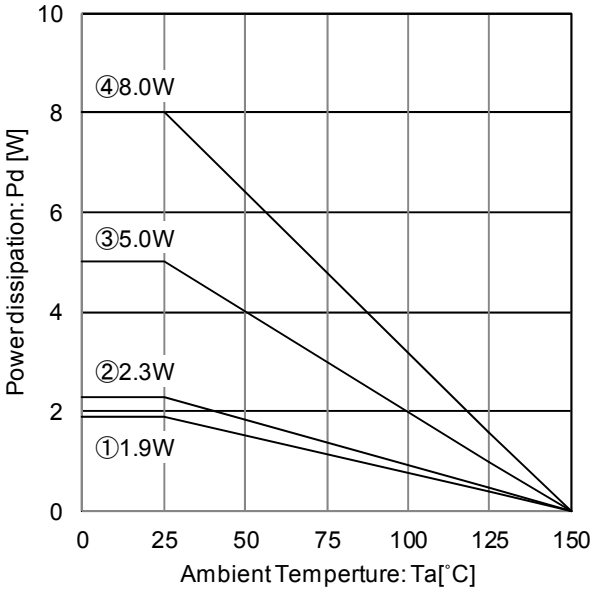


Figure 21. Package data of TO263-5F

IC mounted on ROHM standard board based on JEDEC.
Board material: FR4
Board size: 114.3 mm × 76.2 mm × 1.6 mmt
Top copper foil: The footprint ROHM recommend.
+ wiring to measure.

①: 1-layer PCB
(Copper foil area on the reverse side of PCB: 0 mm × 0 mm)
②: 2-layer PCB
(Copper foil area on the reverse side of PCB: 15.0mm × 15.0 mm)
③: 2-layer PCB
(Copper foil area on the reverse side of PCB: 74.2mm × 74.2 mm)
④: 4-layer PCB
(2inner layers and copper foil area on the reverse side of PCB: 74.2mm × 74.2 mm)

■TO252-J5F

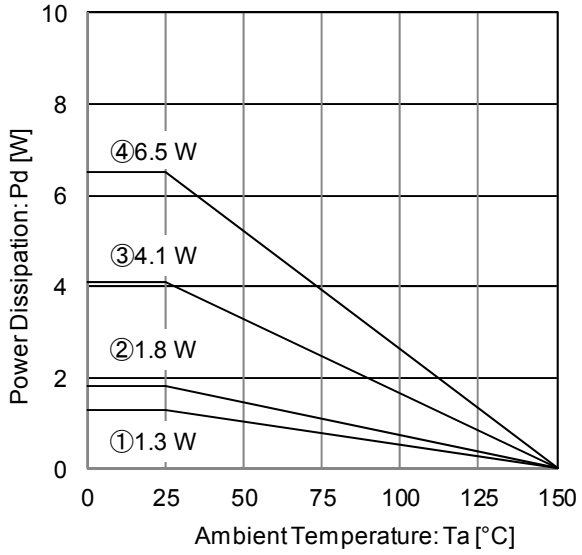


Figure 22. Package data of TO252-J5F

IC mounted on ROHM standard board based on JEDEC.
Board material: FR4
Board size: 114.3 mm × 76.2 mm × 1.6 mmt
Top copper foil: The footprint ROHM recommend.
+ wiring to measure.

①: 1-layer PCB
(Copper foil area on the reverse side of PCB: 0 mm × 0 mm)
②: 2-layer PCB
(Copper foil area on the reverse side of PCB: 15.0mm × 15.0 mm)
③: 2-layer PCB
(Copper foil area on the reverse side of PCB: 74.2mm × 74.2 mm)
④: 4-layer PCB
(2 inner layers and copper foil area on the reverse side of PCB: 74.2mm × 74.2 mm)

Thermal Design

Refer to the heat mitigation characteristics illustrated in Figure 21, 22 and the power dissipation under actual operating conditions should be taken into consideration and a sufficient margin should be allowed for in the thermal design. The amount of heat generated depends on the voltage difference across the input and output, load current, and bias current. Therefore, when actually using the chip, ensure that the generated heat does not exceed the Pd rating. Even if the ambient temperature Ta is at 25 °C, it is possible that the junction temperature Tj reaches high temperatures. Keep the whole operating temperature range within Tj ≤ Tjmax.
Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 114.3mm × 76.2mm × 1.6mmt glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

V_{CC}	: Input Voltage	Ta	: Ambient Temperature
V_O	: Output Voltage	Tc	: Case Temperature
I_O	: Load Current	Tj	: Junction Temperature
I_{CC}	: Circuit Current	θjc	: Thermal Resistance (Junction to Case (bottom))
Pc	: Power Consumption		

The following method is used to calculate the power consumption Pc (W)

$$Pc = (V_{CC} - V_O) \times I_O + V_{CC} \times I_{CC}$$
Power dissipation Pd ≥ Pc

The load current I_O is obtained by operating the IC within the power dissipation range.

$$I_O \leq \frac{Pd - V_{CC} \times I_{CC}}{V_{CC} - V_O}$$ (Refer to Figure 10 for the I_{CC}.)

Thus, the maximum load current $I_O$max for the applied voltage V_{CC} can be calculated during the thermal design process.

The following method is also used to calculate the junction temperature Tj.

$$Tj = Pc \times \theta jc + Tc$$

■TO263-5F

・Calculation example : with TO263-5F package , Ta = 105 °C, V_{CC} = 13.5 V, V_O = 5.0 V, board ③ (Figure 21.)

$$I_O \leq \frac{1.8\ W - 13.5\ V \times 80\ \mu A}{13.5\ V - 5.0\ V}$$ (I_{CC} = 80 μA)

$I_O \leq$ 211 mA

Pd at over 25 °C is calculated by below.
Pd = (Pd at 25 °C) × (150 - Ta) / (150 - 25)
In case of board③ in Figure 21, Ta = 105 °C
Pd = 1.8 W

At Ta = 105 °C with Figure 21 ③ condition, the calculation shows that 211 mA of output current is possible at 8.5 V potential difference across input and output.

・Calculation example : with Tc (bottom) = 80 °C, V_{CC} = 13.5 V, V_O = 5.0 V, I_O = 200 mA, board ③ (Figure 21.)

Pc of the IC can be calculated as follows:

$$Pc = (V_{CC} - V_O) \times I_O + V_{CC} \times I_{CC}$$
$$Pc = (13.5\ V - 5.0\ V) \times 200\ mA + 13.5\ V \times I_{CC}$$
Pc = 1.7 W (I_{CC} = 80 μA)

In case the power consumption Pc is 1.7 W, the junction temperature Tj can be calculated as follows:

$$Tj = Pc \times \theta jc + Tc$$
$$Tj = 1.7\ W \times \theta jc + 80\ °C$$
Tj = 81.7 °C (θjc (bottom) = 1 °C / W Refer to Page 4 Thermal Design)

The junction temperature is 81.7 °C, at above condition.

Selection of Components Externally Connected

・VCC pin capacitor

Insert capacitors with a capacitance of 0.1 μF or higher between the VCC and GND pin. We recommend using ceramic capacitor generally featuring good high frequency characteristic. When selecting a ceramic capacitor, please be consider about temperature and DC - biasing characteristics. Place capacitors closest possible to VCC - GND pin. When input impedance is high, e.g. in case there is distance from battery, line voltage drop needs to be prevented by large capacitor. Choose the capacitance according to the line impedance between the power smoothing circuit and the VCC pin. Selection of the capacitance also depends on the applications. Verify the application and allow sufficient margins in the design. We recommend using a capacitor with excellent voltage and temperature characteristics.

・Output pin capacitor

In order to prevent oscillation, a capacitor needs to be placed between the output pin and GND pin. We recommend using a ceramic capacitor with a capacitance of 6 μF or higher. In selecting the capacitor, ensure that the capacitance of 6 μF or higher is maintained at the intended applied voltage and temperature range. Due to changes in temperature the capacitor's capacitance can fluctuate possibly resulting in oscillation.

In actual applications the stable operating range is influenced by the PCB impedance, input supply impedance and load impedance. Therefore verification of the final operating environment is needed. When selecting a ceramic capacitor, we recommend using X7R or better components with excellent temperature and DC - biasing characteristics and high voltage tolerance.

In case of the transient input voltage and the load current fluctuation, output voltage may fluctuate. In case this fluctuation can be problematic for the application, connect low ESR capacitor (capacitance > 6 μF, ESR < 1 Ω) in paralleled to large capacitor with a capacitance of 13 μF or higher and ESR of 5 Ω or lower. Electrolytic and tantalum capacitors can be used as large capacitor. When selecting an electrolytic capacitor, please consider about increasing ESR and decreasing capacitance at cold temperature.

Place the capacitor closest possible to output pin.

I/O equivalence circuits

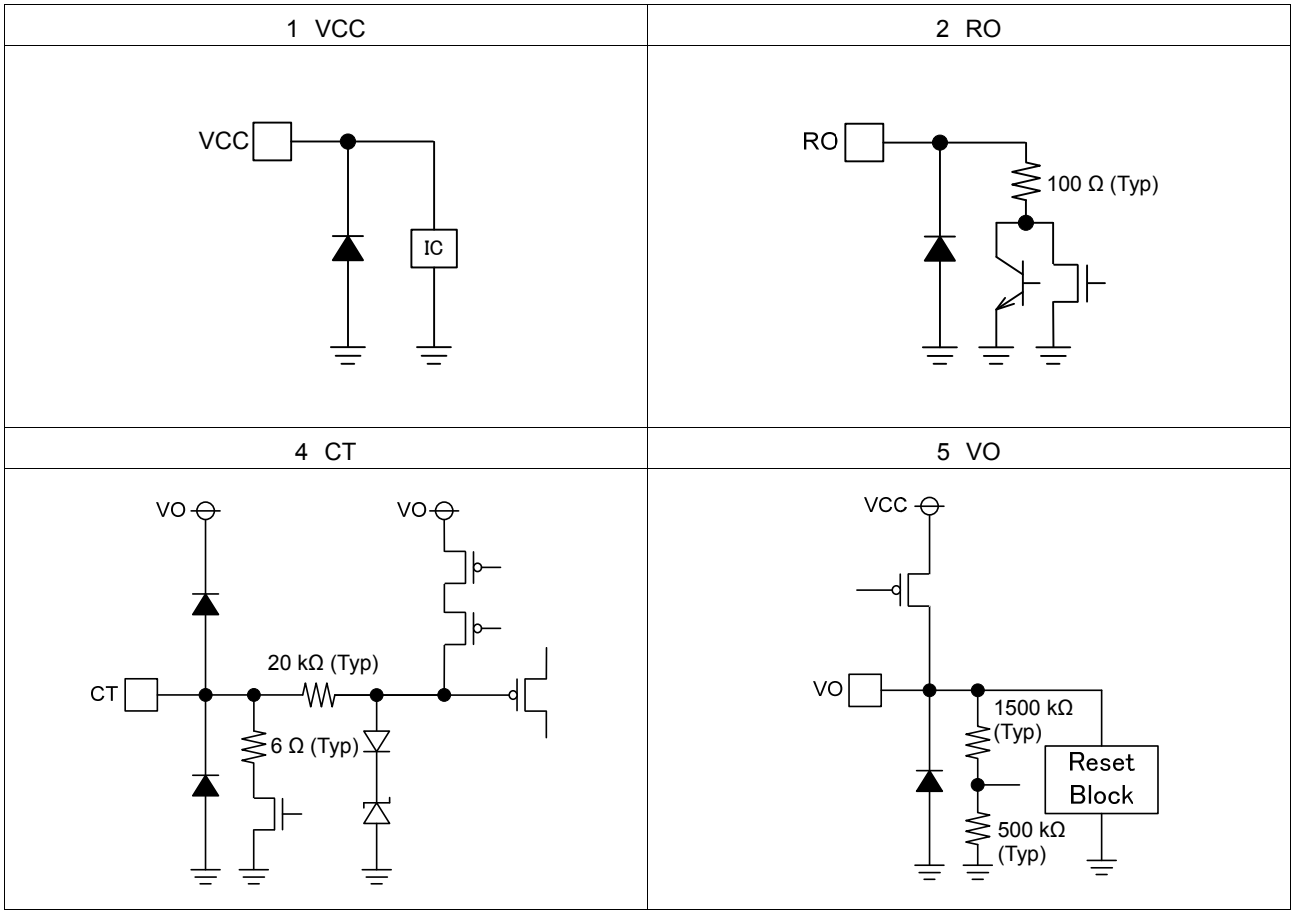


Figure 23. I / O equivalence circuits

Application Examples

・Applying positive surge to the VCC
If the possibility exists that surges higher than 45 V will be applied to the VCC, a Zener Diode should be placed between the VCC and GND as shown in the figure below.

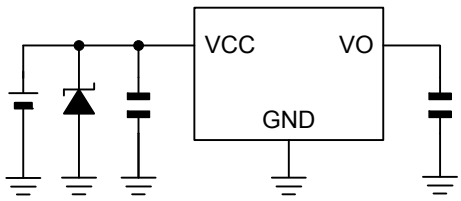


Figure 24. Application Example 1

・Applying negative surge to the VCC
If the possibility exists that negative surges lower than the GND are applied to the VCC, a Shottky Diode should be place between the VCC and GND as shown in the figure below.

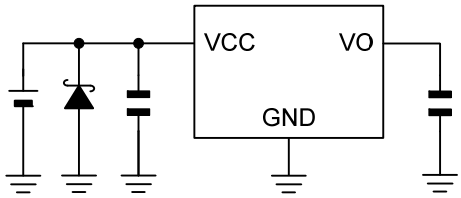


Figure 25. Application Example 2

・Implementing a Protection Diode
If the possibility exists that a large inductive load is connected to the output pin resulting in back-EMF at time of startup and shutdown, a protection diode should be placed as shown in the figure below.

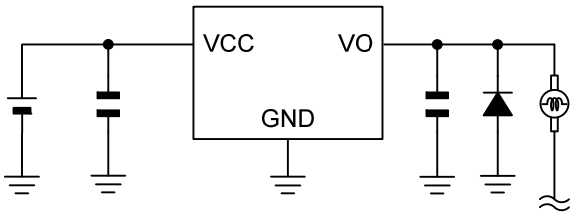


Figure 26. Application Example 3

・Reverse Polarity Diode
In some applications, the VCC and the VO potential might be reversed, possibly resulting in circuit internal damage or damage to the elements. For example, the accumulated charge in the output pin capacitor flowing backward from the VO to the VCC when the VCC shorts to the GND. In order to minimize the damage in such case, use a capacitor with a capacitance less than 1000 μF. Also by inserting a reverse polarity diode in series to the VCC, it can prevent reverse current from reverse battery connection or the case. When the point A is short-circuited GND, if there may be any possible case point B is short-circuited to GND, we also recommend using a bypass diode between the VCC and the VO.

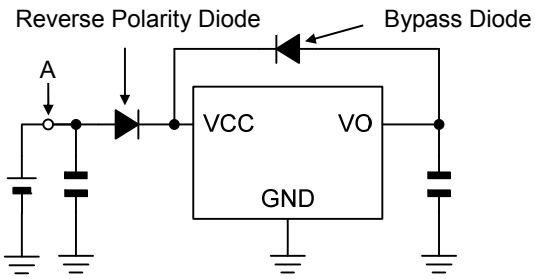


Figure 27. Application Example 4

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   The power dissipation under actual operating conditions should be taken into consideration and a sufficient margin should be allowed for in the thermal design. On the reverse side of the package, the IC has an exposed heat pad for improving the heat dissipation. Use both the front and reverse side of the PCB to increase the heat dissipation pattern as far as possible. The amount of heat generated depends on the voltage difference across the input and output, load current, and bias current. Therefore, when actually using the chip, ensure that the generated heat does not exceed the Pd rating.
   Should by any condition the maximum junction temperature Tjmax = 150 °C rating be exceeded by the temperature increase of the chip, it may result in deterioration of the properties of the chip. The thermal impedance in this specification is based on recommended PCB and measurement condition by JEDEC standard. Verify the application and allow sufficient margins in the thermal design.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

10. Unused Input Pins

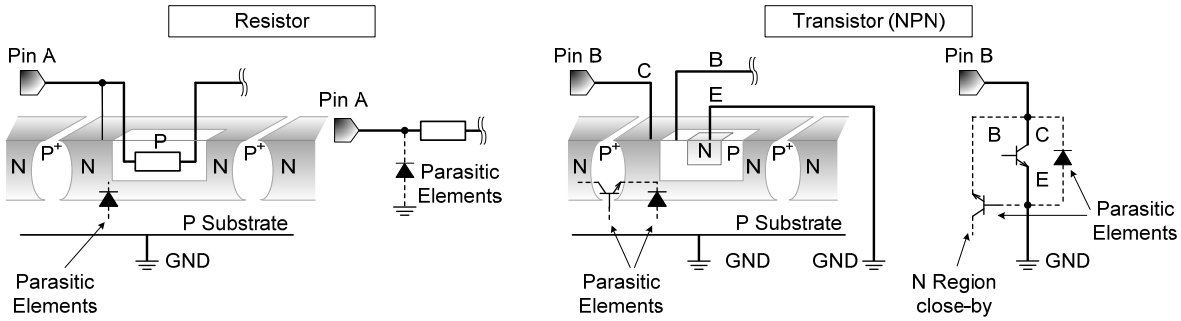
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



12. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Thermal Shutdown Circuit(TSD)

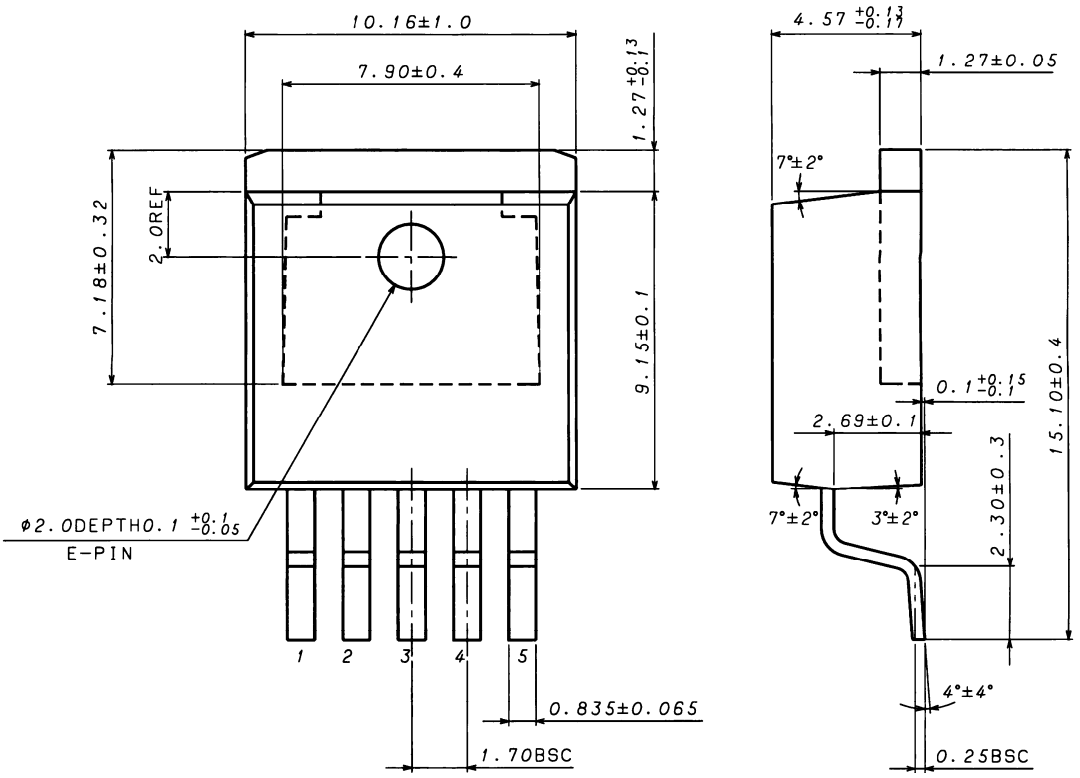
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

14. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Physical Dimension Tape and Reel Information

Package Name	TO263-5F



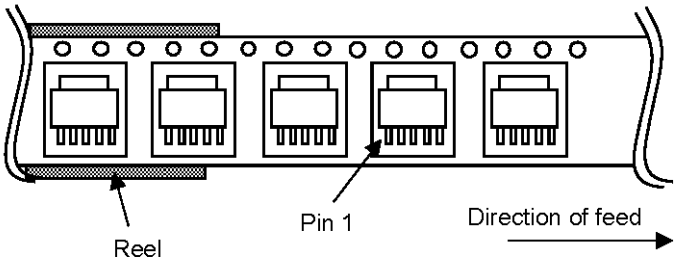
(UNIT:mm)

PKG:TO263-5F

Drawing No.EX563-5001

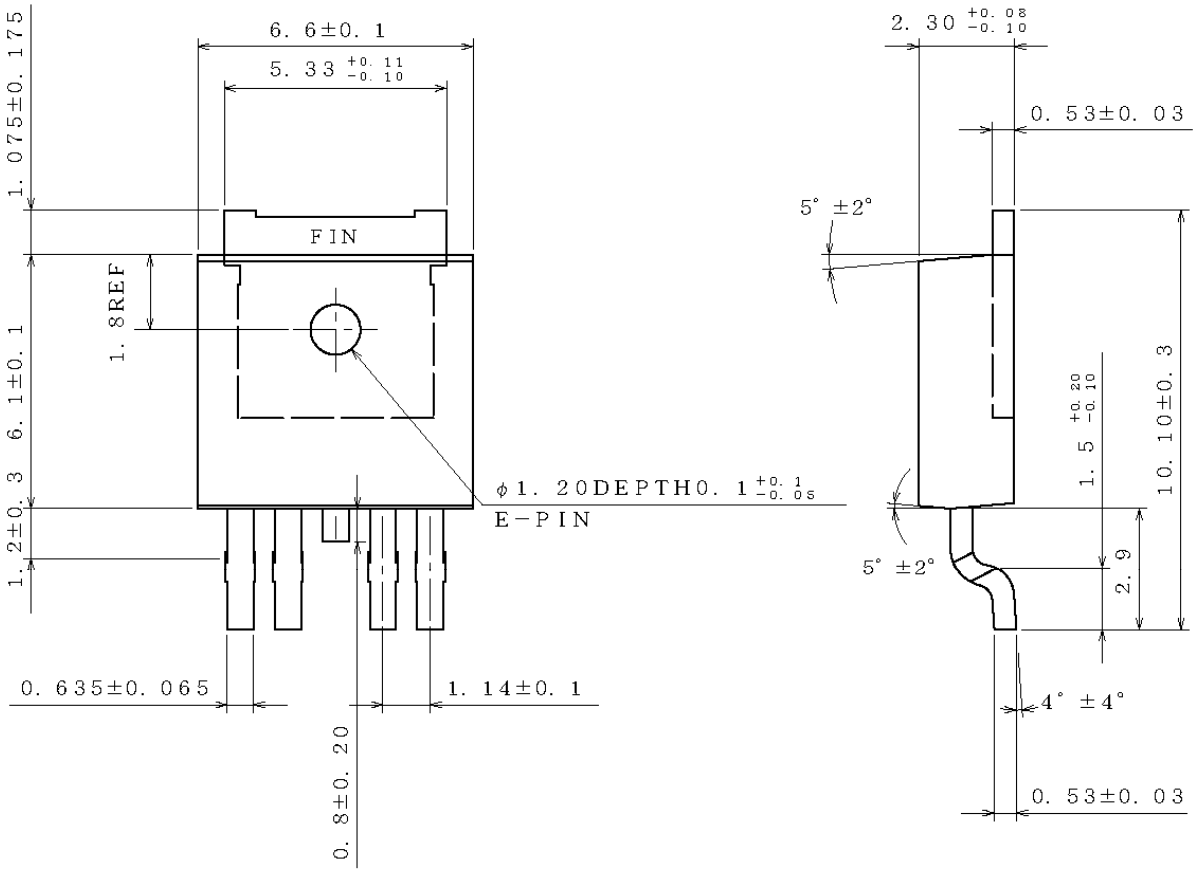
< Tape and Reel Information >

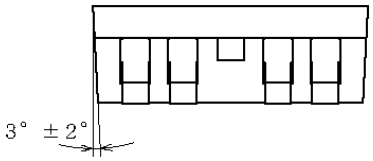
Tape	Embossed carrier tape
Quantity	500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand



Physical Dimension Tape and Reel Information – continued

Package Name	TO252-J5F

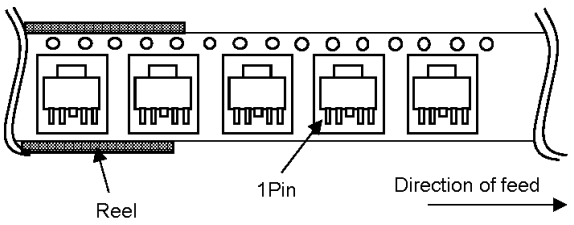




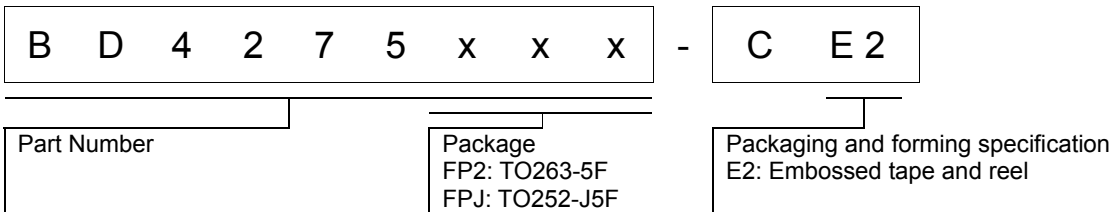
(UNIT:mm)
PKG:TO252−J5F
Drawing No. EX567−5001

< Tape and Reel Information >

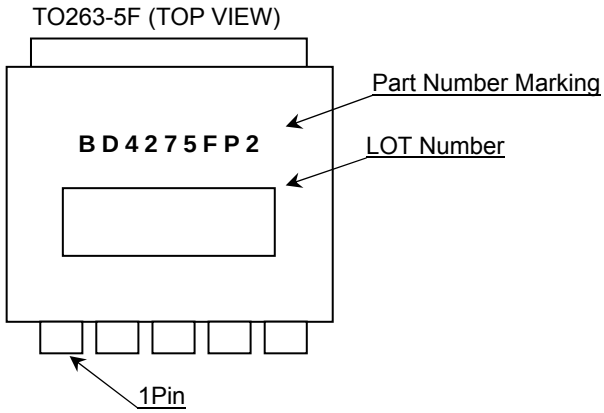
Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand)

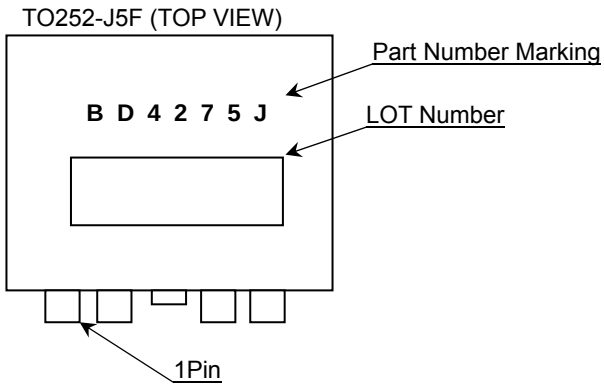


Ordering Information



Marking Diagram





Revision History

Date	Revision	Changes
5.Apr.2013	001	New Release
25.Sep.2013	002	P5 The condition of RO L Voltage at Electrical Characteristics was changed. P10 The Timing Chart was corrected. P11 The statement of “Reference Data” of Package data of TO263-5F and TO252-J5F was deleted. P13 The information of “Output pin capacitor” was changed. P15 The information of “Operational Notes” was changed. P17 TO263-5F quantity written in “Tape and reel information” was corrected. P18 TO252-J5F physical dimension was corrected.
29.Nov.2013	003	P11 The package data of TO263-5F was corrected. P16 The information of “Operational Notes” was changed.
20.May.2015	004	P1 Key Specifications (Reset Detect Voltage) was corrected. P1 AEC-Q100 grade was added. P1 The information of VCC and VO pin capacitors at Typical Application Circuit was added. P4 Revised expression on annotation of Thermal Resistance. P11 Revised expression on the PCB information of Power Dissipation. P13 Revised expression on the information of VCC pin and Output pin capacitors. P14 Added description on Reverse Polarity Diode. P15 Revised expression on the information of Thermal Consideration. P17 TO263-5F Direction of feed written in “Tape and reel information” was corrected.

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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