May 2014

FDN86265P

P-Channel PowerTrench® MOSFET

-150 V, -0.8 A, 1.2 Ω

Features

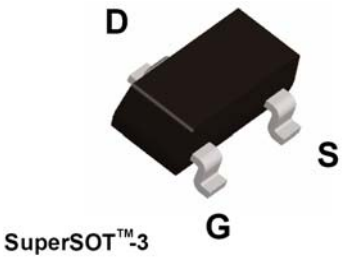
- Max $r_{DS(on)}$ = 1.2 Ω at V_{GS} = -10 V, I_D = -0.8 A
- Max $r_{DS(on)}$ = 1.4 Ω at V_{GS} = -6 V, I_D = -0.7 A
- Very low RDS-on mid voltage P-channel silicon technology optimised for low Qg
- This product is optimised for fast switching applications as well as load switch applications
- 100% UIL tested
- RoHS Compliant

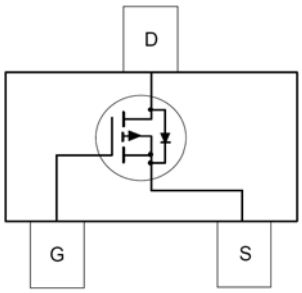
General Description

This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been optimized for the on-state resistance and yet maintain superior switching performance.

Applications

- Active Clamp Switch
- Load Switch





MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		-150	V
V_{GS}	Gate to Source Voltage		±25	V
I_D	-Continuous	(Note 1a)	-0.8	A
	-Pulsed		-5	
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	6	mJ
P_D	Power Dissipation	(Note 1a)	1.5	W
	Power Dissipation	(Note 1b)	0.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	75	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	80	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
265	FDN86265P	SSOT-3	7 ”	8 mm	3000 units

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Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250 μA, V_{GS} = 0 V	-150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		-129		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -120 V, V_{GS} = 0 V			-1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±25 V, V_{DS} = 0 V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250 μA	-2	-3.3	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -10 V, I_D = -0.8 A		0.85	1.2	Ω
		V_{GS} = -6 V, I_D = -0.7 A		0.96	1.4	
		V_{GS} = -10 V, I_D = -0.8 A, T_J = 125 °C		1.54	2.2	
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -0.8 A		1.5		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -75 V, V_{GS} = 0 V, f = 1 MHz		158	210	pF
C_{oss}	Output Capacitance			17	25	pF
C_{rss}	Reverse Transfer Capacitance			1.6	5	pF
R_g	Gate Resistance		0.1	3.3	6.7	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -75 V, I_D = -0.8 A, V_{GS} = -10 V, R_{GEN} = 6 Ω		5.7	12	ns
t_r	Rise Time			2.2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			7.9	16	ns
t_f	Fall Time			9.9	20	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to -10 V, V_{DD} = -75 V, I_D = -0.8 A		2.9	4.1	nC
Q_{gs}	Gate to Source Gate Charge			0.8		nC
Q_{gd}	Gate to Drain “Miller” Charge			0.8		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.8 A (Note 2)		-0.86	-1.3	V
t_{rr}	Reverse Recovery Time	I_F = -0.8 A, di/dt = 100 A/μs		49	78	ns
Q_{rr}	Reverse Recovery Charge			70	112	nC

Notes:
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 80 °C/W when mounted on a 1 in^2 pad of 2 oz copper

b) 180 °C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. Starting T_J = 25 °C; N-ch: L = 3 mH, I_{AS} = -2 A, V_{DD} = -150 V, V_{GS} = -10 V. 100% test at L = 0.1 mH, I_{AS} = -9 A.

Typical Characteristics T_J = 25 °C unless otherwise noted

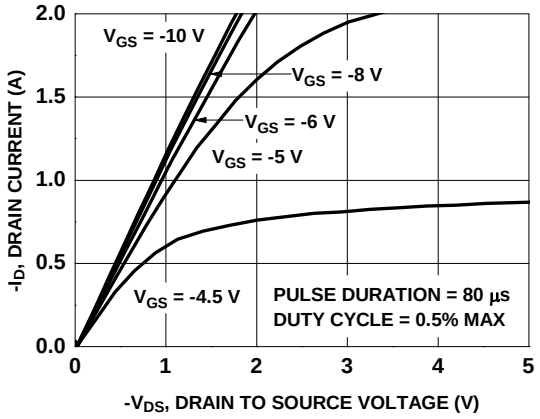

Figure 1. On Region Characteristics

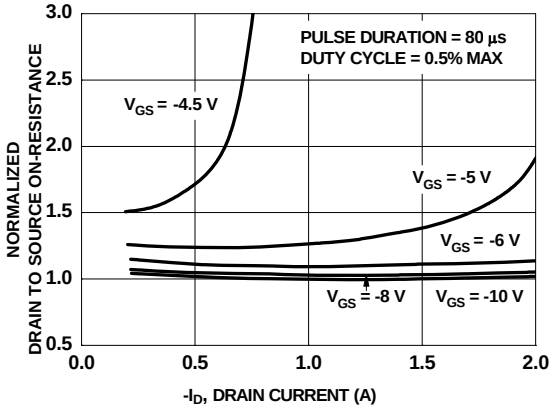

Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

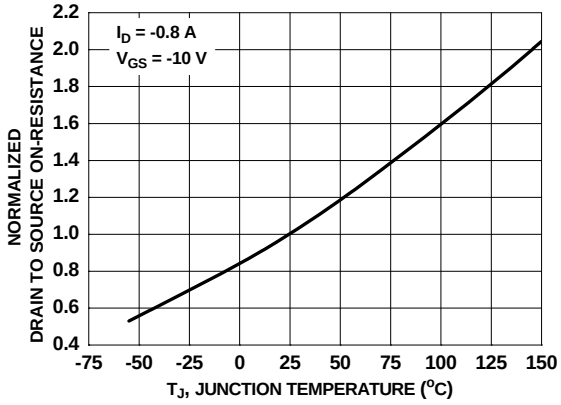

Figure 3. Normalized On Resistance vs Junction Temperature

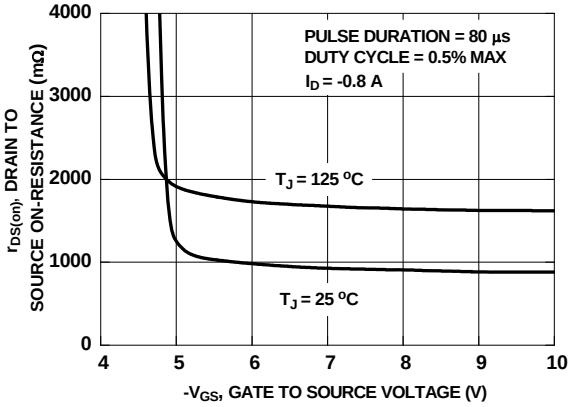

Figure 4. On-Resistance vs Gate to Source Voltage

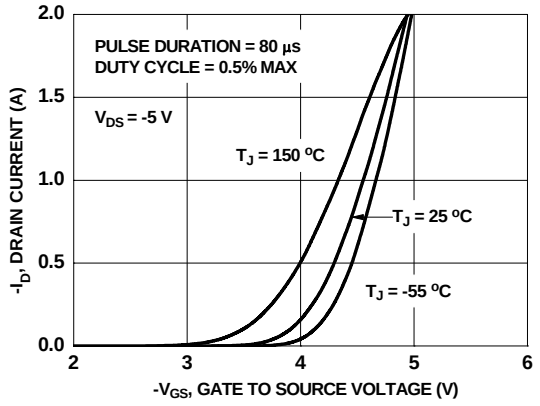

Figure 5. Transfer Characteristics

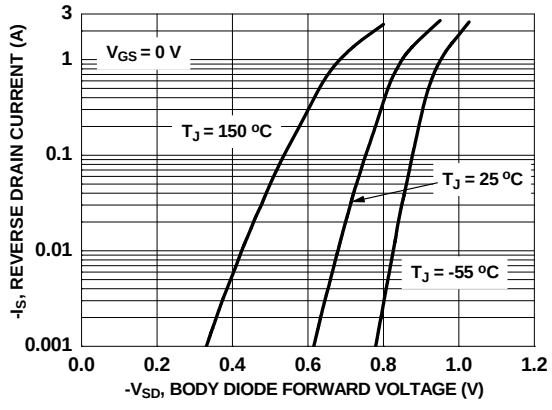

Figure 6. Source to Drain Diode Forward Voltage vs Source Current

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