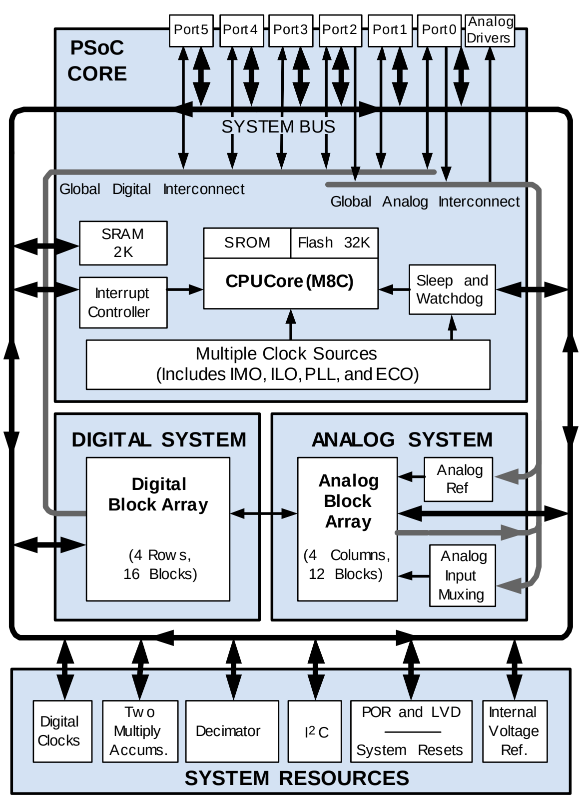
Automotive: CY8C29466 and CY8C29666

Features

- **Powerful Harvard Architecture Processor**
  - M8C Processor Speeds to 12 MHz
  - Two 8x8 Multiply, 32-Bit Accumulate
  - Low Power at High Speed
  - 4.75V to 5.25V Operating Voltage
  - Automotive Temp. Range: -40°C to +125°C
- **Advanced Peripherals (PSoC Blocks)**
  - 12 Rail-to-Rail Analog PSoC Blocks Provide:
    - Up to 14-Bit ADCs
    - Up to 9-Bit DACs
    - Programmable Gain Amplifiers
    - Programmable Filters and Comparators
  - 16 Digital PSoC Blocks Provide:
    - 8- to 32-Bit Timers, Counters, and PWMs
    - CRC and PRS Modules
    - Up to 4 Full-Duplex UARTs
    - Multiple SPI™ Masters or Slaves
    - Connectable to all GPIO Pins
  - Complex Peripherals by Combining Blocks
- **Precision, Programmable Clocking**
  - Internal ±4% 24 MHz Oscillator
  - 24 MHz with Optional 32.768 kHz Crystal
  - Optional External Oscillator, up to 24 MHz
  - Internal Oscillator for Watchdog and Sleep
- **Flexible On-Chip Memory**
  - 32K Bytes Flash Program Storage 100 Erase/Write Cycles
  - 2K Bytes SRAM Data Storage
  - In-System Serial Programming (ISSP™)
  - Partial Flash Updates
  - Flexible Protection Modes
- **Programmable Pin Configurations**
  - 25 mA Sink on All GPIO
  - Pull Up, Pull Down, High Z, Strong, or Open Drain Drive Modes on all GPIO
  - Up to 12 Analog Inputs on GPIO
  - Four 30 mA Analog Outputs on GPIO
  - Configurable Interrupt on All GPIO
- **Additional System Resources**
  - I^2C™ Slave, Master, and Multi-Master to 400 kHz
  - Watchdog and Sleep Timers
  - User-Configurable Low Voltage Detection
  - Integrated Supervisory Circuit
  - On-Chip Precision Voltage Reference
- **Complete Development Tools**
  - Free Development Software (PSoC™ Designer)
  - Full-Featured, In-Circuit Emulator and Programmer
  - Full Speed Emulation
  - Complex Breakpoint Structure
  - 128K Bytes Trace Memory
  - Complex Events
  - C Compilers, Assembler, and Linker



PSoC™ Functional Overview

The PSoC™ family consists of many *Mixed-Signal Array with On-Chip Controller* devices. These devices are designed to replace multiple traditional MCU-based system components with one, low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, as well as programmable interconnects. This architecture allows the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts and packages.

The PSoC architecture, as illustrated on the left, is comprised of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global busing allows all the device resources to be combined into a complete custom system. The PSoC CY8C29x66 automotive family can have up to six IO ports that connect to the global digital and analog interconnects, providing access to 16 digital blocks and 12 analog blocks.

The PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose IO).

The M8C CPU core is a powerful processor with speeds up to 12 MHz, providing a two MIPS 8-bit Harvard architecture microprocessor. The CPU utilizes an interrupt controller with 25 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

Memory includes 32 KB of Flash for program storage and 2 KB of SRAM for data storage. Program Flash utilizes four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 4% over temperature and voltage. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

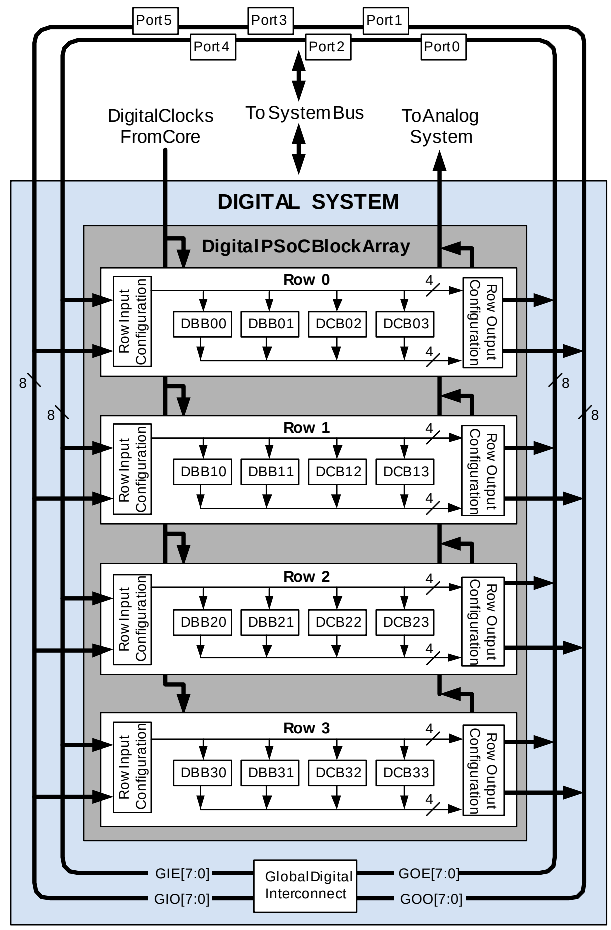
The Digital System

The Digital System is composed of 16 digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references. Digital peripheral configurations include those listed below.

- PWMs (8 to 32 bit)
- PWMs with Dead Band (8 to 32 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity (up to 4)
- SPI Master and Slave (up to 4 each)
- I2C Slave and Multi-master (1 available as a System Resource)
- Cyclical Redundancy Checker/Generator (8 to 32 bit)
- IrDA (up to 4)
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows you the optimum choice of system resources for your application. Family resources are shown in the table titled "PSoC Device Characteristics" on page 3.



Digital System Block Diagram

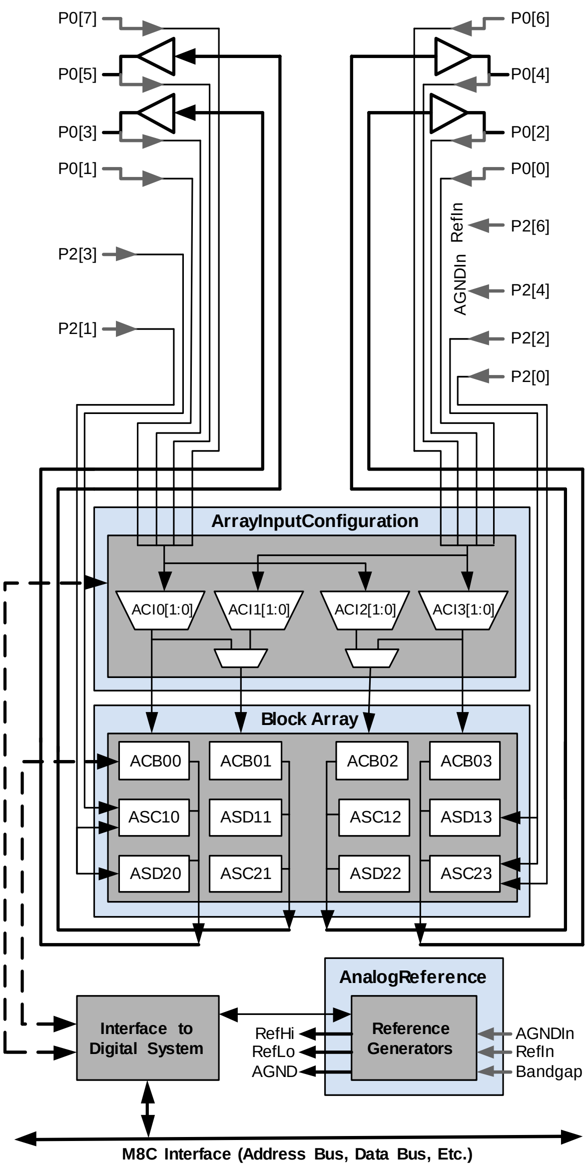
The Analog System

The Analog System is composed of 12 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are listed below.

- Analog-to-digital converters (up to 4, with 6- to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (2, 4, 6, or 8 pole band-pass, low-pass, and notch)
- Amplifiers (up to 4, with selectable gain to 48x)
- Instrumentation amplifiers (up to 2, with selectable gain to 93x)
- Comparators (up to 4, with 16 selectable thresholds)
- DACs (up to 4, with 6- to 9-bit resolution)
- Multiplying DACs (up to 4, with 6- to 9-bit resolution)
- High current output drivers (four with 40 mA drive as a PSoC Core resource)
- 1.3V reference (as a System Resource)
- DTMF Dialer

- Modulators
- Correlators
- Peak Detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks, as shown in the figure below.



Analog System Block Diagram

Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, switch mode pump, low voltage detection, and power on reset. Brief statements describing the merits of each system resource are presented below.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Two multiply accumulates (MACs) provide fast 8-bit multiplier with 32-bit accumulate to assist in both general math as well as digital filters.
- The decimator provides a custom hardware filter for digital signal, processing applications including the creation of Delta Sigma ADCs.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 voltage reference provides an absolute reference for the analog system, including ADCs and DACs.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 3 analog blocks. The following table lists the resources available for specific PSoC device groups. The PSoC device covered by this data sheet is highlighted below.

PSoC Device Characteristics

PSoC Device Group	Digital IO (max)	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	Amount of SRAM	Amount of Flash
CY8C29x66	**44**	**4**	**16**	**12**	**4**	**4**	**12**	**2 KB**	**32 KB**
CY8C27x43	44	2	8	12	4	4	12	256 Bytes	16 KB
CY8C24x23	24	1	4	12	2	2	6	256 Bytes	4 KB
CY8C24x23A	24	1	4	12	2	2	6	256 Bytes	4 KB
CY8C22x13	16	1	4	8	1	1	3	256 Bytes	2 KB
CY8C21x34	28	1	4	28	0	2	4[a]	512 Bytes	8 KB
CY8C21x23	16	1	4	8	0	2	4[a]	256 Bytes	4 KB

a. Limited analog functionality.

Getting Started

The quickest path to understanding the PSoC silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, reference the *PSoC™ Mixed-Signal Array Technical Reference Manual*.

For up-to-date Ordering, Packaging, and Electrical Specification information, reference the latest PSoC device data sheets on the web at http://www.cypress.com/psoc.

Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store at http://www.onfulfillment.com/cypressstore/ contains development kits, C compilers, and all accessories for PSoC development. Click on *PSoC (Programmable System-on-Chip)* to view a current list of available items.

Tele-Training

Free PSoC "Tele-training" is available for beginners and taught by a live marketing or application engineer over the phone. Five training classes are available to accelerate the learning curve including introduction, designing, debugging, advanced design, advanced analog, as well as application-specific classes covering topics like PSoC and the LIN bus. For days and times of the tele-training, see http://www.cypress.com/support/training.cfm.

Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant, go to the following Cypress support web site: http://www.cypress.com/support/cypros.cfm.

Technical Support

PSoC application engineers take pride in fast and accurate response. They can be reached with a 4-hour guaranteed response at http://www.cypress.com/support/login.cfm.

Application Notes

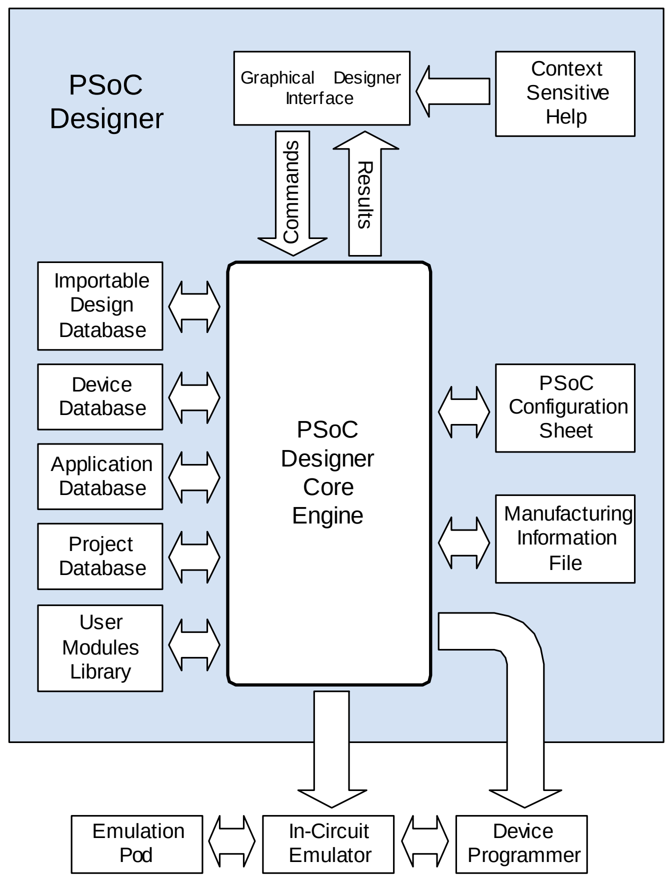
A long list of application notes will assist you in every aspect of your design effort. To locate the PSoC application notes, go to http://www.cypress.com/design/results.cfm.

Development Tools

The Cypress MicroSystems PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows NT 4.0, Windows 2000, Windows Millennium (Me), or Windows XP. (Reference the PSoC Designer Functional Flow diagram below.)

PSoC Designer helps the customer to select an operating configuration for the PSoC, write application code that uses the PSoC, and debug the application. This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and the CYASM macro assembler for the CPUs.

PSoC Designer also supports a high-level C language compiler developed specifically for the devices in the family.



PSoC Designer Subsystems

PSoC Designer Software Subsystems

Device Editor

The Device Editor subsystem allows the user to select different onboard analog and digital components called user modules using the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

PSoC Designer sets up power-on initialization tables for selected PSoC block configurations and creates source code for an application framework. The framework contains software to operate the selected components and, if the project uses more than one operating configuration, contains routines to switch between different sets of PSoC block configurations at run time. PSoC Designer can print out a configuration sheet for a given project configuration for use during application programming in conjunction with the Device Data Sheet. Once the framework is generated, the user can add application-specific code to flesh out the framework. It's also possible to change the selected components and regenerate the framework.

Design Browser

The Design Browser allows users to select and import preconfigured designs into the user's project. Users can easily browse a catalog of preconfigured designs to facilitate time-to-design. Examples provided in the tools include a 300-baud modem, LIN Bus master and slave, fan controller, and magnetic card reader.

Application Editor

In the Application Editor you can edit your C language and Assembly language source code. You can also assemble, compile, link, and build.

Assembler. The macro assembler allows the assembly code to be merged seamlessly with C code. The link libraries automatically use absolute addressing or can be compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compiler. A C language compiler is available that supports Cypress MicroSystems' PSoC family devices. Even if you have never worked in the C language before, the product quickly allows you to create complete C programs for the PSoC family devices.

The embedded, optimizing C compiler provides all the features of C tailored to the PSoC architecture. It comes complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing the designer to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of the USB port. The base unit is universal and will operate with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

Designing with User Modules

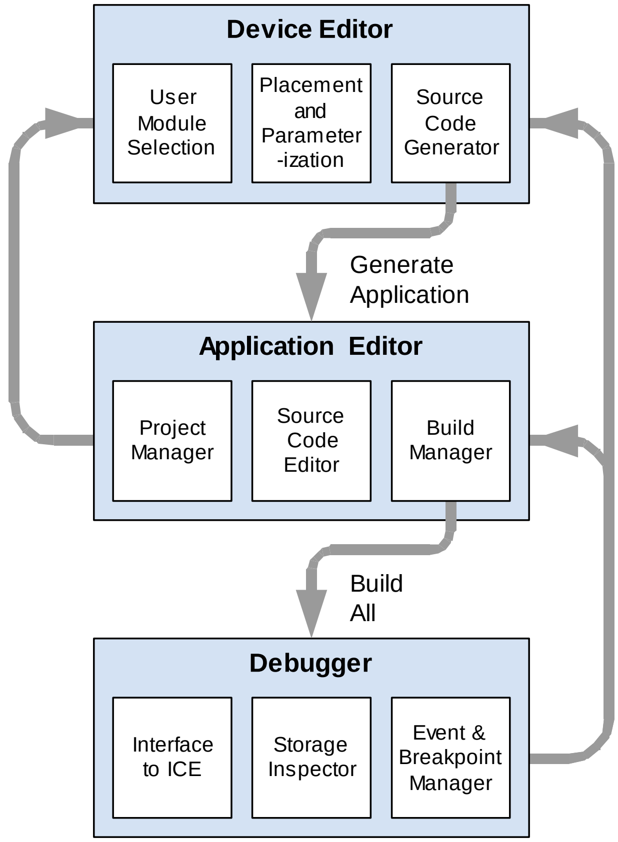
The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. Each block has several registers that determine its function and connectivity to other blocks, multiplexers, buses, and to the IO pins. Iterative development cycles permit you to adapt the hardware as well as the software. This substantially lowers the risk of having to select a different part to meet the final design requirements.

To speed the development process, the PSoC Designer Integrated Development Environment (IDE) provides a library of pre-built, pre-tested hardware peripheral functions, called "User Modules." User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties. The standard User Module library contains over 50 common peripherals such as ADCs, DACs Timers, Counters, UARTs, and other not-so common peripherals such as DTMF Generators and Bi-Quad analog filter sections.

Each user module establishes the basic register settings that implement the selected function. It also provides parameters that allow you to tailor its precise configuration to your particular application. For example, a Pulse Width Modulator User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. User modules also provide tested software to cut your development time. The user module application programming interface (API) provides high-level functions to control and respond to hardware events at run-time. The API also provides optional interrupt service routines that you can adapt as needed.

The API functions are documented in user module data sheets that are viewed directly in the PSoC Designer IDE. These data sheets explain the internal operation of the user module and provide performance specifications. Each data sheet describes the use of each user module parameter and documents the setting of each register controlled by the user module.

The development process starts when you open a new project and bring up the Device Editor, a graphical user interface (GUI) for configuring the hardware. You pick the user modules you need for your project and map them onto the PSoC blocks with point-and-click simplicity. Next, you build signal chains by interconnecting user modules to each other and the IO pins. At this stage, you also configure the clock source connections and enter parameter values directly or by selecting values from drop-down menus. When you are ready to test the hardware configuration or move on to developing code for the project, you perform the "Generate Application" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the high-level user module API functions.



User Module and Source Code Development Flows

The next step is to write your main program, and any sub-routines using PSoC Designer's Application Editor subsystem. The Application Editor includes a Project Manager that allows you to open the project source code files (including all generated code files) from a hierarchal view. The source code editor provides syntax coloring and advanced edit features for both C and assembly language. File search capabilities include simple string searches and recursive "grep-style" patterns. A single mouse click invokes the Build Manager. It employs a professional-strength "makefile" system to automatically analyze all file dependencies and run the compiler and assembler as necessary. Project-level options control optimization strategies used by the compiler and linker. Syntax errors are displayed in a console window. Double clicking the error message takes you directly to the offending line of source code. When all is correct, the linker builds a HEX file image suitable for programming.

The last step in the development process takes place inside the PSoC Designer's Debugger subsystem. The Debugger downloads the HEX file to the In-Circuit Emulator (ICE) where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose IO
GUI	graphical user interface
HBM	human body model
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
IO	input/output
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
PLL	phase-locked loop
POR	power on reset
PPOR	precision power on reset
PSoC™	Programmable System-on-Chip™
PWM	pulse width modulator
SC	switched capacitor
SRAM	static random access memory

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 3-1 on page 13 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexidecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexidecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (e.g., 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or 0x are decimal.

Table of Contents

For an in depth discussion and more information on your PSoC device, obtain the *PSoC Mixed-Signal Array Technical Reference Manual*. This document encompasses and is organized into the following chapters and sections.

1. Pin Information

This chapter describes, lists, and illustrates the CY8C29x66 automotive PSoC device pins and pinout configurations.

1.1 Pinouts

The CY8C29x66 automotive PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital IO. However, Vss, Vdd, and XRES are not capable of Digital IO.

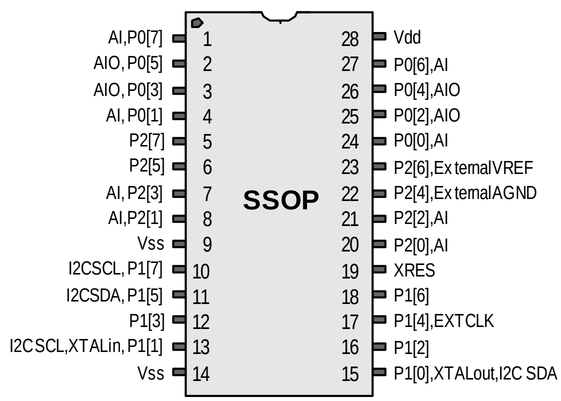
1.1.1 28-Pin Part Pinout

Table 1-1: 28-Pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P0[7]	Analog column mux input.
2	IO	IO	P0[5]	Analog column mux input and column output.
3	IO	IO	P0[3]	Analog column mux input and column output.
4	IO	I	P0[1]	Analog column mux input.
5	IO		P2[7]	
6	IO		P2[5]	
7	IO	I	P2[3]	Direct switched capacitor block input.
8	IO	I	P2[1]	Direct switched capacitor block input.
9	Power		Vss	Ground connection.
10	IO		P1[7]	I2C Serial Clock (SCL).
11	IO		P1[5]	I2C Serial Data (SDA).
12	IO		P1[3]	
13	IO		P1[1]	Crystal (XTALin), I2C Serial Clock (SCL).
14	Power		Vss	Ground connection.
15	IO		P1[0]	Crystal (XTALout), I2C Serial Data (SDA).
16	IO		P1[2]	
17	IO		P1[4]	Optional External Clock Input (EXTCLK).
18	IO		P1[6]	
19	Input		XRES	Active high external reset with internal pull down.
20	IO	I	P2[0]	Direct switched capacitor block input.
21	IO	I	P2[2]	Direct switched capacitor block input.
22	IO		P2[4]	External Analog Ground (AGND).
23	IO		P2[6]	External Voltage Reference (VREF).
24	IO	I	P0[0]	Analog column mux input.
25	IO	IO	P0[2]	Analog column mux input and column output.
26	IO	IO	P0[4]	Analog column mux input and column output.
27	IO	I	P0[6]	Analog column mux input.
28	Power		Vdd	Supply voltage.

LEGEND: A = Analog, I = Input, and O = Output.

CY8C29466 28-Pin PSoC Device



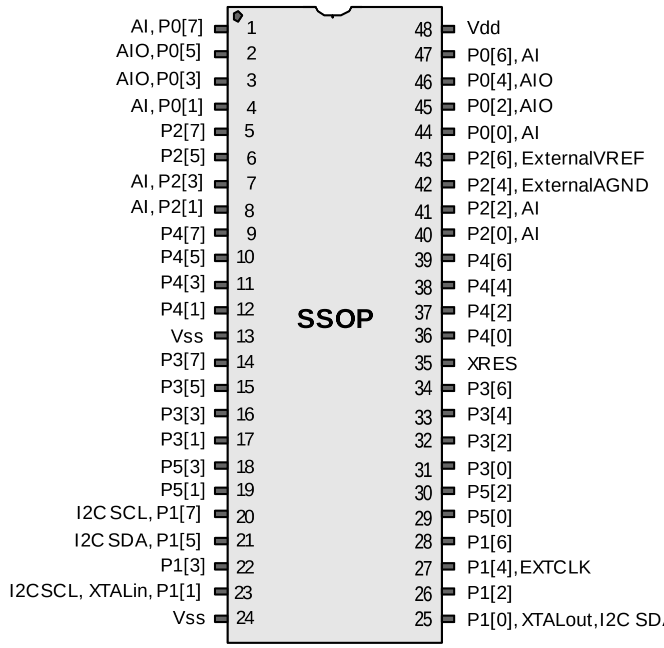
1.1.2 48-Pin Part Pinouts

Table 1-2: 48-Pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P0[7]	Analog column mux input.
2	IO	IO	P0[5]	Analog column mux input and column output.
3	IO	IO	P0[3]	Analog column mux input and column output.
4	IO	I	P0[1]	Analog column mux input.
5	IO		P2[7]	
6	IO		P2[5]	
7	IO	I	P2[3]	Direct switched capacitor block input.
8	IO	I	P2[1]	Direct switched capacitor block input.
9	IO		P4[7]	
10	IO		P4[5]	
11	IO		P4[3]	
12	IO		P4[1]	
13	Power		Vss	Ground connection.
14	IO		P3[7]	
15	IO		P3[5]	
16	IO		P3[3]	
17	IO		P3[1]	
18	IO		P5[3]	
19	IO		P5[1]	
20	IO		P1[7]	I2C Serial Clock (SCL).
21	IO		P1[5]	I2C Serial Data (SDA).
22	IO		P1[3]	
23	IO		P1[1]	Crystal (XTALin), I2C Serial Clock (SCL).
24	Power		Vss	Ground connection.
25	IO		P1[0]	Crystal (XTALout), I2C Serial Data (SDA).
26	IO		P1[2]	
27	IO		P1[4]	Optional External Clock Input (EXTCLK).
28	IO		P1[6]	
29	IO		P5[0]	
30	IO		P5[2]	
31	IO		P3[0]	
32	IO		P3[2]	
33	IO		P3[4]	
34	IO		P3[6]	
35	Input		XRES	Active high external reset with internal pull down.
36	IO		P4[0]	
37	IO		P4[2]	
38	IO		P4[4]	
39	IO		P4[6]	
40	IO	I	P2[0]	Direct switched capacitor block input.
41	IO	I	P2[2]	Direct switched capacitor block input.
42	IO		P2[4]	External Analog Ground (AGND).
43	IO		P2[6]	External Voltage Reference (VREF).
44	IO	I	P0[0]	Analog column mux input.
45	IO	IO	P0[2]	Analog column mux input and column output.
46	IO	IO	P0[4]	Analog column mux input and column output.
47	IO	I	P0[6]	Analog column mux input.
48	Power		Vdd	Supply voltage.

LEGEND: A = Analog, I = Input, and O = Output.

CY8C29666 48-Pin PSoC Device



2. Register Reference

This chapter lists the registers of the CY8C29x66 automotive PSoC device. For detailed register information, reference the *PSoC™ Mixed-Signal Array Technical Reference Manual*.

2.1 Register Conventions

2.1.1 Abbreviations Used

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

2.2 Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as IO space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and should not be accessed.

Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBB20DR0	40	#	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0IE	01	RW	DBB20DR1	41	W	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0GS	02	RW	DBB20DR2	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0DM2	03	RW	DBB20CR0	43	#	ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DR	04	RW	DBB21DR0	44	#	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1IE	05	RW	DBB21DR1	45	W	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1GS	06	RW	DBB21DR2	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1DM2	07	RW	DBB21CR0	47	#	ASD11CR3	87	RW		C7	
PRT2DR	08	RW	DCB22DR0	48	#	ASC12CR0	88	RW	RDI3RI	C8	RW
PRT2IE	09	RW	DCB22DR1	49	W	ASC12CR1	89	RW	RDI3SYN	C9	RW
PRT2GS	0A	RW	DCB22DR2	4A	RW	ASC12CR2	8A	RW	RDI3IS	CA	RW
PRT2DM2	0B	RW	DCB22CR0	4B	#	ASC12CR3	8B	RW	RDI3LT0	CB	RW
PRT3DR	0C	RW	DCB23DR0	4C	#	ASD13CR0	8C	RW	RDI3LT1	CC	RW
PRT3IE	0D	RW	DCB23DR1	4D	W	ASD13CR1	8D	RW	RDI3RO0	CD	RW
PRT3GS	0E	RW	DCB23DR2	4E	RW	ASD13CR2	8E	RW	RDI3RO1	CE	RW
PRT3DM2	0F	RW	DCB23CR0	4F	#	ASD13CR3	8F	RW		CF	
PRT4DR	10	RW	DBB30DR0	50	#	ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW	DBB30DR1	51	W	ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW	DBB30DR2	52	RW	ASD20CR2	92	RW		D2	
PRT4DM2	13	RW	DBB30CR0	53	#	ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW	DBB31DR0	54	#	ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW	DBB31DR1	55	W	ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW	DBB31DR2	56	RW	ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW	DBB31CR0	57	#	ASC21CR3	97	RW	I2C_SCR	D7	#
	18		DCB32DR0	58	#	ASD22CR0	98	RW	I2C_DR	D8	RW
	19		DCB32DR1	59	W	ASD22CR1	99	RW	I2C_MSCR	D9	#
	1A		DCB32DR2	5A	RW	ASD22CR2	9A	RW	INT_CLR0	DA	RW
	1B		DCB32CR0	5B	#	ASD22CR3	9B	RW	INT_CLR1	DB	RW
	1C		DCB33DR0	5C	#	ASC23CR0	9C	RW	INT_CLR2	DC	RW
	1D		DCB33DR1	5D	W	ASC23CR1	9D	RW	INT_CLR3	DD	RW
	1E		DCB33DR2	5E	RW	ASC23CR2	9E	RW	INT_MSK3	DE	RW
	1F		DCB33CR0	5F	#	ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCB02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCB02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCB03DR0	2C	#	TMP0_DR	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP1_DR	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP2_DR	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP3_DR	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBB10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBB10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBB11CR0	37	#	ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCB12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCB13CR0	3F	#	ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBB20FN	40	RW	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0DM1	01	RW	DBB20IN	41	RW	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBB20OU	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW		43		ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBB21FN	44	RW	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1DM1	05	RW	DBB21IN	45	RW	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBB21OU	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW	DCB22FN	48	RW	ASC12CR0	88	RW	RDI3RI	C8	RW
PRT2DM1	09	RW	DCB22IN	49	RW	ASC12CR1	89	RW	RDI3SYN	C9	RW
PRT2IC0	0A	RW	DCB22OU	4A	RW	ASC12CR2	8A	RW	RDI3IS	CA	RW
PRT2IC1	0B	RW		4B		ASC12CR3	8B	RW	RDI3LT0	CB	RW
PRT3DM0	0C	RW	DCB23FN	4C	RW	ASD13CR0	8C	RW	RDI3LT1	CC	RW
PRT3DM1	0D	RW	DCB23IN	4D	RW	ASD13CR1	8D	RW	RDI3RO0	CD	RW
PRT3IC0	0E	RW	DCB23OU	4E	RW	ASD13CR2	8E	RW	RDI3RO1	CE	RW
PRT3IC1	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DM0	10	RW	DBB30FN	50	RW	ASD20CR0	90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW	DBB30IN	51	RW	ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW	DBB30OU	52	RW	ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW	DBB31FN	54	RW	ASC21CR0	94	RW		D4	
PRT5DM1	15	RW	DBB31IN	55	RW	ASC21CR1	95	RW		D5	
PRT5IC0	16	RW	DBB31OU	56	RW	ASC21CR2	96	RW		D6	
PRT5IC1	17	RW		57		ASC21CR3	97	RW		D7	
	18		DCB32FN	58	RW	ASD22CR0	98	RW		D8	
	19		DCB32IN	59	RW	ASD22CR1	99	RW		D9	
	1A		DCB32OU	5A	RW	ASD22CR2	9A	RW		DA	
	1B			5B		ASD22CR3	9B	RW		DB	
	1C		DCB33FN	5C	RW	ASC23CR0	9C	RW		DC	
	1D		DCB33IN	5D	RW	ASC23CR1	9D	RW	OSC_GO_EN	DD	RW
	1E		DCB33OU	5E	RW	ASC23CR2	9E	RW	OSC_CR4	DE	RW
	1F			5F		ASC23CR3	9F	RW	OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	W
DCB02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP0_DR	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP1_DR	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP2_DR	6E	RW		AE			EE	
	2F		TMP3_DR	6F	RW		AF			EF	
DBB10FN	30	RW	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10IN	31	RW	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10OU	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11FN	34	RW	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11IN	35	RW	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11OU	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12FN	38	RW	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12IN	39	RW	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12OU	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
	3B		ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13FN	3C	RW	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13IN	3D	RW	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13OU	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
	3F		ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

3. Electrical Specifications

This chapter presents the DC and AC electrical specifications of the CY8C29x66 automotive PSoC device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com/psoc.

Specifications are valid for -40^{o}C ≤ T_A ≤ 125^{o}C and T_J ≤ 135^{o}C, except where noted.

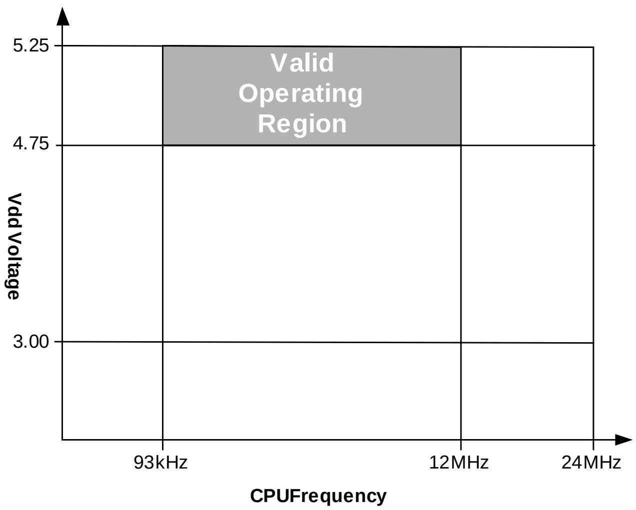


Figure 3-1. Voltage versus CPU Frequency

The following table lists the units of measure that are used in this chapter.

Table 3-1: Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
^{o}C	degree Celsius	µW	micro watts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nano ampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	Ω	ohm
MHz	megahertz	pA	pico ampere
MΩ	megaohm	pF	pico farad
µA	micro ampere	pp	peak-to-peak
µF	micro farad	ppm	parts per million
µH	micro henry	ps	picosecond
µs	microsecond	sps	samples per second
µV	micro volts	σ	sigma: one standard deviation
µVrms	micro volts root-mean-square	V	volts

3.1 Absolute Maximum Ratings

Table 3-2: Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	–	+100	^oC	Higher storage temperatures will reduce data retention time.
T_A	Ambient Temperature with Power Applied	-40	–	+125	^oC	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+5.75	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
V_{IOZ}	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+25	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD
LU	Latch-up Current	–	–	200	mA	

3.2 Operating Temperature

Table 3-3: Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+125	^oC	
T_J	Junction Temperature	-40	–	+135	^oC	The temperature rise from ambient to junction is package specific. See "Thermal Impedances" on page 29. The user must limit the power consumption to comply with this requirement.

3.3 DC Electrical Characteristics

3.3.1 DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 3-4: DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	4.75	–	5.25	V	
I_{DD}	Supply Current	–	8	15	mA	Conditions are Vdd=5.25V, -40 $^oC \le T_A \le$ 125 ^{o}C, CPU=3 MHz, SYSCLK doubler disabled. VC1=1.5 MHz, VC2=93.75 kHz, VC3=0.366 kHz. Analog power = off.
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active. Lower 3/4 temperature range.	–	6	16	µA	Conditions are with internal slow speed oscillator, Vdd = 5.25V, -40 $^oC \le T_A \le$ 55 ^{o}C. Analog power = off.
I_{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active. Higher 1/4 temperature range (hot).	–	6	100	µA	Conditions are with internal slow speed oscillator, Vdd = 5.25V, 55 $^oC < T_A \le$ 125 ^{o}C. Analog power = off.
I_{SBXTL}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, internal slow oscillator, and 32 kHz crystal oscillator active. Lower 3/4 temperature range.	–	8	18	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. Vdd = 5.25V, -40 $^oC \le T_A \le$ 55 ^{o}C. Analog power = off.
I_{SBXTLH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and 32 kHz crystal oscillator active. Higher 1/4 temperature range (hot).	–	8	100	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. Vdd = 5.25V, 55 $^oC < T_A \le$ 125 ^{o}C. Analog power = off.
V_{REF}	Reference Voltage (Bandgap)	1.25	1.3	1.35	V	

3.3.2 DC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 3-5: DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	3.5	–	–	V	IOH = 10 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])).
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])).
V_{IL}	Input Low Level	–	–	0.8	V	Vdd = 4.75 to 5.25.
V_{IH}	Input High Level	2.2	–		V	Vdd = 4.75 to 5.25.
V_H	Input Hysterisis	–	110	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 µA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25^{o}C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25^{o}C.

3.3.3 DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block.

Table 3-6: DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Low Power Input Offset Voltage (absolute value) Mid Power Input Offset Voltage (absolute value) High Power	– – –	1.6 1.3 1.2	11 9 8	mV mV mV	Opamp Bias = High.
TCV_{OSOA}	Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	10	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range. All Cases, except highest. Power = High, Opamp Bias = High	0.0 0.5	– –	Vdd Vdd - 0.5	V V	
G_{OLOA}	Open Loop Gain	–	80	–	dB	
$V_{OHIGHOA}$	High Output Voltage Swing (worst case internal load)	Vdd - 0.2	–	–	V	
V_{OLOWOA}	Low Output Voltage Swing (worst case internal load)	–	–	0.2	V	
I_{SOA}	Supply Current (including associated AGND buffer) Power=Low Power=Low, Opamp Bias=High Power=Medium Power=Medium, Opamp Bias=High Power=High Power=High, Opamp Bias=High	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	–	80	–	dB	Vss ≤ VIN ≤ (Vdd - 2.25) or (Vdd - 1.25V) ≤ VIN ≤ Vdd.

3.3.4 DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 3-7: DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	16	mV	
TCV_{OSOB}	Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance	–	1	–	Ω	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 32 ohms to Vdd/2)	0.5 x Vdd + 1.3	–	–	V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 32 ohms to Vdd/2)	–	–	0.5 x Vdd - 1.3	V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	–	64	–	dB	

3.3.5 DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block.

Table 3-8: DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
V_{BG5}	Bandgap Voltage Reference 5V	1.25	1.30	1.35	V
–	AGND = Vdd/2[a] CT Block Power = High	Vdd/2 - 0.02	Vdd/2	Vdd/2 + 0.02	V
–	AGND = 2 x BandGap[a] CT Block Power = High	2.4	2.60	2.8	V
–	AGND = P2[4] (P2[4] = Vdd/2)[a] CT Block Power = High	P2[4] - 0.02	P2[4]	P2[4] + 0.02	V
–	AGND = BandGap[a] CT Block Power = High	1.23	1.3	1.37	V
–	AGND = 1.6 x BandGap[a] CT Block Power = High	1.98	2.08	2.14	V
–	AGND Column to Column Variation (AGND=Vdd/2)[a] CT Block Power = High	- 0.035	0.000	0.035	V
–	RefHi = Vdd/2 + BandGap Ref Control Power = High	Vdd/2 + 1.15	Vdd/2 + 1.30	Vdd/2 + 1.45	V
–	RefHi = 3 x BandGap Ref Control Power = High	3.65	3.9	4.15	V
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V) Ref Control Power = High	P2[6] + 2.4	P2[6] + 2.6	P2[6] + 2.8	V
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2) Ref Control Power = High	P2[4] + 1.24	P2[4] + 1.30	P2[4] + 1.36	V
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V) Ref Control Power = High	P2[4] + P2[6] - 0.1	P2[4] + P2[6]	P2[4] + P2[6] + 0.1	V
–	RefHi = 2 x BandGap Ref Control Power = High	2.4	2.60	2.8	V
–	RefHi = 3.2 x BandGap Ref Control Power = High	3.9	4.16	4.42	V
–	RefLo = Vdd/2 – BandGap Ref Control Power = High	Vdd/2 - 1.45	Vdd/2 - 1.3	Vdd/2 - 1.15	V
–	RefLo = BandGap Ref Control Power = High	1.15	1.30	1.45	V
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V) Ref Control Power = High	2.4 - P2[6]	2.6 - P2[6]	2.8 + P2[6]	V
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2) Ref Control Power = High	P2[4] - 1.45	P2[4] - 1.3	P2[4] - 1.15	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V) Ref Control Power = High	P2[4] - P2[6] - 0.1	P2[4] - P26	P2[4] - P2[6] + 0.1	V

a. AGND tolerance includes the offsets of the local buffer in the PSoC block. BG = Bandgap voltage is 1.3V ± 0.05V.

3.3.6 DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 3-9: DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.24	–	kΩ	
C_{SC}	Capacitor Unit Value (Switch Cap)	–	80	–	fF	

3.3.7 DC POR, and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 3-10: DC POR, and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	Vdd Value for PPOR Trip (positive ramp)					
V_{PPOR1R}	PORLEV[1:0] = 01b	–	4.40	–	V	
V_{PPOR2R}	PORLEV[1:0] = 10b		4.60		V	
	Vdd Value for PPOR Trip (negative ramp)					
V_{PPOR1}	PORLEV[1:0] = 01b	–	4.40	–	V	
V_{PPOR2}	PORLEV[1:0] = 10b		4.60		V	
	PPOR Hysteresis					
V_{PH1}	PORLEV[1:0] = 01b	–	0	–	mV	
V_{PH2}	PORLEV[1:0] = 10b	–	0	–	mV	
	Vdd Value for LVD Trip					
V_{LVD6}	VM[2:0] = 110b	4.70	4.80	4.90	V	
V_{LVD7}	VM[2:0] = 111b	4.80	4.90	5.00	V	

3.3.8 DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 3-11: DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply Current During Programming or Verify	–	15	30	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	3.5	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)[a]	100	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[a,b]	51,200	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention[c]	15	–	–	Years	

a. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

b. A maximum of 512 x 100 block endurance cycles is allowed.

c. Flash data retention based on the use condition of ≤ 7000 hours at T_A ≤ 125°C and the remaining time at T_A ≤ 65°C.

3.4 AC Electrical Characteristics

3.4.1 AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 3-12: AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	Internal Main Oscillator Frequency for 24 MHz	23.04	24	24.96	MHz	Trimmed. Utilizing factory trim values.
F_{CPU1}	CPU Frequency (5V Nominal)	0.09	12	12.48	MHz	
F_{48M}	Digital PSoC Block Frequency	–	–	–	MHz	Not allowed.
F_{24M}	Digital PSoC Block Frequency	0	24	24.96[a]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent.
F_{PLL}	PLL Frequency	–	23.986	–	MHz	Is a multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	–	–	800	ps	
$T_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	
$T_{PLLSLEWSLOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T_{OS}	External Crystal Oscillator Startup to 1%	–	1700	2620	ms	
T_{OSACC}	External Crystal Oscillator Startup to 200 ppm	–	2800	3800	ms	
Jitter32k	32 kHz Period Jitter	–	100		ns	
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Jitter24M1P	24 MHz Period Jitter (IMO) Peak-to-Peak	–	300		ps	
Jitter24M1R	24 MHz Period Jitter (IMO) Root Mean Squared	–	–	600	ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.48	MHz	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

a. See the individual user module data sheets for information on maximum frequencies for user modules.

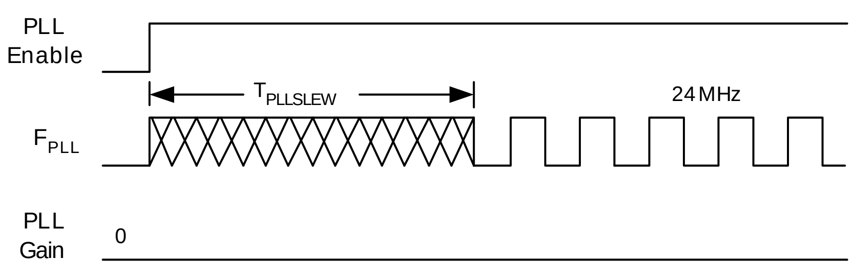


Figure 3-2. PLL Lock Timing Diagram

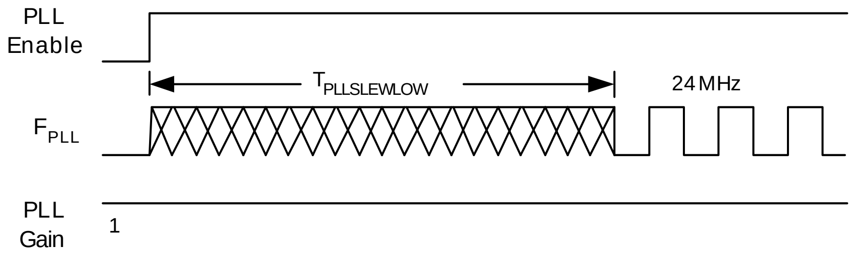


Figure 3-3. PLL Lock for Low Gain Setting Timing Diagram

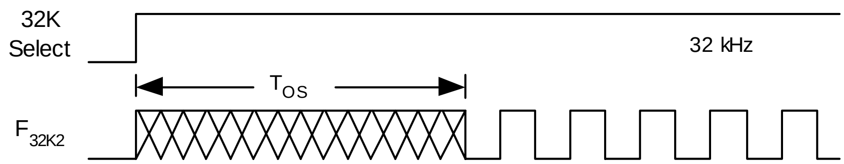


Figure 3-4. External Crystal Oscillator Startup Timing Diagram

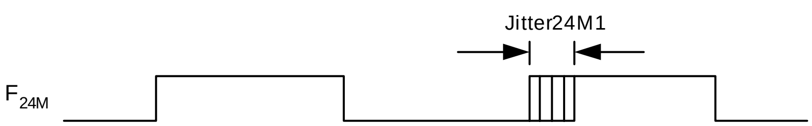


Figure 3-5. 24 MHz Period Jitter (IMO) Timing Diagram

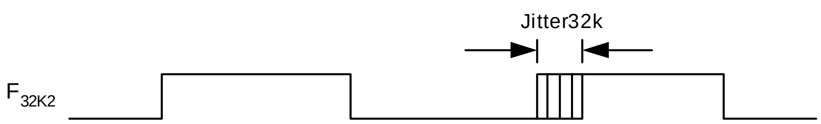


Figure 3-6. 32 kHz Period Jitter (ECO) Timing Diagram

3.4.2 AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 3-13: AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12.48	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	22	ns	Vdd = 4.75 to 5.25V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	22	ns	Vdd = 4.75 to 5.25V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	9	27	–	ns	Vdd = 4.75 to 5.25V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	9	22	–	ns	Vdd = 4.75 to 5.25V, 10% - 90%

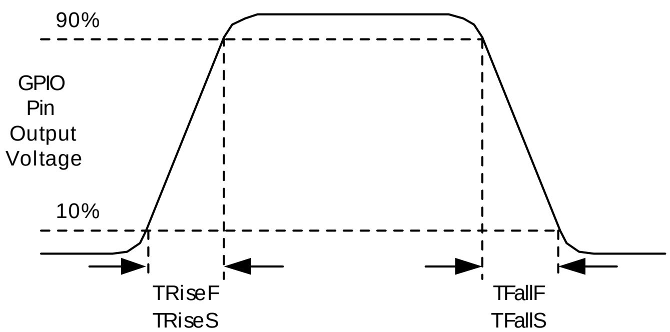


Figure 3-7. GPIO Timing Diagram

3.4.3 AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Table 3-14: AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
SR_{ROA}	Rising Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain)					
	Power = Low	0.15	–		V/µs	
	Power = Low, Opamp Bias = High	0.15			V/µs	
	Power = Medium	0.15			V/µs	
	Power = Medium, Opamp Bias = High	1.7	–		V/µs	
	Power = High	1.7			V/µs	
	Power = High, Opamp Bias = High	6.5	–		V/µs	
SR_{FOA}	Falling Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain)					
	Power = Low	0.01	–		V/µs	
	Power = Low, Opamp Bias = High	0.01			V/µs	
	Power = Medium	0.01			V/µs	
	Power = Medium, Opamp Bias = High	0.5	–		V/µs	
	Power = High	0.5			V/µs	
	Power = High, Opamp Bias = High	4.0	–		V/µs	
BW_{OA}	Gain Bandwidth Product					
	Power = Low	0.75	–		MHz	
	Power = Low, Opamp Bias = High	0.75			MHz	
	Power = Medium	0.75			MHz	
	Power = Medium, Opamp Bias = High	3.1	–		MHz	
	Power = High	3.1			MHz	
	Power = High, Opamp Bias = High	5.4	–		MHz	

When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

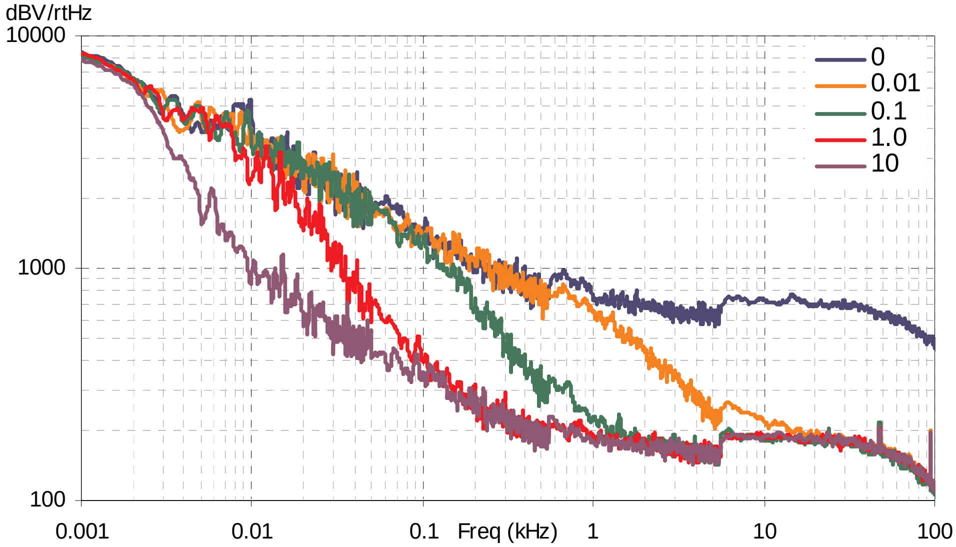


Figure 3-8. Typical AGND Noise with P2[4] Bypass

At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

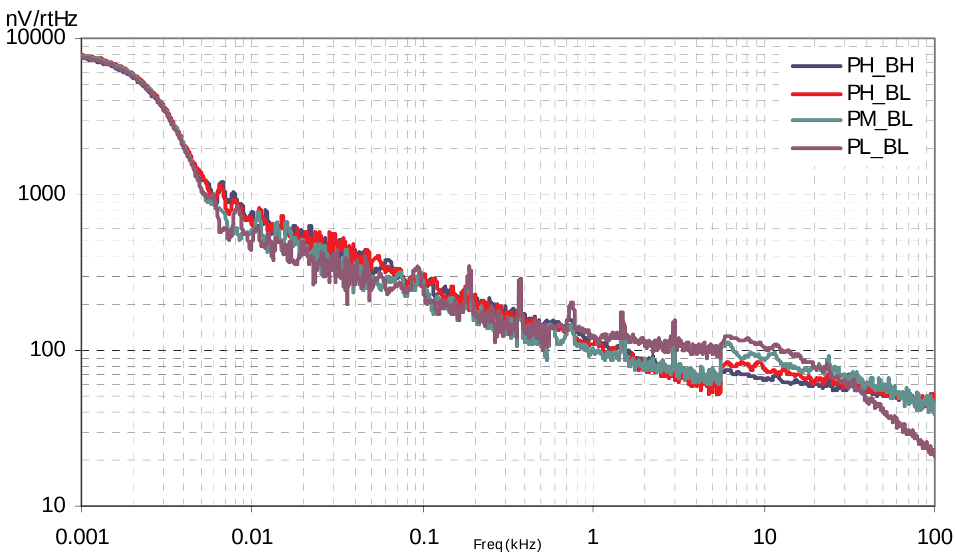


Figure 3-9. Typical Opamp Noise

3.4.4 AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 3-15: AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Maximum Block Clocking Frequency (> 4.75V)			24.96	MHz	4.75V < Vdd < 5.25V.
Timer	Capture Pulse Width	50[a]	–	–	ns	
	Maximum Frequency, No Capture	–	–	24.96	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, With Capture	–	–	24.96	MHz	
Counter	Enable Pulse Width	50[a]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	24.96	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, Enable Input	–	–	24.96	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[a]	–	–	ns	
	Disable Mode	50[a]	–	–	ns	
	Maximum Frequency	–	–	24.96	MHz	4.75V < Vdd < 5.25V.
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	24.96	MHz	4.75V < Vdd < 5.25V.
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.96	MHz	
SPIM	Maximum Input Clock Frequency	–	–	4	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	2	MHz	
	Width of SS_ Negated Between Transmissions	50[a]	–	–	ns	
Transmitter	Maximum Input Clock Frequency	–	–	8	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	–	16	24.96	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.

a. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

3.4.5 AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 3-16: AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	–	–	4	µs	
	Power = High	–	–	4	µs	
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	–	–	4	µs	
	Power = High	–	–	4	µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load					
	Power = Low	0.6	–	–	V/µs	
	Power = High	0.6	–	–	V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load					
	Power = Low	0.6	–	–	V/µs	
	Power = High	0.6	–	–	V/µs	
BW_{OB}	Small Signal Bandwidth, 20mV$_{pp}$, 3dB BW, 100pF Load					
	Power = Low	0.8	–	–	MHz	
	Power = High	0.8	–	–	MHz	
BW_{OB}	Large Signal Bandwidth, 1V$_{pp}$, 3dB BW, 100pF Load					
	Power = Low	300	–	–	kHz	
	Power = High	300	–	–	kHz	

3.4.6 AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 3-17: AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0	–	24.24	MHz	
–	High Period	20.6	–	–	ns	
–	Low Period	20.6	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

3.4.7 AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 3-18: AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	15	–	ms	
T_{WRITE}	Flash Block Write Time	–	30	–	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	

3.4.8 AC I2C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 3-19: AC Characteristics of the I2C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz	
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs	
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs	
$T_{SUSTAI2C}$	Set-up Time for a Repeated START Condition	4.7	–	0.6	–	µs	
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs	
$T_{SUDATI2C}$	Data Set-up Time	250	–	100[a]	–	ns	
$T_{SUSTOI2C}$	Set-up Time for STOP Condition	4.0	–	0.6	–	µs	
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs	
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns	

a. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT}$ ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

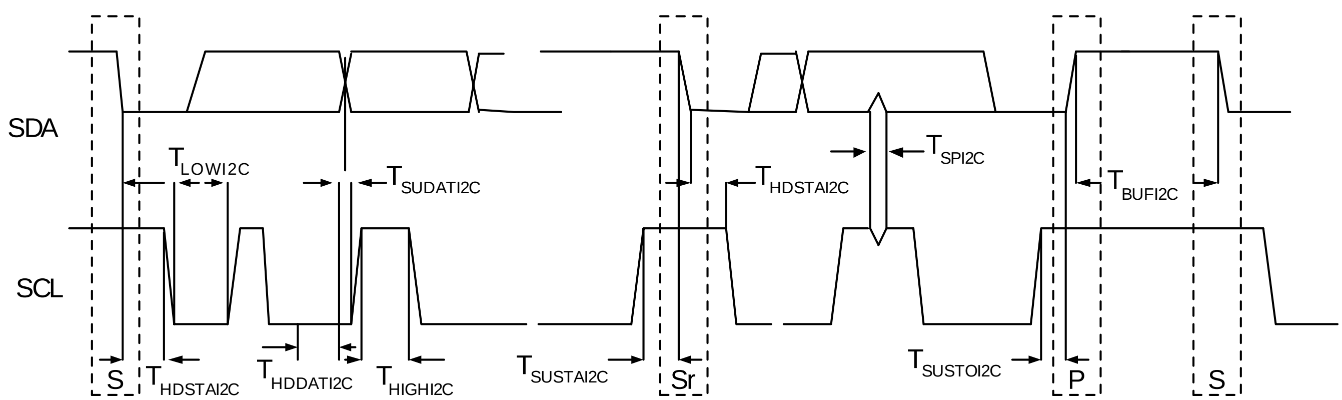


Figure 3-10. Definition for Timing for Fast/Standard Mode on the I2C Bus

4. Packaging Information

This chapter illustrates the packaging specifications for the CY8C29x66 automotive PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/support/link.cfm?mr=poddim.

4.1 Packaging Dimensions

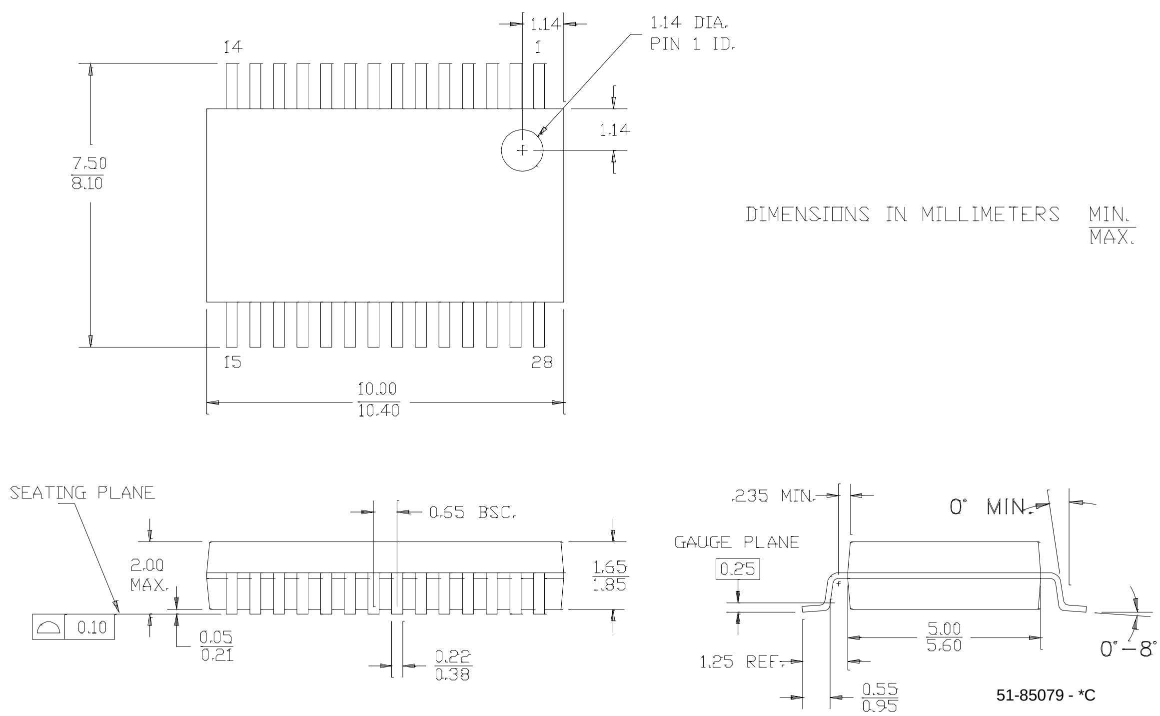


Figure 4-1. 28-Lead (210-Mil) SSOP

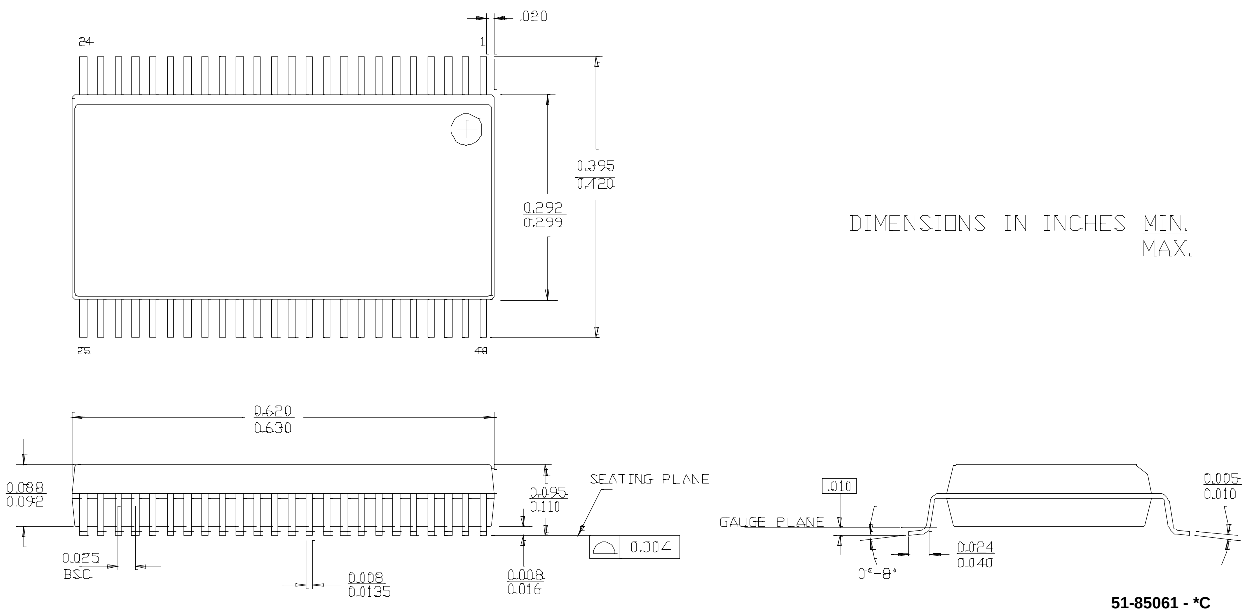


Figure 4-2. 48-Lead (300-Mil) SSOP

4.2 Thermal Impedances

Table 4-1: Thermal Impedances per Package

Package	Typical θ_{JA} *
28 SSOP	95^{o}C/W
48 SSOP	69 ^{o}C/W

* $T_J = T_A$ + POWER x θ_{JA}

4.3 Capacitance on Crystal Pins

Table 4-2: Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
28 SSOP	2.8 pF
48 SSOP	3.3 pF

5. Ordering Information

The following table lists the CY8C29x66 PSoC device's key package features and ordering codes.

Table 5-1: CY8C29x66 Automotive PSoC Key Features and Ordering Information

Package	Ordering Code	Flash (Kbytes)	RAM (Bytes)	Switch Mode Pump	Temperature Range	Digital PSoC Blocks (Rows of 4)	Analog PSoC Blocks (Columns of 3)	Digital IO Pins	Analog Inputs	Analog Outputs	XRES Pin
28 Pin (210 Mil) SSOP	CY8C29466-12PVXE	32	2K	No	-40C to +125C	16	12	24	12	4	Yes
28 Pin (210 Mil) SSOP (Tape and Reel)	CY8C29466-12PVXET	32	2K	No	-40C to +125C	16	12	24	12	4	Yes
48 Pin (300 Mil) SSOP	CY8C29666-12PVXE	32	2K	No	-40C to +125C	16	12	44	12	4	Yes
48 Pin (300 Mil) SSOP (Tape and Reel)	CY8C29666-12PVXET	32	2K	No	-40C to +125C	16	12	44	12	4	Yes

5.1 Ordering Code Definitions

CY 8 C 29 xxx-SPxx

Package Type:
- PX = PDIP Pb Free
- SX = SOIC Pb Free
- PVX = SSOP Pb Free
- LFX = MLF Pb Free
- AX = TQFP Pb Free

Thermal Rating:
- C = Commercial
- I = Industrial
- E = Extended

Speed: 12 MHz

Part Number

Family Code

Technology Code: C = CMOS

Marketing Code: 8 = Cypress MicroSystems

Company ID: CY = Cypress

6. Sales and Service Information

To obtain information about Cypress MicroSystems or PSoC sales and technical support, reference the following information or go to the section titled "Getting Started" on page 4 in this document.

Cypress MicroSystems
2700 162nd Street SW
Building D
Lynnwood, WA 98037

Phone: 800.669.0557
Facsimile: 425.787.4641

Web Sites: Company Information – http://www.cypress.com
Sales – http://www.cypress.com/aboutus/sales_locations.cfm
Technical Support – http://www.cypress.com/support/login.cfm

6.1 Revision History

Table 6-1: CY8C29X66 Automotive Data Sheet Revision History

Document Title: CY8C29466 and CY8C29666 Automotive PSoC Mixed-Signal Array Preliminary Data Sheet				
Document Number: 38-12026				
Revision	**ECN #**	**Issue Date**	**Origin of Change**	**Description of Change**
**	228771	06/01/2004	SFV	First release of the CY8C29x66 automotive PSoC device data sheet.
*A	271452	See ECN	HMT	Update per SFV memo. Input changes from MWR, including removing SMP.
Distribution: External/Public		**Posting**: None		

6.2 Copyrights and Flash Code Protection

Note the following details of the Flash code protection features on Cypress MicroSystems devices:

Cypress MicroSystems products meet the specifications contained in their particular Cypress MicroSystems Data Sheets. Cypress MicroSystems believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress MicroSystems, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress MicroSystems nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Cypress MicroSystems is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress MicroSystems are committed to continuously improving the code protection features of our products.