Hysteretic Boost-Buck (Ćuk) LED Driver IC

Features

- Constant current LED Driver
- Steps input voltage up or down
- Low EMI
- Variable frequency operation
- Internal 75V linear regulator
- Input and output current sensing
- Input current limit
- Enable & PWM dimming
- Ambient temperature rating up to 125°C
- Meets AEC-Q100 requirements

Applications

- Automotive LED Lighting

Reference Documents

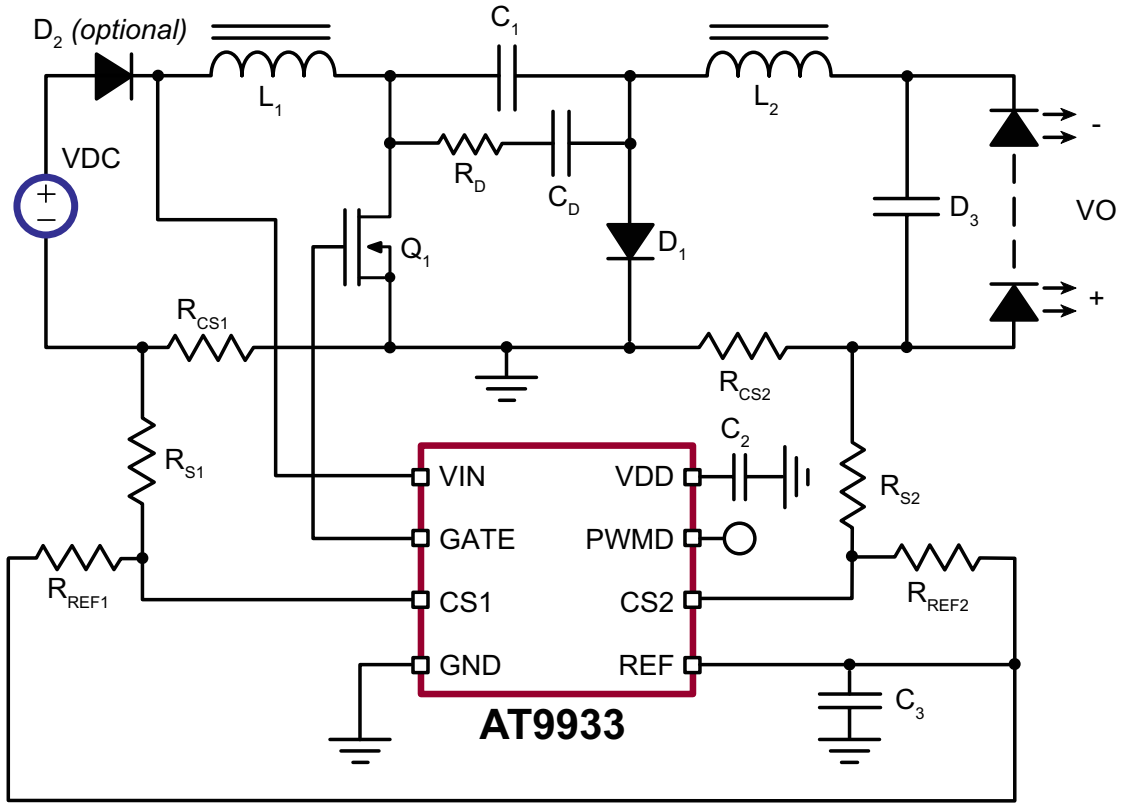
- AEC-Q100 Rev. F, 7/18/2003
- SAE J1752-3

General Description

The AT9933 is a variable frequency PWM controller IC, designed to control an LED lamp driver using a low-noise boost-buck (Ćuk) topology. The AT9933 uses patent-pending hysteretic current-mode control to regulate both the input and the output currents. This enables superior input surge immunity without the necessity for complex loop compensation. Input current control enables current limiting during startup, input under-voltage and output overload conditions. The AT9933 provides a low-frequency PWM dimming input that can accept an external control signal with a duty cycle of 0 - 100% and a high dimming ratio.

The AT9933 based LED driver is ideal for automotive LED lamps. The part is rated for up to 125°C ambient temperatures and is AEC-Q100 compliant.

Typical Application Circuit



Ordering Information

Device	8-Lead SOIC *4.90x3.90mm body* *1.75mm height (max)* *1.27mm pitch*
AT9933	AT9933LG-G

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

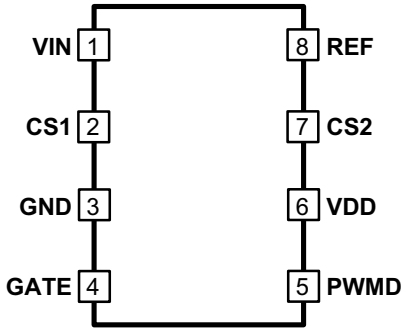
Parameter	Value
V_{IN} to GND	-0.5V to +75V
CS1, CS2, PWMD, GATE to GND	-0.3V to (V_{DD} + 0.3V)
$V_{DD(MAX)}$	12V
Continuous Power Dissipation (T_A = +25°C)	
8-Pin SOIC	700mW
Junction temperature	+150°C
Storage temperature range	-65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Resistance

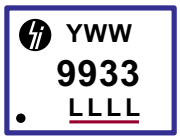
Package	θ_{ja}
8-Lead SOIC	128 °C/W

Pin Configuration



8-Lead SOIC (LG)
(top view)

Product Marking



Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC (LG)

Electrical Characteristics *(Specifications are at T_A = 25°C. V_{IN} = Open, V_{DD} = 7.5V unless otherwise noted)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
Input							
V_{INDC}	Input DC supply voltage range[1]	*	(2)	-	75	V	DC input voltage
I_{INSD}	Shut-down mode supply current[1]	-	-	0.5	1.0	mA	PWMD connected to GND, V_{IN} = 12V
Internal Regulator							
V_{DD}	Internally regulated voltage	*	7.0	7.5	9.0	V	V_{IN} = 8 - 75V, $I_{DD(ext)}$ = 0, 500pF capacitor at GATE, PWMD = GND
UVLO	V_{DD} undervoltage lockout threshold	*	6.35	6.70	7.05	V	V_{DD} rising
ΔUVLO	V_{DD} undervoltage lockout hysteresis	-	-	500	-	mV	---

Notes:

1. *Also limited by package power dissipation limit, whichever is lower.*
2. *Depends on the current drawn by the part - see application section.*

* *Specifications apply over the full operating ambient temperature range of -40°C < T_A < +125°C. Guaranteed by design and characterization.*

Electrical Characteristics *(cont.)(Specifications are at T_A = 25°C. V_{IN} = Open, V_{DD} = 7.5V unless otherwise noted)*

Sym	Description		Min	Typ	Max	Units	Conditions
Reference							
V_{REF}	REF pin voltage 0°C < T_A < +85°C	-	1.212	1.25	1.288	V	REF bypassed with a 0.1µF capacitor to GND, I_{REF} = 0, PWMD = 5.0V
	REF pin voltage -40°C < T_A < 125°C	-	1.187	1.25	1.312		
$V_{REFLINE}$	Line regulation of reference voltage	-	0	-	20	mV	REF bypassed with a 0.1µF capacitor to GND, I_{REF} = 0, V_{DD} = 7.0 - 9.0V, PWMD = 5.0V
I_{REF}	Reference output current range	-	-0.01	-	500	µA	REF bypassed with a 0.1µF capacitor to GND, I_{REF} = 0; V_{DD} = 7.0 - 9.0V, PWMD = 5.0V
$V_{REFLOAD}$	Load regulation of reference voltage	-	0	-	10	mV	REF bypassed with a 0.1µF capacitor to GND, I_{REF} = 0 - 500µA, PWMD = 5.0V
PWM Dimming							
$V_{PWMD(lo)}$	PWMD input low voltage	*	-	-	0.8	V	V_{DD} = 7.0 - 9.0V
$V_{PWMD(hi)}$	PWMD input high voltage	*	2.0	-	-	V	V_{DD} = 7.0 - 9.0V
R_{PWMD}	PWMD pull-down resistance	-	50	100	150	kΩ	V_{PWMD} = 5.0V
GATE							
I_{SOURCE}	GATE short circuit current	-	0.165	-	-	A	V_{GATE} = 0V
I_{SINK}	GATE sinking current	-	0.165	-	-	A	V_{GATE} = V_{DD}
T_{RISE}	GATE output rise time	-	-	30	50	ns	C_{GATE} = 500pF
T_{FALL}	GATE output fall time	-	-	30	50	ns	C_{GATE} = 500pF
Input Current Sense Comparator							
$V_{TURNON1}$	Voltage required to turn GATE on	*	85	100	115	mV	CS2 = 200mV; CS1 increasing; GATE goes LOW to HIGH
$V_{TURNOFF1}$	Voltage required to turn GATE off	*	-15	0	15	mV	CS2 = 200mV; CS1 decreasing; GATE goes HIGH to LOW
$T_{D1,ON}$	Delay to output (turn on)	-	-	150	250	ns	CS2 = 200mV; CS1 = 50mV to +200mV step
$T_{D1,OFF}$	Delay to output (turn off)	-	-	150	250	ns	CS2 = 200mV; CS1 = 50mV to -100mV step
Output Current Sense Comparator							
$V_{TURNON2}$	Voltage required to turn GATE on	*	85	100	115	mV	CS1 = 200mV; CS2 increasing; GATE goes LOW to HIGH
$V_{TURNOFF2}$	Voltage required to turn GATE off	*	-15	0	15	mV	CS1 = 200mV; CS2 decreasing; GATE goes HIGH to LOW
$T_{D2,ON}$	Delay to output (turn on)	-	-	150	250	ns	CS1 = 200mV; CS2 = 50mV to +200mV step
$T_{D2,OFF}$	Delay to output (turn off)	-	-	150	250	ns	CS1 = 200mV; CS2 = 50mV to -100mV step

Notes:

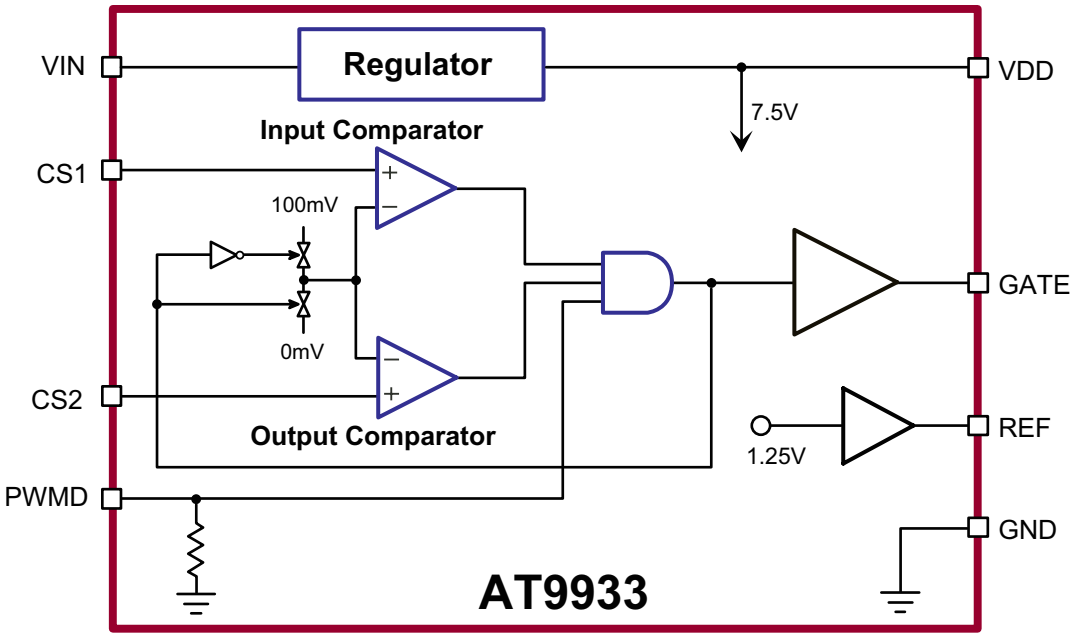
1. *Also limited by package power dissipation limit, whichever is lower.*
2. *Depends on the current drawn by the part - see application section.*

* *Specifications apply over the full operating ambient temperature range of -40ºC < T_A < +125ºC. Guaranteed by design and characterization.*

Pin Description

Pin Number	Name	Description
1	VIN	This pin is the input of a 8.0 - 75V voltage regulator.
2	CS1	These pins are used to sense the input and output currents of the boost-buck converter. They are the non-inverting inputs of the internal comparators.
7	CS2	
3	GND	Ground return for all the internal circuitry. This pin must be electrically connected to the ground of the power train.
4	GATE	This pin is the output gate driver for an external N-channel power MOSFET.
5	PWMD	When this pin is left open or pulled to GND, the gate driver is disabled. Pulling the pin to a voltage greater than 2.0V will enable the gate drive output.
6	VDD	This is a power supply pin for all internal circuits. It must be bypassed to GND with a low ESR capacitor greater than 0.1µF.
8	REF	This pin provides accurate reference voltage. It must be bypassed with a 0.01 - 0.1µF capacitor to GND.

Block Diagram



Functional Description

Power Topology

The AT9933 is optimized to drive a continuous conduction mode (CCM) boost-buck DC/DC converter topology commonly referred to as "Ćuk converter" (see Circuit Diagram on page 1). This power converter topology offers numerous advantages useful for driving high-brightness light emitting diodes (HB LED). These advantages include step-up or step-down voltage conversion ratio and low input and output current ripple. The output load is decoupled from the input voltage with a capacitor making the driver inherently failure-safe for the output load.

The AT9933 offers a simple and effective control technique for use with a boost-buck LED driver. It uses two hysteretic mode controllers – one for the input and one for the output. The outputs of these two hysteretic comparators are AND-ED and used to drive the external FET. This control scheme gives accurate current control and constant output current in the presence of input voltage transients without the need for complicated loop design.

Input Voltage Regulator

The AT9933 can be powered directly from its VIN pin that takes a voltage up to 75V. When a voltage is applied at the VIN pin, the AT9933 seeks to regulate a constant 7.5V (typ) at the VDD pin. The regulator also has a built in under-voltage lockout which shuts off the IC if the voltage at the VDD pin falls below the UVLO threshold.

The VDD pin must be bypassed by a low ESR capacitor (≥0.1µF) to provide a low impedance path for the high frequency current of the output gate driver.

The input current drawn from the V_{IN} pin is a sum of the 1mA current drawn by the internal circuit and the current drawn by the gate driver (which in turn depends on the switching frequency and the gate charge of the external FET).

$$I_{IN} = 1.0mA + Q_G \bullet f_S \qquad (1)$$

In the above equation, f_S is the switching frequency and Q_G is the gate charge of the external FET (which can be obtained from the datasheet of the FET).

Minimum Input Voltage at VIN pin

The minimum input voltage at which the converter will start and stop depends on the minimum voltage drop required for the linear regulator. The internal linear regulator will regulate the voltage at the VDD pin when V_{IN} is between 8.0 and 75V. However, when V_{IN} is less than 8.0V, the converter will still function as long as V_{DD} is greater than the under voltage lockout. Thus, under certain conditions, the converter will be able to start at V_{IN} voltages of less than 8.0V. The start/stop voltages at the VIN pin can be determined using the maximum voltage drop across the linear regulator as a function of the current drawn. This data is shown in Fig. 1 for ambient temperatures of 25ºC and 125ºC.

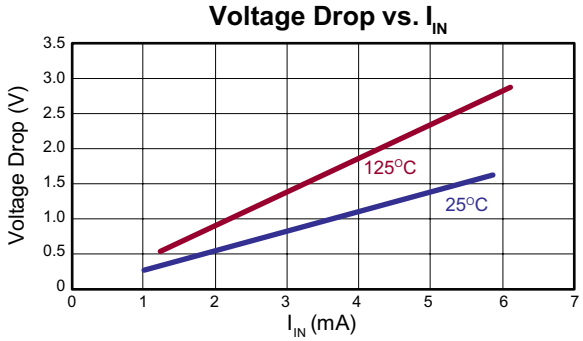


Fig. 1. Maximum Voltage Drop vs. Input Current

Assume an ambient temperature of 125°C. Assuming the IC is driving a 15nC gate charge FET at 300kHz, the total input current is estimated to be 5.5mA (using Eqn. 1). At this input current, the maximum voltage drop from Fig. 1 can be approximately estimated to be V_{DROP} = 2.7V. However, before the IC starts switching the current drawn will be 1.0mA. At this current level, the voltage drop is approximately V_{DROP1} = 0.5V. Thus, the start/stop V_{IN} voltages can be computed to be:

$$V_{IN\text{-}START} = UVLO_{MAX} + V_{DROP1}$$
$$= 6.95V + 0.5V$$
$$= 7.45V$$
$$V_{IN\text{-}STOP} = UVLO_{MAX} - \Delta UVLO + V_{DROP}$$
$$= 6.95 - 0.5V + 2.7V$$
$$= 9.15V$$

Note that in this case, since the gate drive draws too much current, $V_{IN\text{-}START}$ is less than $V_{IN\text{-}STOP}$. In such cases, the control IC will oscillate between on and off if the input voltage is between the start and stop voltages. In these circumstances, it is recommended that the input voltage be kept higher than $V_{IN\text{-}STOP}$ (in this case the IC will operate normally if the input voltage is kept higher than 9.2V).

In case of input transients that reduce the input voltage below 8.0V (like cold crank condition in an automotive system), the VIN pin of the AT9933 can be connected to the drain of the MOSFET through a switching diode with a small (1.0nF) capacitor between VIN and GND (as long as the drain voltage does not exceed 75V). Since the drain of the FET is at a voltage equal to the sum of the input and output voltages, the IC will still be operational when the input goes below 8V. In these cases, a larger capacitor is needed to the VDD pin to supply power to the IC when the MOSFET is on.

In this case $V_{DD\ UVLO}$ cannot be relied upon to turn off the IC at low input voltages when input current levels can get too large. The input current limit must then be designed to limit the input current to safe levels during input undervoltage conditions.

Reference

An internally trimmed voltage reference of 1.25V is provided at the REF pin. The reference can supply a maximum output current of 500µA to drive external resistor dividers.

This reference can be used to set the current thresholds of the two comparators as shown in the Typical Application Circuit.

Current Comparators

The AT9933 features two identical comparators with a built-in 100mV hysteresis. When the GATE is low, the inverting terminal is connected to 100mV and when the GATE is high, it is connected to GND. One comparator is used for the input current control and the other for the output current control.

The input side hysteretic controller is in operation during start-up, overload and input undervoltage conditions. This ensures that the input current never exceeds the designed value. During normal operation, the input current will be less than the programmed current and hence, the output of the input side comparator will be HIGH. The output of the AND gate will then be dictated by the output current controller.

The output side hysteretic comparator will be in operation during the steady state operation of the circuit. This comparator turns the MOSFET on and off based on the LED current.

PWM Dimming

PWM Dimming can be achieved by applying a TTL-compatible square wave signal at the PWM pin. When the PWMD pin is pulled high, the gate driver is enabled and the circuit operates normally. When the PWMD pin is left open or connected to GND, the gate driver is disabled and the external MOSFET turns off. The IC is designed so that the signal at the PWMD pin inhibits the driver only and the IC need not go through the entire start-up cycle each time ensuring a quick response time for the output current. The recommended PWM Dimming frequency range is from 100Hz to a few kilo hertz.

The flying capacitor in the Ćuk converter (C1) is initially charged to the input voltage VDC (through diodes D_1 and D_2). When the circuit is turned on and reaches steady state, the voltage across C_1 will be VDC+VO. In the absence of diode D_2, when the circuit is turned off, capacitor C_1 will discharge through the LEDs and the input voltage source VDC. Thus, during PWM dimming, if capacitor C_1 has to be charged and discharged each cycle, the transient response of the circuit will be limited. By adding diode D_2, the voltage across capacitor C_1 is held at VDC+VO even when the circuit is turned off enabling the circuit to return quickly to its steady state (and bypassing the start-up stage) upon being enabled.

Application Information

Over-voltage Protection

Over-voltage protection can be added by splitting the output side resistor R_{S2} into two components and adding a zener diode D_3 (see the Design Example Circuit on the following page). When there is an open LED condition, the diode D_3 will clamp the output voltage and the zener diode current will be regulated by the sum of R_{S2A} and R_{CS2}.

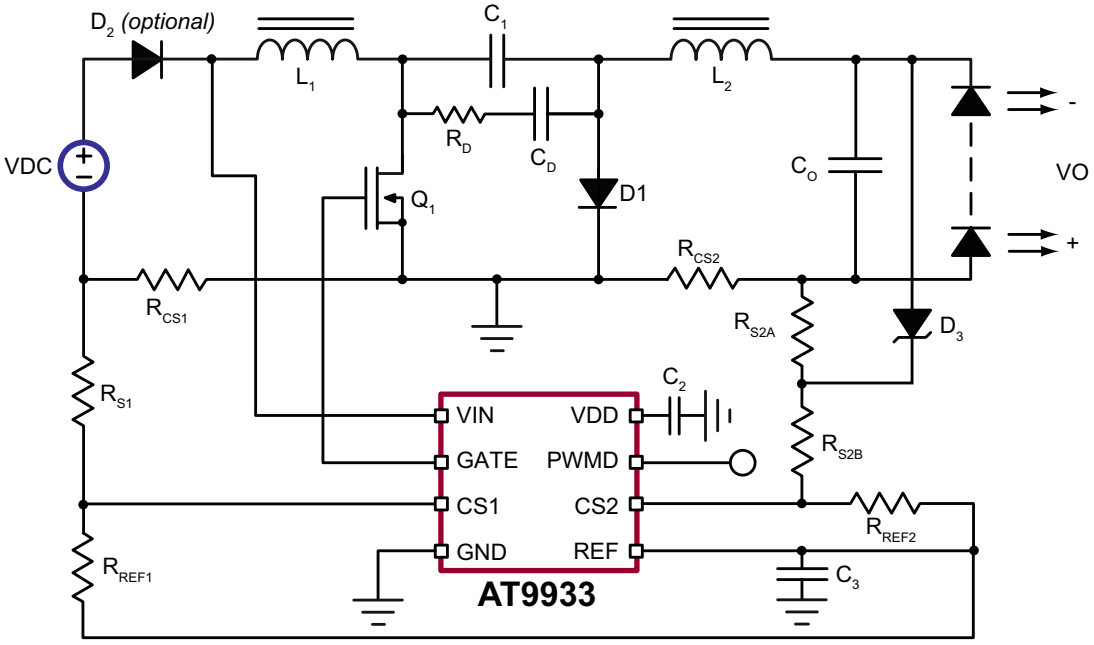
Damping Circuit

The Ćuk converter is inherently unstable when the output current is being controlled. An uncontrolled input current will lead to an un-damped oscillation between L_1 and C_1 causing excessively high voltages across C_1. To prevent these oscillations, a damping circuit consisting of R_D and C_D is applied across the capacitor C_1. This damping circuit will stabilize the circuit and help in the proper operation of the AT9933 based Ćuk converter.

Design and Operation of the Boost-Buck Converter

For details on the design for a Boost-Buck converter using the AT9933 and the calculation of the damping components, please refer to Application Note AN-H51 and AN-H58.

Design Example Circuit



Design Example

The choice of the resistor dividers to set the input and output current levels is illustrated by means of the design example given below.

The parameters of the power circuit are:

$V_{IN\ MIN}$ = 9.01V
$V_{IN\ MAX}$ = 16V
V_O = 28V
I_O = 0.35A
$f_{S\ MIN}$ = 300kHz

Using these parameters, the values of the power stage inductors and capacitor can be computed as (see Application Note AN-H51 for details):

L1 = 82µH
L2 = 150µH
C1 = 0.22µF

The input and output currents for this design are:

$I_{IN\ MAX}$ = 1.6A
ΔI_{IN} = 0.21A
I_O = 350mA
ΔI_O = 87.5mA

Current Limits

The current sense resistor (R_{CS2}), combined with the other resistors (R_{S2} & R_{REF2}), determines the output current limits.

The current sense resistor (R_{CS1}), combined with the other resistors (R_{S1} & R_{REF1}), determines the input current limits.

The resistors can be chosen using the following equations:

$$I \times R_{CS} = 1.2V \times (R_S / R_{REF}) - 0.05V \qquad (2)$$

$$\Delta I \times R_{CS} = 0.1V \times (R_S / R_{REF}) + 0.1V \qquad (3)$$

Where I is the current (either I_O or I_{IN}) and ΔI is the peak-to-peak ripple in the current (either ΔI_O or ΔI_{IN}).

For the input side, the current level used in the equations should be larger than the maximum input current so that it does not interfere with the normal operation of the circuit. The peak input current can be computed as:

$$I_{IN,PK} = I_{IN,MAX} + (\Delta I_{IN} / 2)$$

$$= 1.706A \qquad (4)$$

Assuming a 30% peak-to-peak ripple when the converter is in input current limit mode, the minimum value of the input current will be:

$$I_{LIM,MIN} = 0.85 \bullet I_{IN,LIM} \quad (5)$$

Setting

$$I_{LIM,MIN} = 1.05 \bullet I_{IN,PK} \quad (6)$$

The current level to limit the converter can then be computed.

$$I_{IN,LIM} = (1.05 / 0.85)\ X\ I_{IN,PK}$$

$$= 2.1A \quad (7)$$

Using $I_O = 350mA$ and $\Delta I_O = 87.5mA$ in (1) and (2),

$$R_{CS2} = 1.78\Omega$$

$$R_{S2} / R_{REF2} = 0.5625$$

Before the design of the output side is complete, over voltage protection has to be included in the design. For this application, choose a 33V zener diode. This is the voltage at which the output will clamp in case of an open LED condition. For a 350mW diode, the maximum current rating at 33V works out to about 10mA. Using a 2.5mA current level during open LED conditions, and assuming the same R_{S2}/R_{REF2} ratio,

$$R_{CS2} + R_{S2A} = 120\Omega \quad (8)$$

Choose the following values for the resistors:

$R_{CS2} = 1.65\Omega$, 1/4W, 1%
$R_{REF2} = 10k\Omega$, 1/8W, 1%
$R_{S2A} = 100\Omega$, 1/8W, 1%
$R_{S2B} = 5.23k\Omega$, 1/8W, 1%

The current sense resistor needs to be at least a 1/4W, 1% resistor.

Similarly, using $I_{IN} = 2.1A$ and $\Delta I_{IN} = 0.3xI_{IN} = 0.63$ in (1) and (2):

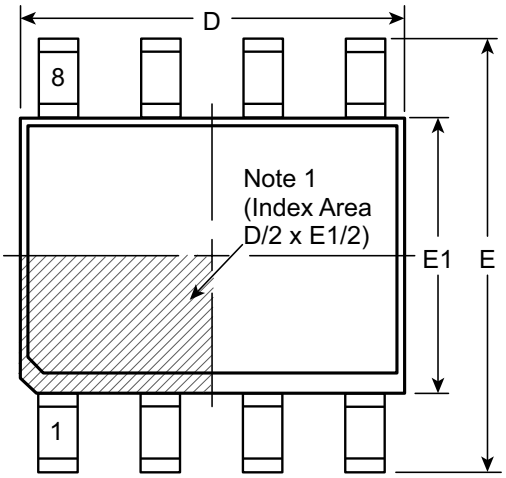
$$R_{S1} / R_{REF1} = 0.442$$
$$R_{CS1} = 0.228\Omega$$
$$P_{RCS1} = I^2_{IN,LIM} \bullet R_{CS1} = 1W$$

Choose the following values for the resistors:

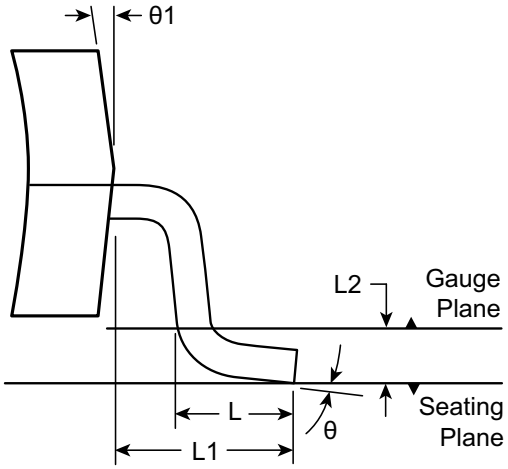
R_{CS1} = parallel combination of three 0.68Ω, 1/2W, 5% resistors
$R_{REF1} = 10k\Omega$, 1/8W, 1%
$R_{S1} = 4.42k\Omega$, 1/8W, 1%

8-Lead SOIC (Narrow Body) Package Outline (LG)

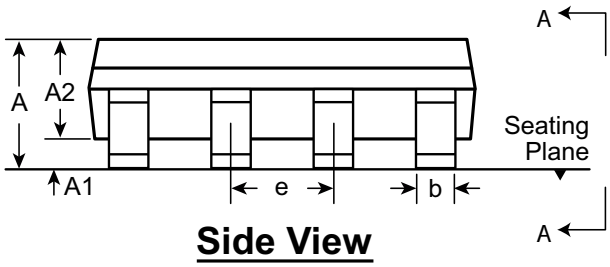
4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



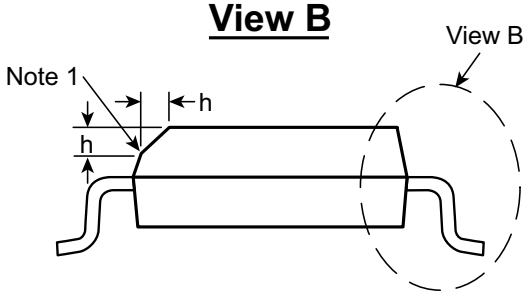
Top View



View B



Side View



View A-A

Note:

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
***Supertex Doc. #:** DSPD-8SOLGTG, Version I041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
Tel: 408-222-8888
www.supertex.com