

## Low Quiescent Current Dual Output LDO

### Features

- Dual Output LDO:
  - $V_{OUT1} = 1.5V$  to  $3.3V$  @  $300\text{ mA}$
  - $V_{OUT2} = 1.5V$  to  $3.3V$  @  $150\text{ mA}$
- Output Voltage (See Table 8-1)
- Low Dropout Voltage:
  - $V_{OUT1} = 104\text{ mV}$  @  $300\text{ mA}$  Typical
  - $V_{OUT2} = 150\text{ mV}$  @  $150\text{ mA}$  Typical
- Low Supply Current:  $116\text{ }\mu\text{A}$  Typical  
TC1302A/B with both output voltages available
- Reference Bypass Input for Low-Noise Operation
- Both Output Voltages Stable with a Minimum of  $1\text{ }\mu\text{F}$  Ceramic Output Capacitor
- Separate  $V_{OUT1}$  and  $V_{OUT2}$   $\overline{\text{SHDN}}$  pins (**TC1302B**)
- Power-Saving Shutdown Mode of Operation
- Wake-up from  $\overline{\text{SHDN}}$ :  $5.3\text{ }\mu\text{s}$ . Typical
- Small 8-pin DFN or MSOP Package Options
- Operating Junction Temperature Range:
  - $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Overtemperature and Overcurrent Protection

### Applications

- Cellular/GSM/PHS Phones
- Battery-Operated Systems
- Hand-Held Medical Instruments
- Portable Computers/PDAs
- Linear Post-Regulators for SMPS
- Pagers

### Related Literature

- AN765, "Using Microchip's Micropower LDOs", DS00765, Microchip Technology Inc., 2002
- AN766, "Pin-Compatible CMOS Upgrades to BiPolar LDOs", DS00766, Microchip Technology Inc., 2002
- AN792, "A Method to Determine How Much Power a SOT23 Can Dissipate in an Application", DS00792, Microchip Technology Inc., 2001

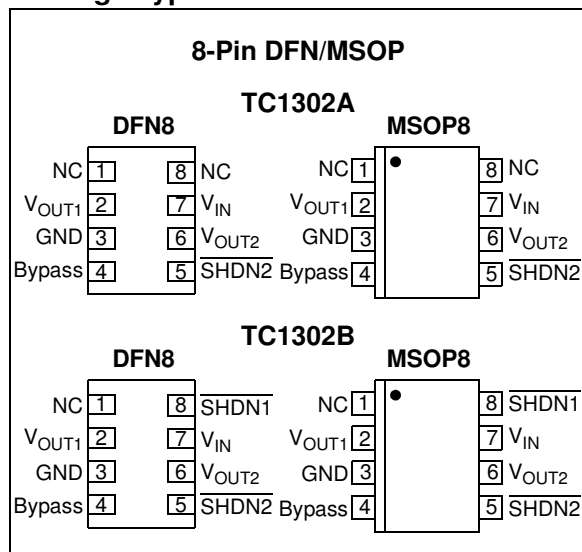
### Description

The TC1302A/B combines two Low Dropout (LDO) regulators into a single 8-pin MSOP or DFN package. Both regulator outputs feature low dropout voltage,  $104\text{ mV}$  @  $300\text{ mA}$  for  $V_{OUT1}$ ,  $150\text{ mV}$  @  $150\text{ mA}$  for  $V_{OUT2}$ , low quiescent current consumption,  $58\text{ }\mu\text{A}$  each and a typical regulation accuracy of  $0.5\%$ . Several fixed-output voltage combinations are available. A reference bypass pin is available to further reduce output noise and improve the power supply rejection ratio of both LDOs.

The TC1302A/B is stable over all line and load conditions, with a minimum of  $1\text{ }\mu\text{F}$  of ceramic output capacitance, and utilizes a unique compensation scheme to provide fast dynamic response to sudden line voltage and load current changes.

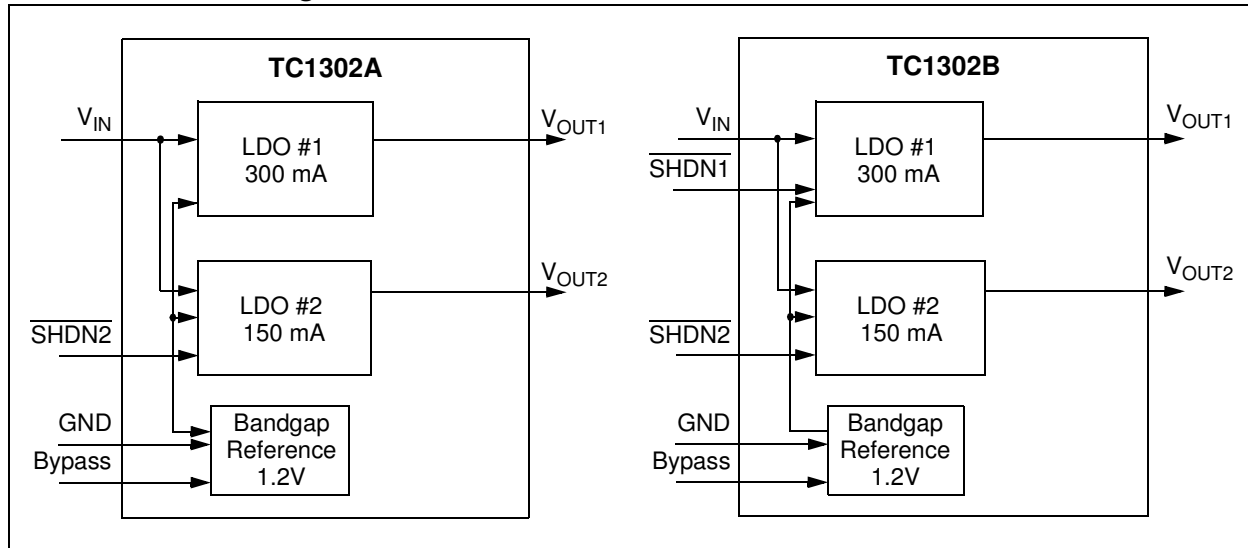
Additional features include an overcurrent limit and overtemperature protection that combine to provide a robust design for all load fault conditions.

### Package Types

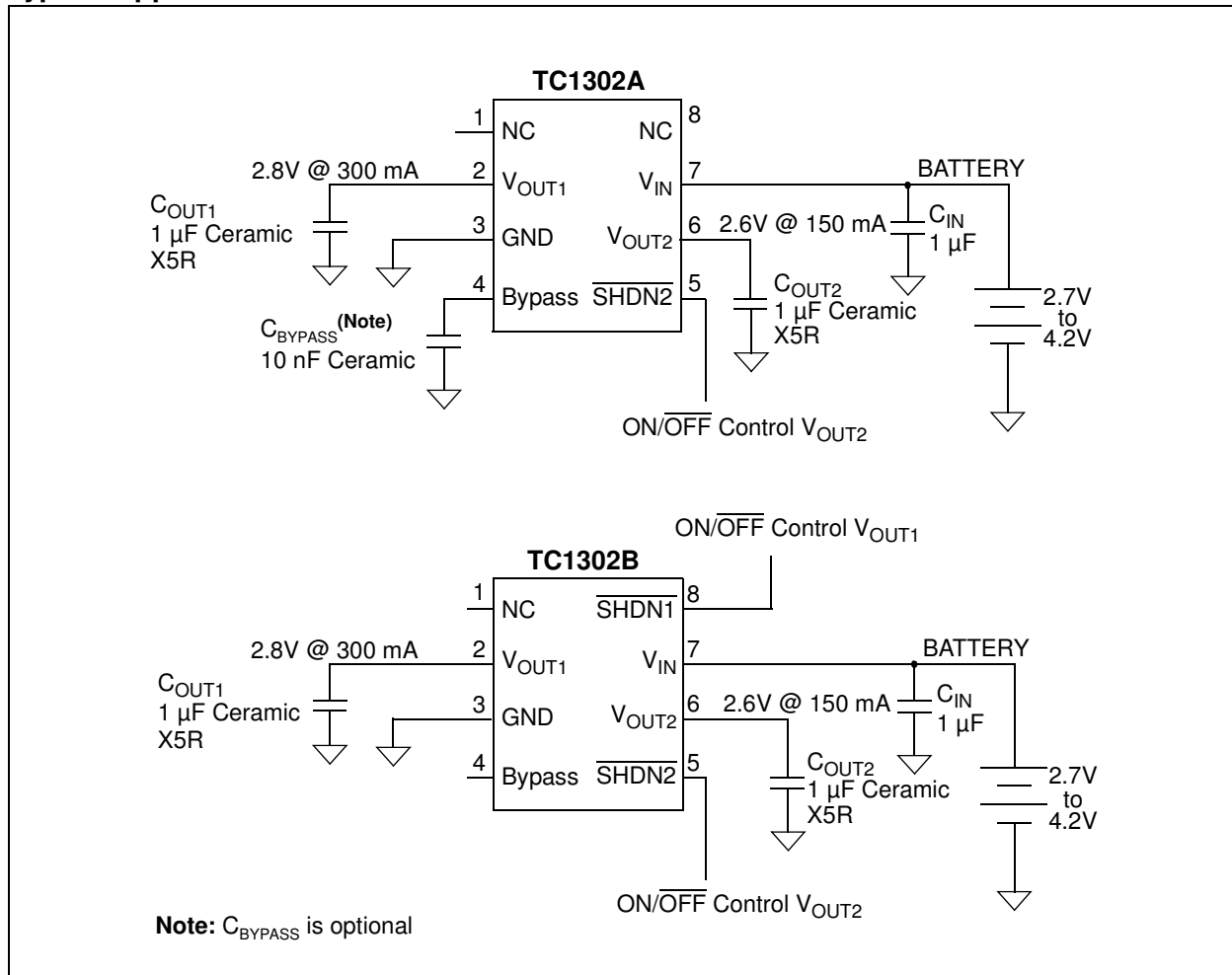


# TC1302A/B

## Functional Block Diagrams



## Typical Application Circuits



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

V <sub>DD</sub> .....	6.5V
Maximum Voltage on Any Pin .....	(V <sub>SS</sub> – 0.3) to (V <sub>IN</sub> + 0.3)V
Power Dissipation .....	Internally Limited ( <b>Note 7</b> )
Storage temperature .....	-65°C to +150°C
Maximum Junction Temperature, T <sub>J</sub> .....	+150°C
Continuous Operating Temperature Range ..	-40°C to +125°C
ESD protection on all pins, HBM, MM.....	4 kV, 400V

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### DC CHARACTERISTICS

**Electrical Specifications:** Unless otherwise noted, V<sub>IN</sub> = V<sub>R</sub> + 1V, I<sub>OUT1</sub> = I<sub>OUT2</sub> = 100 μA, C<sub>IN</sub> = 4.7 μF, C<sub>OUT1</sub> = C<sub>OUT2</sub> = 1 μF, C<sub>BYPASS</sub> = 10 nF, SHDN > V<sub>IH</sub>, T<sub>A</sub> = +25°C.  
**Boldface** type specifications apply for junction temperatures of -40°C to +125°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Operating Voltage	V <sub>IN</sub>	<b>2.7</b>	—	<b>6.0</b>	V	<b>Note 1</b>
Maximum Output Current	I <sub>OUT1Max</sub>	<b>300</b>	—	—	mA	V <sub>IN</sub> = 2.7V to 6.0V ( <b>Note 1</b> )
Maximum Output Current	I <sub>OUT2Max</sub>	<b>150</b>	—	—	mA	V <sub>IN</sub> = 2.7V to 6.0V ( <b>Note 1</b> )
Output Voltage Tolerance (V <sub>OUT1</sub> and V <sub>OUT2</sub> )	V <sub>OUT</sub>	<b>V<sub>R</sub> – 2.5</b>	V <sub>R</sub> ±0.5	<b>V<sub>R</sub> + 2.5</b>	%	<b>Note 2</b>
Temperature Coefficient (V <sub>OUT1</sub> and V <sub>OUT2</sub> )	TCV <sub>OUT</sub>	—	25	—	ppm/°C	<b>Note 3</b>
Line Regulation (V <sub>OUT1</sub> and V <sub>OUT2</sub> )	ΔV <sub>OUT</sub> /ΔV <sub>IN</sub>	—	0.02	<b>0.2</b>	%/V	(V <sub>R</sub> + 1V) ≤ V <sub>IN</sub> ≤ 6V
Load Regulation, V <sub>OUT</sub> ≥ 2.5V (V <sub>OUT1</sub> and V <sub>OUT2</sub> )	ΔV <sub>OUT</sub> /V <sub>OUT</sub>	<b>-1</b>	0.1	<b>+1</b>	%	I <sub>OUTX</sub> = 0.1 mA to I <sub>OUTMax</sub> ; ( <b>Note 4</b> )
Load Regulation, V <sub>OUT</sub> < 2.5V (V <sub>OUT1</sub> and V <sub>OUT2</sub> )	ΔV <sub>OUT</sub> /V <sub>OUT</sub>	<b>-1.5</b>	0.1	<b>+1.5</b>	%	I <sub>OUTX</sub> = 0.1 mA to I <sub>OUTMax</sub> ; ( <b>Note 4</b> )
Thermal Regulation	ΔV <sub>OUT</sub> /ΔP <sub>D</sub>	—	0.04	—	%/W	<b>Note 5</b>
<b>Dropout Voltage (Note 6)</b>						
V <sub>OUT1</sub> > 2.7V	V <sub>IN</sub> – V <sub>OUT</sub>	—	104	<b>180</b>	mV	I <sub>OUT1</sub> = 300 mA
V <sub>OUT2</sub> > 2.6V	V <sub>IN</sub> – V <sub>OUT</sub>	—	150	<b>250</b>	mV	I <sub>OUT2</sub> = 150 mA
<b>Supply Current</b>						
<b>TC1302A</b>	I <sub>IN(A)</sub>	—	103	<b>180</b>	μA	SHDN2 = V <sub>IN</sub> , I <sub>OUT1</sub> = I <sub>OUT2</sub> = 0 mA
<b>TC1302B</b>	I <sub>IN(B)</sub>	—	114	<b>180</b>	μA	SHDN1 = SHDN2 = V <sub>IN</sub> , I <sub>OUT1</sub> = I <sub>OUT2</sub> = 0 mA

- Note 1:** The minimum V<sub>IN</sub> has to meet two conditions: V<sub>IN</sub> ≥ 2.7V and V<sub>IN</sub> ≥ V<sub>R</sub> + V<sub>DROPOUT</sub>.  
**Note 2:** V<sub>R</sub> is defined as the higher of the two regulator nominal output voltages (V<sub>OUT1</sub> or V<sub>OUT2</sub>).  
**Note 3:** TCV<sub>OUT</sub> = ((V<sub>OUTmax</sub> - V<sub>OUTmin</sub>) \* 10<sup>6</sup>)/(V<sub>OUT</sub> \* ΔT).  
**Note 4:** Regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 0.1 mA to the maximum specified output current. Changes in output voltage due to heating effects are covered by the thermal regulation specification.  
**Note 5:** Thermal regulation is defined as the change in output voltage at a time t after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a current pulse equal to I<sub>LMAX</sub> at V<sub>IN</sub> = 6V for t = 10 msec.  
**Note 6:** Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its value measured at a 1V differential.  
**Note 7:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T<sub>A</sub>, T<sub>J</sub>, θ<sub>JA</sub>). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown.

# TC1302A/B

## DC CHARACTERISTICS (Continued)

**Electrical Specifications:** Unless otherwise noted,  $V_{IN} = V_R + 1V$ ,  $I_{OUT1} = I_{OUT2} = 100 \mu A$ ,  $C_{IN} = 4.7 \mu F$ ,  $C_{OUT1} = C_{OUT2} = 1 \mu F$ ,  $C_{BYPASS} = 10 nF$ ,  $\overline{SHDN} > V_{IH}$ ,  $T_A = +25^\circ C$ .  
**Boldface** type specifications apply for junction temperatures of  $-40^\circ C$  to  $+125^\circ C$ .

Parameters	Sym	Min	Typ	Max	Units	Conditions
Shutdown Supply Current <b>TC1302A</b>	$I_{IN\_SHDNA}$	—	58	<b>90</b>	$\mu A$	$\overline{SHDN2} = GND$
Shutdown Supply Current <b>TC1302B</b>	$I_{IN\_SHDNB}$	—	0.1	1	$\mu A$	$\overline{SHDN1} = \overline{SHDN2} = GND$
Power Supply Rejection Ratio	PSRR	—	58	—	dB	$f \leq 100 Hz$ , $I_{OUT1} = I_{OUT2} = 50 mA$ , $C_{IN} = 0 \mu F$
Output Noise	eN	—	830	—	$nV/(Hz)^{1/2}$	$f \leq 1 kHz$ , $I_{OUT1} = I_{OUT2} = 50 mA$ , $C_{IN} = 0 \mu F$
<b>Output Short Circuit Current (Average)</b>						
$V_{OUT1}$	$I_{OUTsc1}$	—	200	—	mA	$R_{LOAD1} \leq 1 \Omega$
$V_{OUT2}$	$I_{OUTsc2}$	—	140	—	mA	$R_{LOAD2} \leq 1 \Omega$
SHDN Input High Threshold	$V_{IH}$	<b>45</b>	—	—	$\%V_{IN}$	$V_{IN} = 2.7V$ to $6.0V$
SHDN Input Low Threshold	$V_{IL}$	—	—	<b>15</b>	$\%V_{IN}$	$V_{IN} = 2.7V$ to $6.0V$
Wake Up Time (From SHDN mode), ( $V_{OUT2}$ )	$t_{WK}$	—	5.3	20	$\mu s$	$V_{IN} = 5V$ , $I_{OUT1} = I_{OUT2} = 30 mA$ , <b>See Figure 5-1</b>
Settling Time (From SHDN mode), ( $V_{OUT2}$ )	$t_S$	—	50	—	$\mu s$	$V_{IN} = 5V$ , $I_{OUT1} = I_{OUT2} = 50 mA$ , <b>See Figure 5-2</b>
Thermal Shutdown Die Temperature	$T_{SD}$	—	150	—	$^\circ C$	$V_{IN} = 5V$ , $I_{OUT1} = I_{OUT2} = 100 \mu A$
Thermal Shutdown Hysteresis	$T_{HYS}$	—	10	—	$^\circ C$	$V_{IN} = 5V$

- Note**
- 1: The minimum  $V_{IN}$  has to meet two conditions:  $V_{IN} \geq 2.7V$  and  $V_{IN} \geq V_R + V_{DROPOUT}$ .
  - 2:  $V_R$  is defined as the higher of the two regulator nominal output voltages ( $V_{OUT1}$  or  $V_{OUT2}$ ).
  - 3:  $TCV_{OUT} = ((V_{OUTmax} - V_{OUTmin}) * 10^6) / (V_{OUT} * \Delta T)$ .
  - 4: Regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 0.1 mA to the maximum specified output current. Changes in output voltage due to heating effects are covered by the thermal regulation specification.
  - 5: Thermal regulation is defined as the change in output voltage at a time  $t$  after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a current pulse equal to  $I_{LMAX}$  at  $V_{IN} = 6V$  for  $t = 10 msec$ .
  - 6: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its value measured at a 1V differential.
  - 7: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e.,  $T_A$ ,  $T_J$ ,  $\theta_{JA}$ ). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown.

## TEMPERATURE SPECIFICATIONS

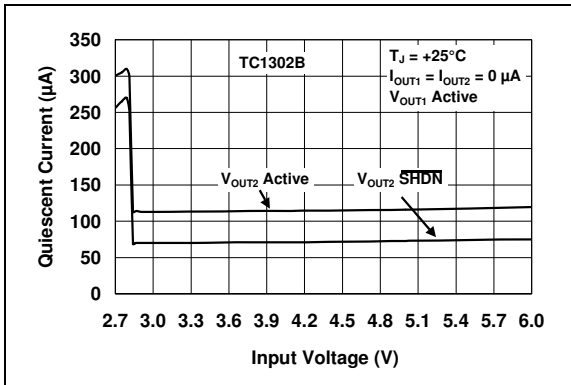
**Electrical Specifications:** Unless otherwise indicated, all limits are specified for:  $V_{IN} = +2.7V$  to  $+6.0V$ .

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Temperature Ranges</b>						
Operating Junction Temperature Range	$T_A$	-40	—	+125	$^\circ C$	Steady State
Storage Temperature Range	$T_A$	-65	—	+150	$^\circ C$	
Maximum Junction Temperature	$T_J$	—	—	+150	$^\circ C$	Transient
<b>Thermal Package Resistances</b>						
Thermal Resistance, MSOP8	$\theta_{JA}$	—	208	—	$^\circ C/W$	Typical 4-Layer Board
Thermal Resistance, DFN8	$\theta_{JA}$	—	41	—	$^\circ C/W$	Typical 4-Layer Board with Vias

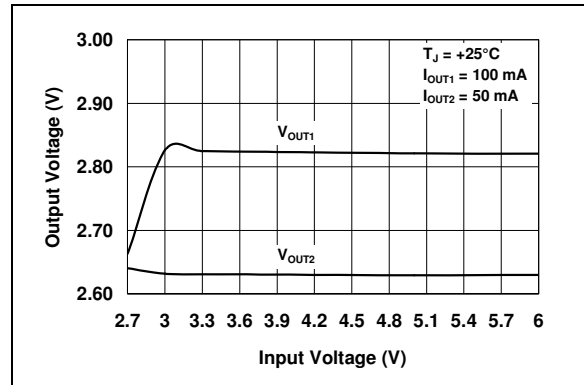
## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

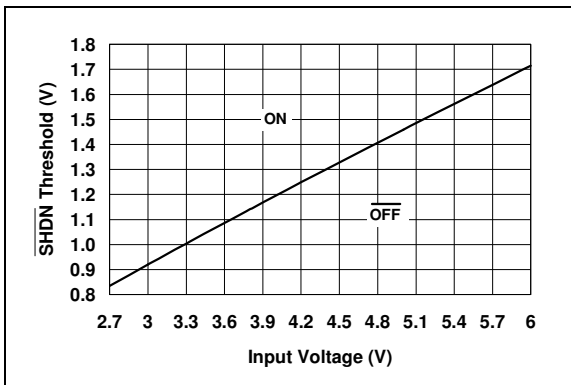
**Note:** Unless otherwise indicated,  $V_{IN} = V_R + 1V$ ,  $I_{OUT1} = I_{OUT2} = 100 \mu A$ ,  $C_{IN} = 4.7 \mu F$ ,  $C_{OUT1} = C_{OUT2} = 1 \mu F$  (X5R or X7R),  $C_{BYPASS} = 0 pF$ ,  $\overline{SHDN1} = \overline{SHDN2} > V_{IH}$ ,  $T_A = +25^\circ C$ .



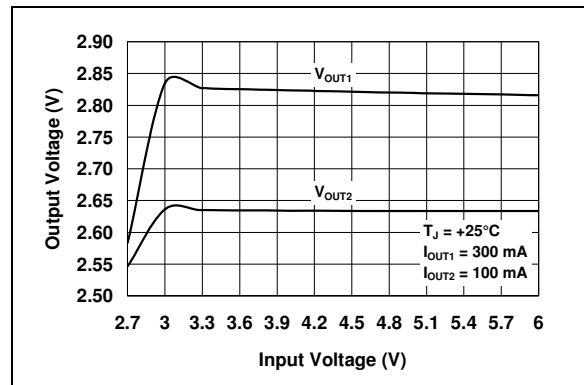
**FIGURE 2-1:** Quiescent Current vs. Input Voltage.



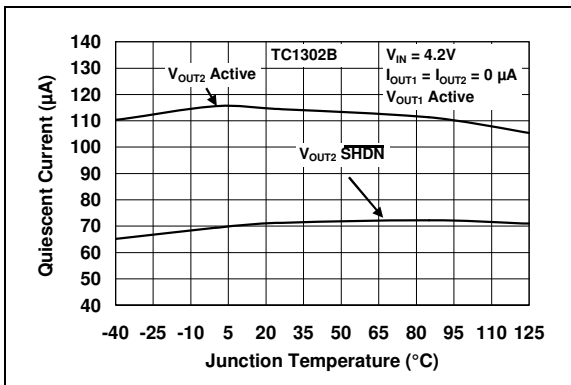
**FIGURE 2-4:** Output Voltage vs. Input Voltage.



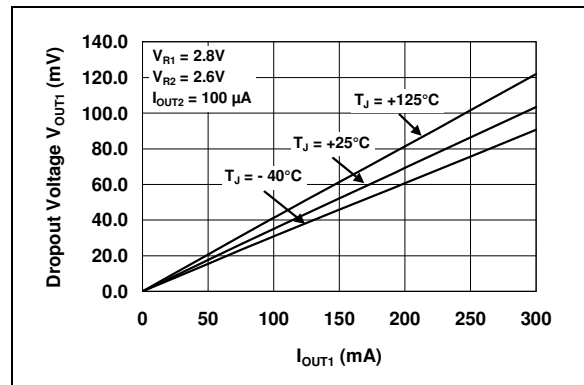
**FIGURE 2-2:**  $\overline{SHDN}$  Voltage Threshold vs. Input Voltage.



**FIGURE 2-5:** Output Voltage vs. Input Voltage.



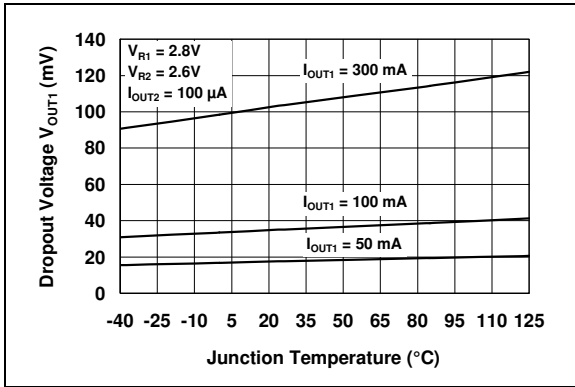
**FIGURE 2-3:** Quiescent Current vs. Junction Temperature.



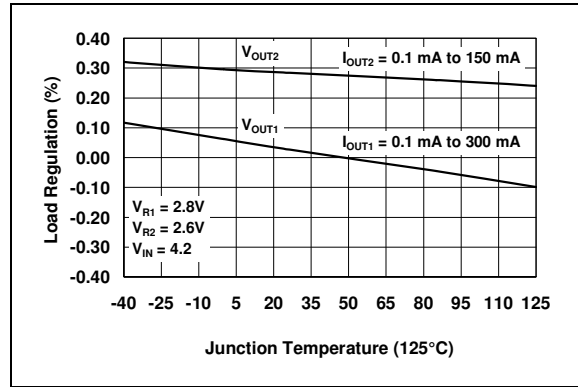
**FIGURE 2-6:** Dropout Voltage vs. Output Current ( $V_{OUT1}$ ).

# TC1302A/B

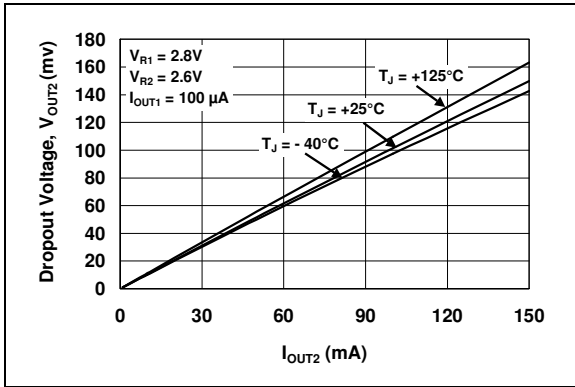
**Note:** Unless otherwise indicated,  $V_{IN} = V_R + 1V$ ,  $I_{OUT1} = I_{OUT2} = 100 \mu A$ ,  $C_{IN} = 4.7 \mu F$ ,  $C_{OUT1} = C_{OUT2} = 1 \mu F$  (X5R or X7R),  $C_{BYPASS} = 0 pF$ ,  $\overline{SHDN1} = \overline{SHDN2} > V_{IH}$ ,  $T_A = +25^\circ C$ .



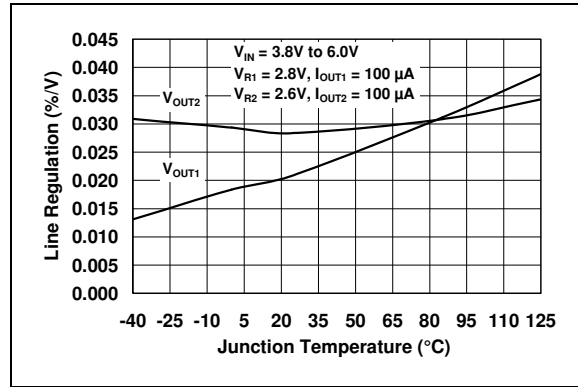
**FIGURE 2-7:** Dropout Voltage vs. Junction Temperature ( $V_{OUT1}$ ).



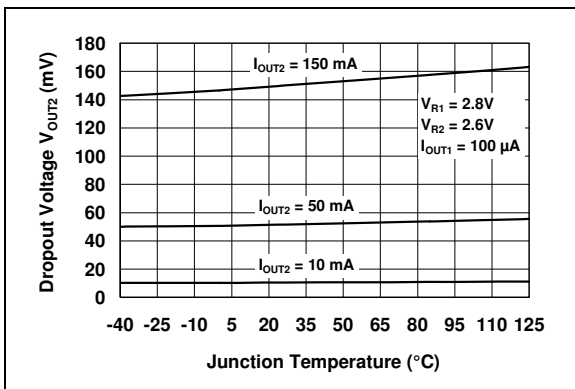
**FIGURE 2-10:**  $V_{OUT1}$  and  $V_{OUT2}$  Load Regulation vs. Junction Temperature.



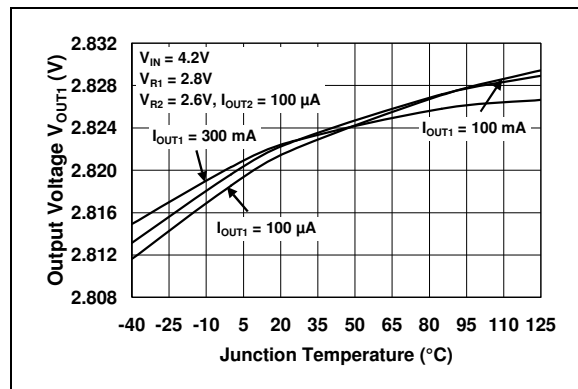
**FIGURE 2-8:** Dropout Voltage vs. Output Current ( $V_{OUT2}$ ).



**FIGURE 2-11:**  $V_{OUT1}$  and  $V_{OUT2}$  Line Regulation vs. Junction Temperature.

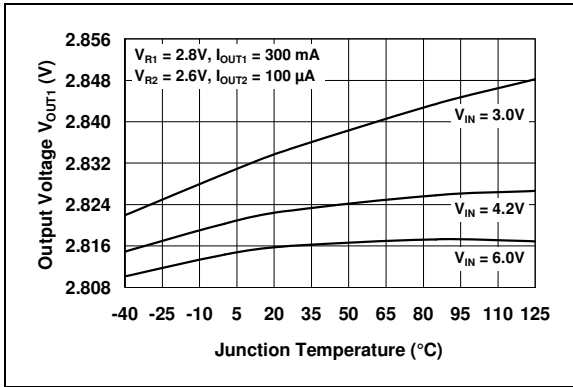


**FIGURE 2-9:** Dropout Voltage vs. Junction Temperature ( $V_{OUT2}$ ).

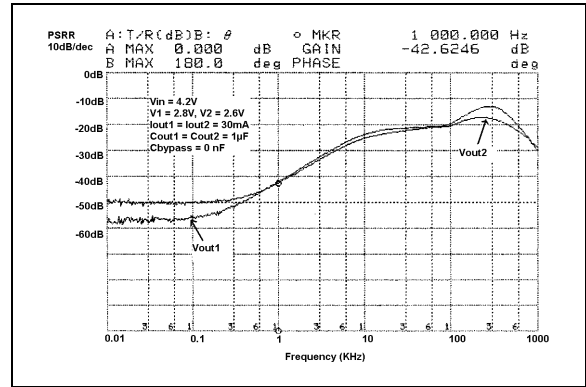


**FIGURE 2-12:**  $V_{OUT1}$  vs. Junction Temperature.

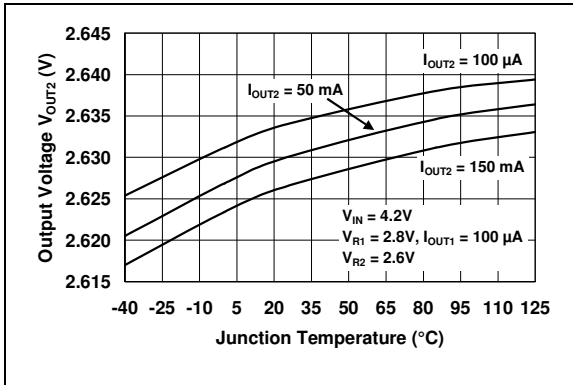
**Note:** Unless otherwise indicated,  $V_{IN} = V_R + 1V$ ,  $I_{OUT1} = I_{OUT2} = 100 \mu A$ ,  $C_{IN} = 4.7 \mu F$ ,  $C_{OUT1} = C_{OUT2} = 1 \mu F$  (X5R or X7R),  $C_{BYPASS} = 0 pF$ ,  $SHDN1 = SHDN2 > V_{IH}$ ,  $T_A = +25^\circ C$ .



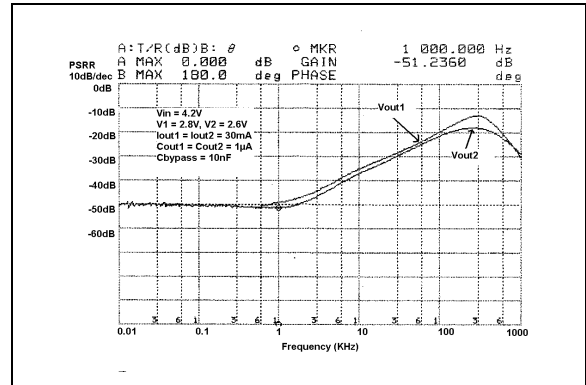
**FIGURE 2-13:**  $V_{OUT1}$  vs. Junction Temperature.



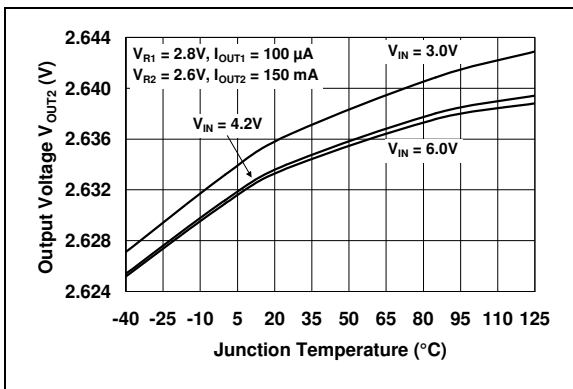
**FIGURE 2-16:** Power Supply Rejection Ratio vs. Frequency (without bypass capacitor).



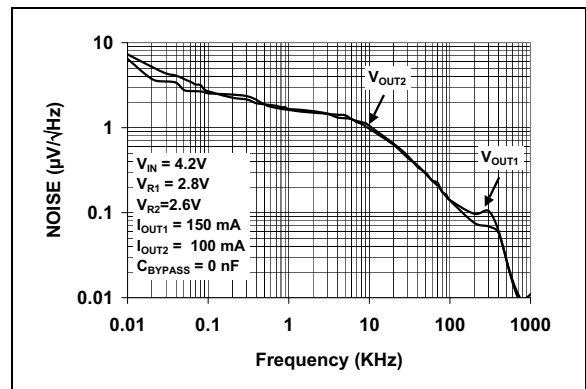
**FIGURE 2-14:**  $V_{OUT2}$  vs. Junction Temperature.



**FIGURE 2-17:** Power Supply Rejection Ratio vs. Frequency (with bypass capacitor).



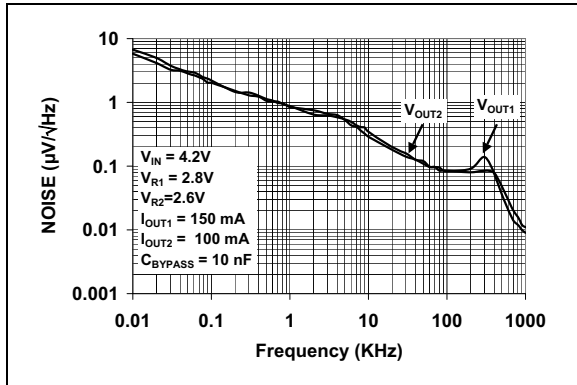
**FIGURE 2-15:**  $V_{OUT2}$  vs. Junction Temperature.



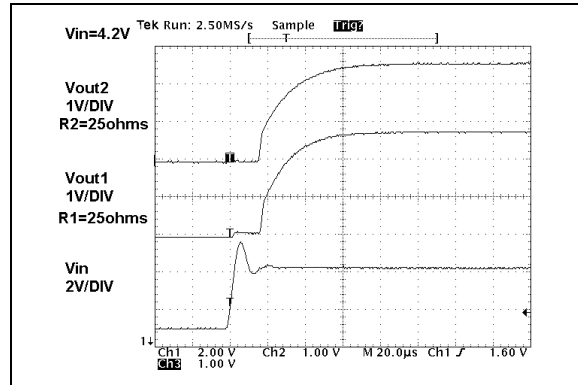
**FIGURE 2-18:**  $V_{OUT1}$  and  $V_{OUT2}$  Noise vs. Frequency (without bypass capacitor).

# TC1302A/B

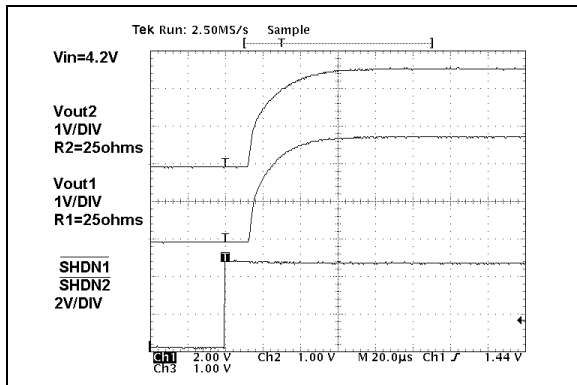
**Note:** Unless otherwise indicated,  $V_{IN} = V_R + 1V$ ,  $I_{OUT1} = I_{OUT2} = 100 \mu A$ ,  $C_{IN} = 4.7 \mu F$ ,  $C_{OUT1} = C_{OUT2} = 1 \mu F$  (X5R or X7R),  $C_{BYPASS} = 0 pF$ ,  $SHDN1 = SHDN2 > V_{IH}$ ,  $T_A = +25^\circ C$ .



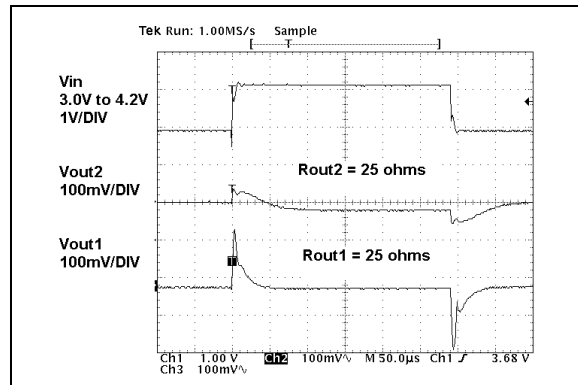
**FIGURE 2-19:**  $V_{OUT1}$  and  $V_{OUT2}$  Noise vs. Frequency (with bypass capacitor).



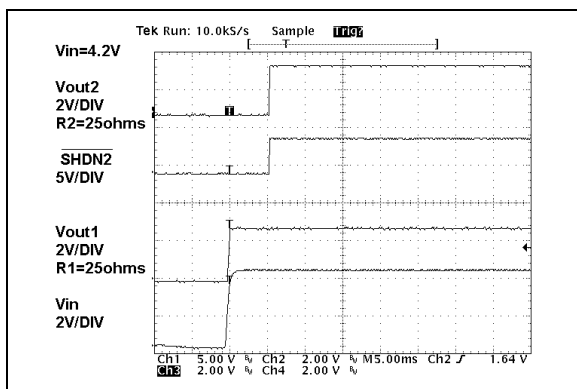
**FIGURE 2-22:**  $V_{OUT1}$  and  $V_{OUT2}$  Power-up from Input Voltage TC1302B.



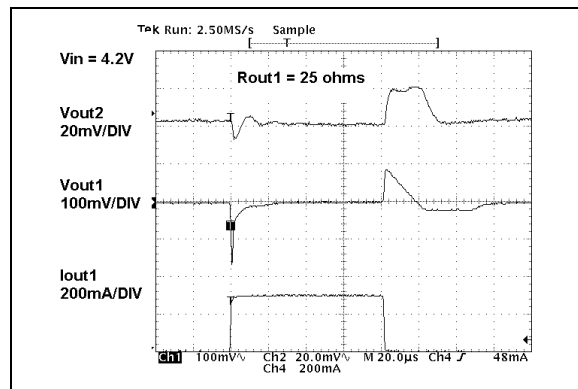
**FIGURE 2-20:**  $V_{OUT1}$  and  $V_{OUT2}$  Power-up from Shutdown TC1302B.



**FIGURE 2-23:** Dynamic Line Response.



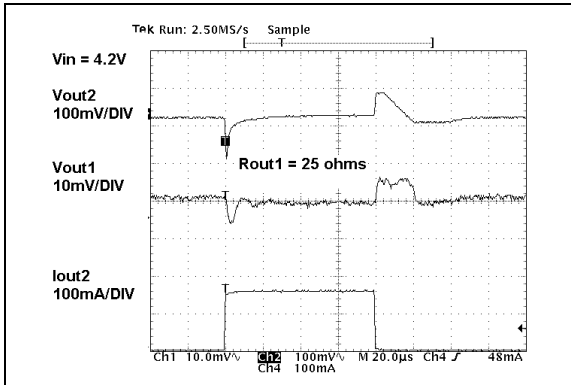
**FIGURE 2-21:**  $V_{OUT2}$  Power-up from Shutdown Input TC1302A.



**FIGURE 2-24:** 300 mA Dynamic Load Step  $V_{OUT1}$ .



**Note:** Unless otherwise indicated,  $V_{IN} = V_R + 1V$ ,  $I_{OUT1} = I_{OUT2} = 100 \mu A$ ,  $C_{IN} = 4.7 \mu F$ ,  $C_{OUT1} = C_{OUT2} = 1 \mu F$  (X5R or X7R),  $C_{BYPASS} = 0 pF$ ,  $SHDN1 = SHDN2 > V_{IH}$ ,  $T_A = +25^\circ C$ .



**FIGURE 2-25:** 150 mA Dynamic Load Step  
 $V_{OUT2}$

# TC1302A/B

## 3.0 TC1302A PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

**TABLE 3-1: TC1302A PIN FUNCTION TABLE**

Pin No.	Name	Function
1	NC	No connect.
2	V <sub>OUT1</sub>	Regulated output voltage #1, capable of 300 mA.
3	GND	Circuit ground pin.
4	Bypass	Internal reference bypass pin. A 10 nF external capacitor can be used to further reduce output noise and improve PSRR performance.
5	$\overline{\text{SHDN2}}$	Output #2 shutdown control input.
6	V <sub>OUT2</sub>	Regulated output voltage #2, capable of 150 mA.
7	V <sub>IN</sub>	Unregulated input voltage pin.
8	NC	No connect.

### 3.1 Regulated Output Voltage #1 (V<sub>OUT1</sub>)

Connect V<sub>OUT1</sub> to the positive side of the V<sub>OUT1</sub> capacitor and load. Capable of 300 mA maximum output current. V<sub>OUT1</sub> output is available when V<sub>IN</sub> is available; there is no pin to turn it OFF. See TC1302B if ON/OFF control of V<sub>OUT1</sub> is desired.

### 3.2 Circuit Ground Pin (GND)

Connect GND to the negative side of the input and output capacitor. Only the LDO internal circuitry bias current flows out of this pin (200  $\mu$ A maximum).

### 3.3 Reference Bypass Input

By connecting an external 10 nF capacitor (typical) to the Bypass Input, both outputs (V<sub>OUT1</sub> and V<sub>OUT2</sub>) will have less noise and improved Power Supply Ripple Rejection (PSRR) performance. The LDO output voltage start-up time will increase with the addition of an external bypass capacitor. By leaving this pin unconnected, the start-up time will be minimized.

### 3.4 Output Voltage #2 Shutdown (SHDN2)

ON/OFF control is performed by connecting  $\overline{\text{SHDN2}}$  to its proper level. When the input of this pin is connected to a voltage less than 15% of V<sub>IN</sub>, V<sub>OUT2</sub> will be OFF. If this pin is connected to a voltage that is greater than 45% of V<sub>IN</sub>, V<sub>OUT2</sub> will be turned ON.

### 3.5 Regulated Output Voltage #2 (V<sub>OUT2</sub>)

Connect V<sub>OUT2</sub> to the positive side of the V<sub>OUT2</sub> capacitor and load. This pin is capable of a maximum output current of 150 mA. V<sub>OUT2</sub> can be turned ON and OFF using SHDN2.

### 3.6 Unregulated Input Voltage Pin (V<sub>IN</sub>)

Connect the unregulated input voltage source to V<sub>IN</sub>. If the input voltage source is located more than several inches away or is a battery, a typical input capacitance of 1  $\mu$ F to 4.7  $\mu$ F is recommended.

## 4.0 TC1302B PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 4-1.

**TABLE 4-1: TC1302B PIN FUNCTION TABLE**

Pin No.	Name	Function
1	NC	No connect.
2	V <sub>OUT1</sub>	Regulated output voltage #1, capable of 300 mA.
3	GND	Circuit ground pin.
4	Bypass	Internal reference bypass pin. A 10 nF external capacitor can be used to further reduce output noise and improve PSRR performance.
5	$\overline{\text{SHDN2}}$	Output #2 shutdown control input.
6	V <sub>OUT2</sub>	Regulated output voltage #2, capable of 150 mA.
7	V <sub>IN</sub>	Unregulated Input voltage pin.
8	$\overline{\text{SHDN1}}$	Output #1 shutdown control input.

### 4.1 Regulated Output Voltage #1 (V<sub>OUT1</sub>)

Connect V<sub>OUT1</sub> to the positive side of the V<sub>OUT1</sub> capacitor and load. Capable of 300 mA maximum output current. For the TC1302B, V<sub>OUT1</sub> can be turned ON and OFF using the SHDN1 input pin.

### 4.2 Circuit Ground Pin (GND)

Connect GND to the negative side of the input and output capacitor. Only the LDO internal circuitry bias current flows out of this pin (200  $\mu$ A maximum).

### 4.3 Reference Bypass Input

By connecting an external 10 nF capacitor (typical) to the bypass input, both outputs (V<sub>OUT1</sub> and V<sub>OUT2</sub>) will have less noise and improved Power Supply Ripple Rejection (PSRR) performance. The LDO output voltage startup time will increase with the addition of an external bypass capacitor. By leaving this pin unconnected, the startup time will be minimized.

### 4.4 Output Voltage #2 Shutdown (SHDN2)

ON/ $\overline{\text{OFF}}$  control is performed by connecting  $\overline{\text{SHDN2}}$  to its proper level. When this pin is connected to a voltage less than 15% of V<sub>IN</sub>, V<sub>OUT2</sub> will be  $\overline{\text{OFF}}$ . If this pin is connected to a voltage that is greater than 45% of V<sub>IN</sub>, V<sub>OUT2</sub> will be turned ON.

### 4.5 Regulated Output Voltage #2 (V<sub>OUT2</sub>)

Connect V<sub>OUT2</sub> to the positive side of the V<sub>OUT2</sub> capacitor and load. This pin is capable of a maximum output current of 150 mA. V<sub>OUT2</sub> can be turned ON and OFF using SHDN2.

### 4.6 Unregulated Input Voltage Pin (V<sub>IN</sub>)

Connect the unregulated input voltage source to V<sub>IN</sub>. If the input voltage source is located more than several inches away, or is a battery, a typical minimum input capacitance of 1  $\mu$ F and 4.7  $\mu$ F is recommended.

### 4.7 Output Voltage #1 Shutdown (SHDN1)

ON/ $\overline{\text{OFF}}$  control is performed by connecting  $\overline{\text{SHDN1}}$  to its proper level. When this pin is connected to a voltage less than 15% of V<sub>IN</sub>, V<sub>OUT1</sub> will be  $\overline{\text{OFF}}$ . If this pin is connected to a voltage that is greater than 45% of V<sub>IN</sub>, V<sub>OUT1</sub> will be turned ON.

# TC1302A/B

---

## 5.0 DETAILED DESCRIPTION

### 5.1 Device Overview

The TC1302A/B is a combination device consisting of one 300 mA LDO regulator with a fixed output voltage  $V_{OUT1}$  (1.5V – 3.3V) and one 150 mA LDO regulator with a fixed output voltage  $V_{OUT2}$  (1.5V – 3.3V).

For the TC1302A, the 300 mA output ( $V_{OUT1}$ ) is always present, independent of the level of  $\overline{\text{SHDN2}}$ . The 150 mA output ( $V_{OUT2}$ ) can be turned ON/OFF by controlling the level of  $\overline{\text{SHDN2}}$ .

For the TC1302B,  $V_{OUT1}$  and  $V_{OUT2}$  each have independent shutdown input pins ( $\overline{\text{SHDN1}}$  and  $\overline{\text{SHDN2}}$ ) to control their respective outputs.

### 5.2 LDO Output #1

LDO output #1 is rated for 300 mA of output current. The typical dropout voltage for  $V_{OUT1} = 104 \text{ mV} @ 300 \text{ mA}$ . A 1  $\mu\text{F}$  (minimum) output capacitor is needed for stability and should be located as close to the  $V_{OUT1}$  pin and ground as possible.

### 5.3 LDO Output #2

LDO output #2 is rated for 150 mA of output current. The typical dropout voltage for  $V_{OUT2} = 150 \text{ mV}$ . A 1  $\mu\text{F}$  (minimum) capacitor is needed for stability and should be located as close to the  $V_{OUT2}$  pin and ground as possible.

### 5.4 Input Capacitor

Low input source impedance is necessary for the two LDO outputs to operate properly. When operating from batteries, or in applications with long lead length (> 10 inches) between the input source and the LDO, some input capacitance is recommended. A minimum of 1.0  $\mu\text{F}$  to 4.7  $\mu\text{F}$  is recommended for most applications. When using large capacitors on the LDO outputs, larger capacitance is recommended on the LDO input. The capacitor should be placed as close to the input of the LDO as is practical. Larger input capacitors will help reduce the input impedance and further reduce any high-frequency noise on the input and output of the LDO.

### 5.5 Output Capacitor

A minimum output capacitance of 1  $\mu\text{F}$  for each of the TC1302A/B LDO outputs is necessary for stability. Ceramic capacitors are recommended because of their size, cost and environmental robustness qualities. Tantalum or aluminum electrolytic capacitors can be used on the LDO outputs as well. The Equivalent Series Resistance (ESR) requirements on the electrolytic output capacitor's are between 0 and 2 ohms. The output capacitor should be located as close to the LDO output as is practical. Ceramic materials, X7R and X5R, have low temperature coefficients and are well within the acceptable ESR range required. A typical 1  $\mu\text{F}$  X5R 0805 capacitor has an ESR of 50 milliohms. Larger LDO output capacitors can be used with the TC1302A/B to improve dynamic performance and power supply ripple rejection performance. A maximum of 10  $\mu\text{F}$  is recommended. Aluminum electrolytic capacitors are not recommended for low temperature applications of < -25 °C.

### 5.6 Bypass Input

The Bypass pin is connected to the internal LDO reference. By adding capacitance to this pin, the LDO ripple rejection, input voltage transient response and output noise performance are all increased. A typical bypass capacitor between 470 pF to 10 nF is recommended. Larger bypass capacitors can be used, but result in a longer time period for the LDO outputs to reach their rated output voltage when started from  $\overline{\text{SHDN}}$  or  $V_{IN}$ .

### 5.7 GND

For the optimal noise and PSRR performance, the GND pin of the TC1302A/B should be tied to a quiet circuit ground. For applications that have switching or noisy inputs, tie the GND pin to the return of the output capacitor. Ground planes help lower inductance and voltage spikes caused by fast transient load currents and are recommended for applications that are subjected to fast load transients.

### 5.8 $\overline{\text{SHDN1}}/\overline{\text{SHDN2}}$ Operation

The TC1302A  $\overline{\text{SHDN2}}$  pin is used to turn  $V_{OUT2}$  ON and OFF. A logic-high level on  $\overline{\text{SHDN2}}$  will enable the  $V_{OUT2}$  output, while a logic-low on the  $\overline{\text{SHDN2}}$  pin will disable the  $V_{OUT2}$  output. For the TC1302A,  $V_{OUT1}$  is not affected by  $\overline{\text{SHDN2}}$  and will be enabled as long as the input voltage is present.

The TC1302B  $\overline{\text{SHDN1}}$  and  $\overline{\text{SHDN2}}$  pins are used to turn  $V_{OUT1}$  and  $V_{OUT2}$  ON and OFF. They operate independent of each other.

## 5.9 TC1302A $\overline{\text{SHDN2}}$ Timing

$V_{\text{OUT1}}$  will rise independent of the level of  $\overline{\text{SHDN2}}$  for the TC1302A. Figure 5-1 is used to define the wake-up time from shutdown ( $t_{\text{WK}}$ ) and the settling time ( $t_{\text{S}}$ ). The wake-up time is dependant upon the frequency of operation. The faster the  $\overline{\text{SHDN}}$  pin is pulsed, the shorter the wake-up time will be.

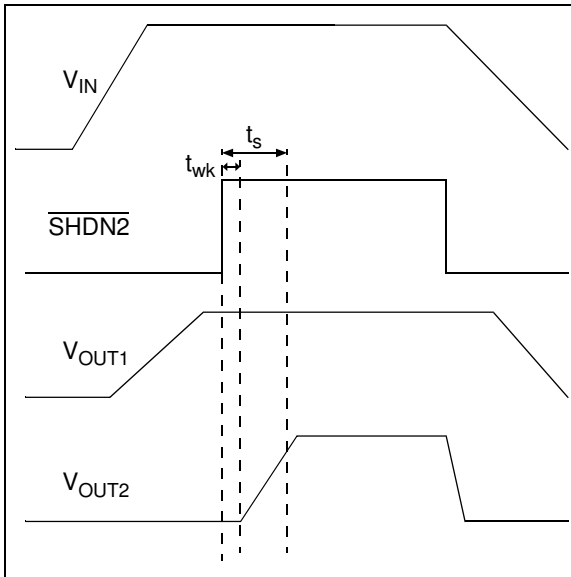


FIGURE 5-1: TC1302A Timing.

## 5.10 TC1302B $\overline{\text{SHDN1}}$ / $\overline{\text{SHDN2}}$ Timing

For the TC1302B, the  $\overline{\text{SHDN1}}$  input pin is used to control  $V_{\text{OUT1}}$ . The  $\overline{\text{SHDN2}}$  input pin is used to control  $V_{\text{OUT2}}$ , independent of the logic input on  $\overline{\text{SHDN1}}$ .

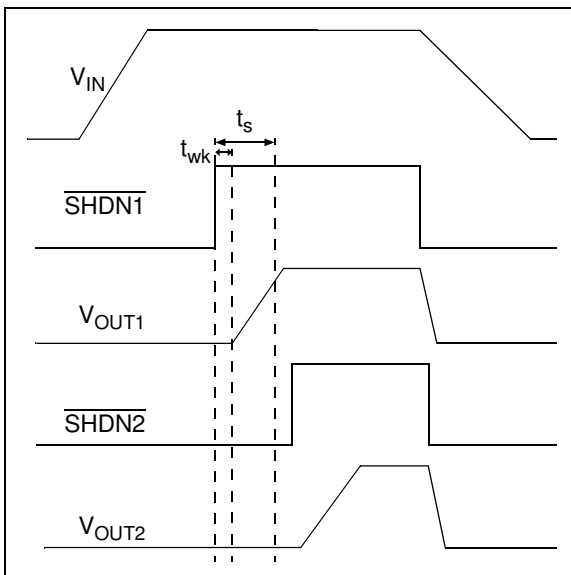


FIGURE 5-2: TC1302B Timing.

## 5.11 Device Protection

### 5.11.1 OVERCURRENT LIMIT

In the event of a faulted output load, the maximum current the LDO output will permit to flow is limited internally for each of the TC1302A/B outputs. The peak current limit for  $V_{\text{OUT1}}$  is typically 1.1A, while the peak current limit for  $V_{\text{OUT2}}$  is typically 0.5A. During short-circuit operation, the average current is limited to 200 mA for  $V_{\text{OUT1}}$  and 140 mA for  $V_{\text{OUT2}}$ .

### 5.11.2 OVERTEMPERATURE PROTECTION

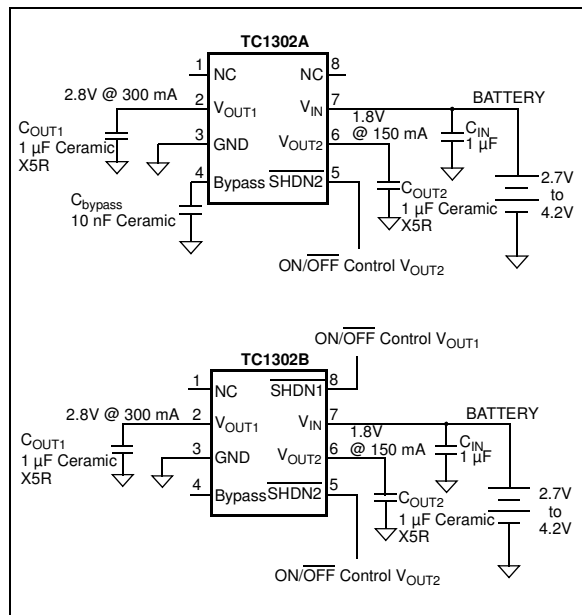
If the internal power dissipation within the TC1302A/B is excessive due to a faulted load or higher-than-specified line voltage, an internal temperature-sensing element will prevent the junction temperature from exceeding approximately 150°C. If the junction temperature does reach 150°C, both outputs will be disabled until the junction temperature cools to approximately 140°C and the device resumes normal operation. If the internal power dissipation continues to be excessive, the device will again shut off.

# TC1302A/B

## 6.0 APPLICATION CIRCUITS/ISSUES

### 6.1 Typical Application

The TC1302A/B is used for applications that require the integration of two LDOs.



**FIGURE 6-1:** Typical Application Circuit TC1302A/B.

#### 6.1.1 APPLICATION INPUT CONDITIONS

- Package Type = 3x3DFN8
- Input Voltage Range = 2.7V to 4.2V
- $V_{IN}$  maximum = 4.2V
- $V_{IN}$  typical = 3.6V
- $V_{OUT1}$  = 300 mA maximum
- $V_{OUT2}$  = 150 mA maximum

## 6.2 Power Calculations

### 6.2.1 POWER DISSIPATION

The internal power dissipation within the TC1302A/B is a function of input voltage, output voltage, output current and quiescent current. The following equation can be used to calculate the internal power dissipation for each LDO.

#### EQUATION 6-1:

$$P_{LDO} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$$

- $P_{LDO}$  = LDO Pass device internal power dissipation
- $V_{IN(MAX)}$  = Maximum input voltage
- $V_{OUT(MIN)}$  = LDO minimum output voltage

In addition to the LDO pass element power dissipation, there is power dissipation within the TC1302A/B as a result of quiescent or ground current. The power dissipation, as a result of the ground current, can be calculated using the following equation.

#### EQUATION 6-2:

$$P_{I(GND)} = V_{IN(MAX)} \times I_{VIN}$$

- $P_{I(GND)}$  = Total current in ground pin.
- $V_{IN(MAX)}$  = Maximum input voltage.
- $I_{VIN}$  = Current flowing in the  $V_{IN}$  pin with no output current on either LDO output.

The total power dissipated within the TC1302A/B is the sum of the power dissipated in both of the LDOs and the  $P_{I(GND)}$  term. Because of the CMOS construction, the typical  $I_{GND}$  for the TC1302A/B is 116  $\mu$ A. Operating at a maximum of 4.2V results in a power dissipation of 0.5 milliWatts. For most applications, this is small compared to the LDO pass device power dissipation and can be neglected.

The maximum continuous operating junction temperature specified for the TC1302A/B is +125°C. To estimate the internal junction temperature of the TC1302A/B, the total internal power dissipation is multiplied by the thermal resistance from junction to ambient ( $R\theta_{JA}$ ) of the device. The thermal resistance from junction-to-ambient for the 3x3DFN8 pin package is estimated at 41° C/W.

#### EQUATION 6-3:

$$T_{J(MAX)} = P_{TOTAL} \times R\theta_{JA} + T_{AMAX}$$

- $T_{J(MAX)}$  = Maximum continuous junction temperature.
- $P_{TOTAL}$  = Total device power dissipation.
- $R\theta_{JA}$  = Thermal resistance from junction to ambient.
- $T_{AMAX}$  = Maximum Ambient Temperature.

The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. The following equation can be used to determine the package maximum internal power dissipation.

## EQUATION 6-4:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{R\theta_{JA}}$$

$P_{D(MAX)}$  = maximum device power dissipation.  
 $T_{J(MAX)}$  = maximum continuous junction temperature.  
 $T_{A(MAX)}$  = maximum ambient temperature.  
 $R\theta_{JA}$  = Thermal resistance from junction to ambient.

## EQUATION 6-5:

$$T_{J(RISE)} = P_{D(MAX)} \times R\theta_{JA}$$

$T_{J(RISE)}$  = Rise in device junction temperature over the ambient temperature.  
 $P_{D(MAX)}$  = Maximum device power dissipation.  
 $R\theta_{JA}$  = Thermal resistance from junction-to-ambient.

## EQUATION 6-6:

$$T_J = T_{J(RISE)} + T_A$$

$T_J$  = Junction temperature.  
 $T_{J(RISE)}$  = Rise in device junction temperature over the ambient temperature.  
 $T_A$  = Ambient Temperature.

## 6.3 Typical Application

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation, as a result of ground current, is small enough to be neglected.

### 6.3.1 POWER DISSIPATION EXAMPLE

#### Package

Package Type = 3x3DFN8

Input Voltage

$$V_{IN} = 2.7V \text{ to } 4.2V$$

#### LDO Output Voltages and Currents

$$V_{OUT1} = 2.8V$$

$$I_{OUT1} = 300 \text{ mA}$$

$$V_{OUT2} = 1.8V$$

$$I_{OUT2} = 150 \text{ mA}$$

#### Maximum Ambient Temperature

$$T_{A(MAX)} = 50^\circ\text{C}$$

#### Internal Power Dissipation

Internal power dissipation is the sum of the power dissipation for each LDO pass device.

$$P_{LDO1(MAX)} = (V_{IN(MAX)} - V_{OUT1(MIN)}) \times I_{OUT1(MAX)}$$

$$P_{LDO1} = (4.2V - (0.975 \times 2.8V)) \times 300 \text{ mA}$$

$$P_{LDO1} = 441.0 \text{ milliWatts}$$

$$P_{LDO2} = (4.2V - (0.975 \times 1.8V)) \times 150 \text{ mA}$$

$$P_{LDO2} = 366.8 \text{ milliWatts}$$

$$P_{TOTAL} = P_{LDO1} + P_{LDO2}$$

$$P_{TOTAL} = 807.8 \text{ milliWatts}$$

#### Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance from junction to ambient for the application. The thermal resistance from junction to ambient ( $R\theta_{JA}$ ) is derived from an EIA/JEDEC standard for measuring thermal resistance for small surface-mount packages. The EIA/JEDEC specification is JESD51-7 "High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages". The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors, such as copper area and thickness. Refer to AN792, "A Method to Determine How Much Power a SOT23 Can Dissipate in an Application", (DS00792), for more information regarding this subject.

$$T_{J(RISE)} = P_{TOTAL} \times R\theta_{JA}$$

$$T_{J(RISE)} = 807.8 \text{ milliWatts} \times 41.0^\circ\text{C/W}$$

$$T_{J(RISE)} = 33.1^\circ\text{C}$$

#### Junction Temperature Estimate

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated below.

$$T_J = T_{J(RISE)} + T_{A(MAX)}$$

$$T_J = 83.1^\circ\text{C}$$

#### Maximum Package Power Dissipation at 50°C Ambient Temperature

3x3DFN8 (41°C/Watt  $R\theta_{JA}$ )

$$P_{D(MAX)} = (125^\circ\text{C} - 50^\circ\text{C})/41^\circ\text{C/W}$$

$$P_{D(MAX)} = 1.83 \text{ Watts}$$

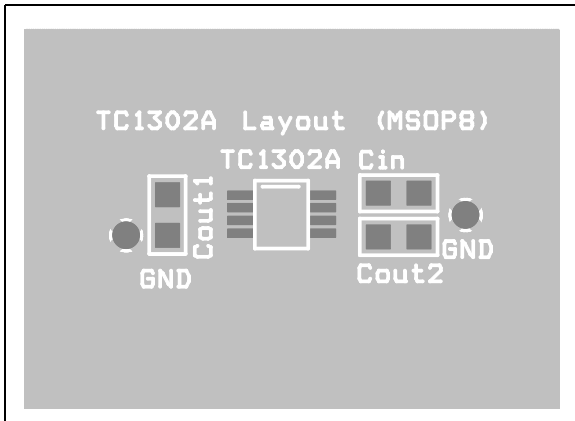
MSOP8 (208°C/Watt  $R\theta_{JA}$ )

$$P_{D(MAX)} = (125^\circ\text{C} - 50^\circ\text{C})/208^\circ\text{C/W}$$

$$P_{D(MAX)} = 0.360 \text{ Watts}$$

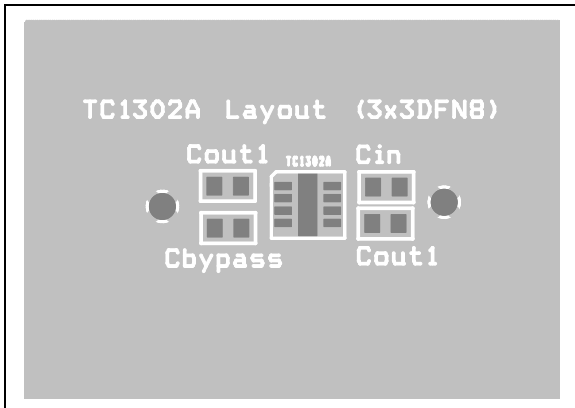
# TC1302A/B

## 7.0 TYPICAL LAYOUT



**FIGURE 7-1:** MSOP8 Silk-screen Layer.

When designing the physical layout for the TC1302A/B, the highest priority should be placed on positioning the input and output capacitors as close to the device pins as is practical. Figure 7-1 above represents a typical placement of the components when using the SMT0805 capacitors.



**FIGURE 7-2:** DFN3x3 Silk-screen Example.

Figure 7-2 above represents a typical placement of the components when using the SMT0603 capacitors.

## 8.0 ADDITIONAL OUTPUT VOLTAGES

### 8.1 Output Voltage Options

Table 8-1 describes the range of output voltage options available for the TC1302A/B.  $V_{OUT1}$  and  $V_{OUT2}$  can be factory preset from 1.5V to 3.3V in 100 mV increments.

**TABLE 8-1: CUSTOM OUTPUT VOLTAGES**

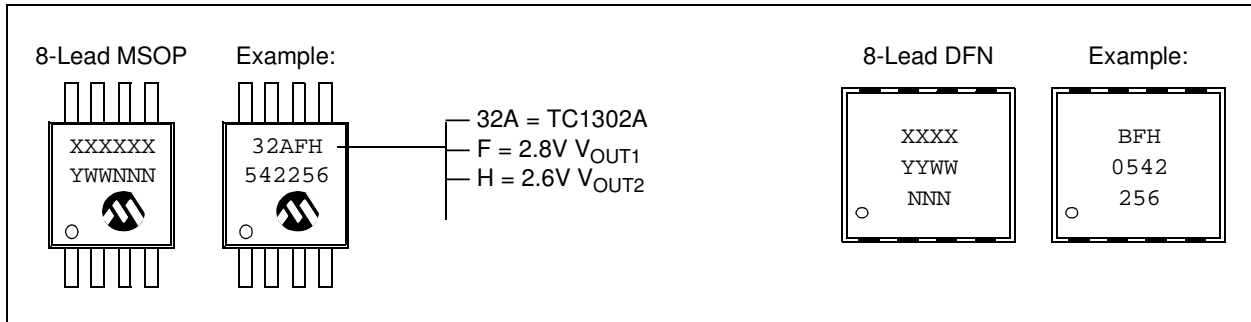
$V_{OUT1}$	$V_{OUT2}$
1.5V to 3.3V	1.5V to 3.3V

For a listing of TC1302A/B standard parts, refer to the Product Identification System on page 23.



## 9.0 PACKAGING INFORMATION

### 9.1 Package Marking Information



X1 represents  $V_{OUT1}$  configuration:

Code	$V_{OUT1}$	Code	$V_{OUT1}$	Code	$V_{OUT1}$
A	3.3V	J	2.4V	S	1.5V
B	3.2V	K	2.3V	T	1.65V
C	3.1V	L	2.2V	U	2.85V
D	3.0V	M	2.1V	V	2.65V
E	2.9V	N	2.0V	W	1.85V
F	2.8V	O	1.9V	X	—
G	2.7V	P	1.8V	Y	—
H	2.6V	Q	1.7V	Z	—
I	2.5V	R	1.6V		

X2 represents  $V_{OUT2}$  configuration:

Code	$V_{OUT2}$	Code	$V_{OUT1}$	Code	$V_{OUT2}$
A	3.3V	J	2.4V	S	1.5V
B	3.2V	K	2.3V	T	1.65V
C	3.1V	L	2.2V	U	2.85V
D	3.0V	M	2.1V	V	2.65V
E	2.9V	N	2.0V	W	1.85V
F	2.8V	O	1.9V	X	—
G	2.7V	P	1.8V	Y	—
H	2.6V	Q	1.7V	Z	—
I	2.5V	R	1.6V		

For a listing of TC1302A/B standard parts, refer to the Product Identification System on page 23.

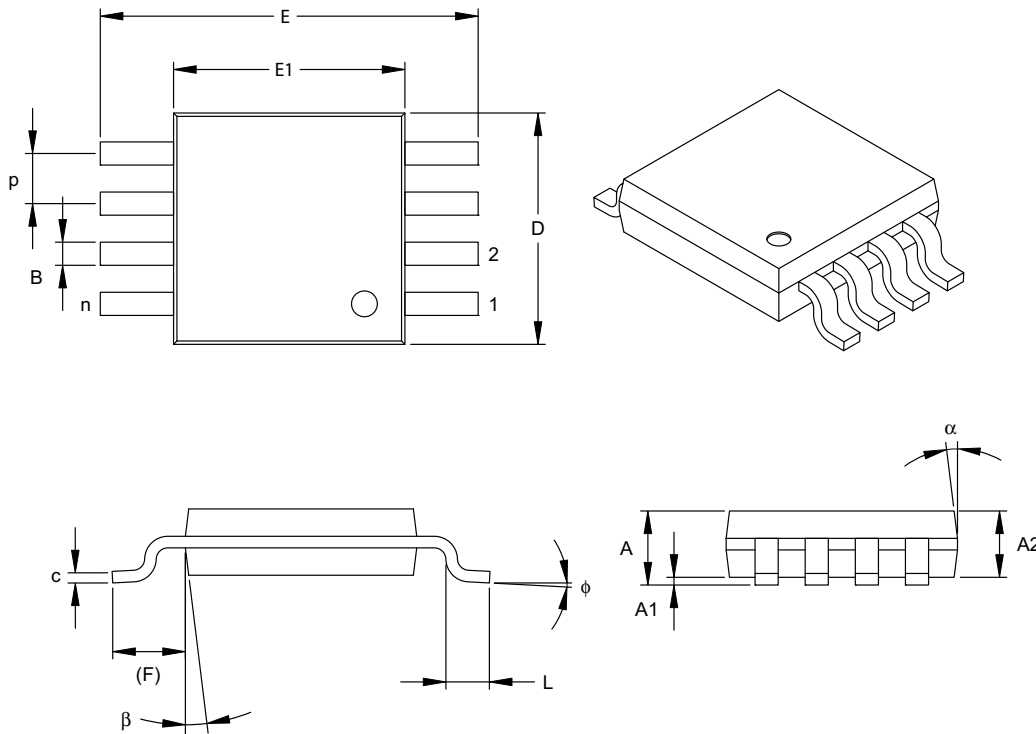
**Legend:** XX...X Customer-specific information  
 Y Year code (last digit of calendar year)  
 YY Year code (last 2 digits of calendar year)  
 WW Week code (week of January 1 is week '01')  
 NNN Alphanumeric traceability code  
 (e3) Pb-free JEDEC designator for Matte Tin (Sn)  
 \* This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

# TC1302A/B

## 8-Lead Plastic Micro Small Outline Package (UA) (MSOP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	P	.026 BSC			0.65 BSC		
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E	.193 TYP.			4.90 BSC		
Molded Package Width	E1	.118 BSC			3.00 BSC		
Overall Length	D	.118 BSC			3.00 BSC		
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F	.037 REF			0.95 REF		
Foot Angle	φ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

\*Controlling Parameter

Notes:

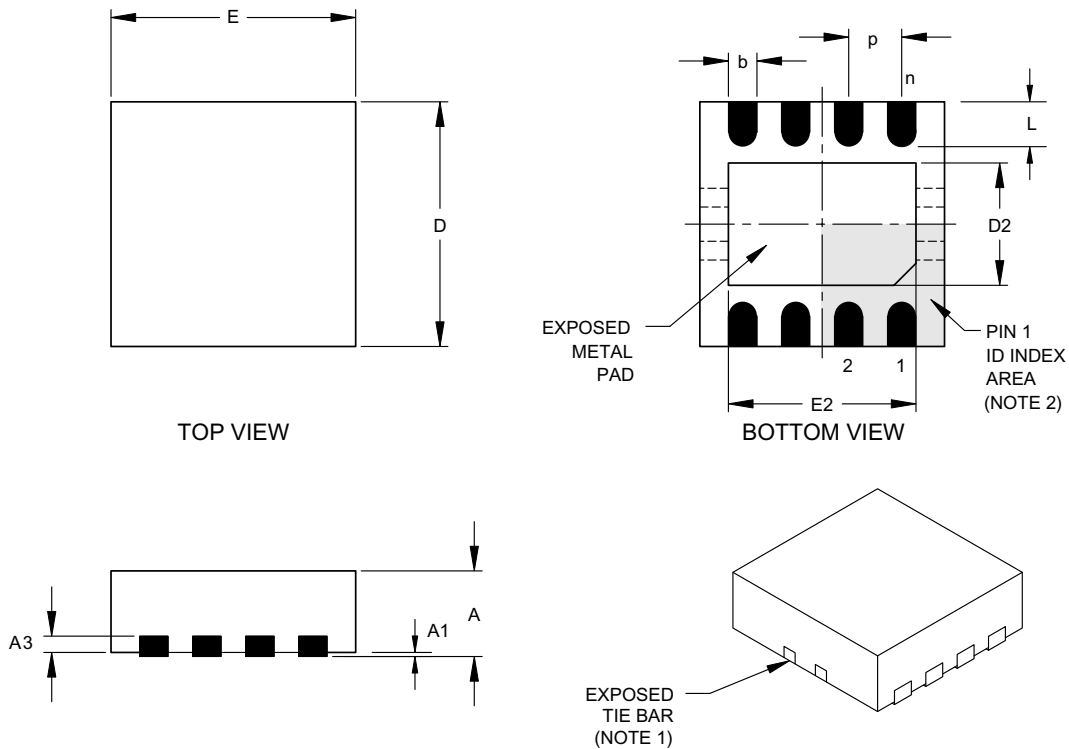
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

## 8-Lead Plastic Dual Flat No Lead Package (MF) 3x3x0.9 mm Body (DFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES			MILLIMETERS*		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	.031	.035	.039	0.80	0.90	1.00
Standoff	A1	.000	.001	.002	0.00	0.02	0.05
Lead Thickness	A3		.008 REF.			0.20 REF.	
Overall Length	E		.118 BSC			3.00 BSC	
Exposed Pad Length (Note 4)	E2	.055		.096	1.39		2.45
Overall Width	D		.118 BSC			3.00 BSC	
Exposed Pad Width (Note 4)	D2	.047		.069	1.20		1.75
Lead Width	b	.007	.010	.015	0.23	0.26	0.37
Lead Length	L	.012	.019	.022	0.30	0.48	0.55

\*Controlling Parameter

Notes:

- Package may have one or more exposed tie bars at ends.
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
- Exposed pad dimensions vary with paddle size.
- JEDEC equivalent: Pending

Drawing No. C04-062

# TC1302A/B

---

NOTES:

## **APPENDIX A: REVISION HISTORY**

### **Revision A (September 2003)**

Original data sheet release.

### **Revision B (January 2005)**

The following is the list of modifications:

1. Correct the incorrect part number options shown on the Product Identification System page and change the “standard” output voltage and reset voltage combinations.
2. Added Appendix A: Revision History.

### **Revision C (November 2012)**

Added a note to each package outline drawing.

# TC1302A/B

---

NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X-	X	X	X	XX	XX															
TC1302	Type A/B	V <sub>OUT1</sub>	V <sub>OUT2</sub>	Temp Range	Package	Tube or Tape & Reel															
		Standard Configurations																			
<p>Device: TC1302A: Dual Output LDO with Single Shutdown input. TC1302B: Dual Output LDO with Dual Shutdown Inputs.</p> <table border="1"> <thead> <tr> <th>Standard Configurations: *</th> <th>V<sub>OUT1</sub>/V<sub>OUT2</sub></th> <th>Configuration Code</th> </tr> </thead> <tbody> <tr> <td>TC1302A</td> <td>3.0/1.65</td> <td>DT</td> </tr> <tr> <td>TC1302B</td> <td>3.0/1.65</td> <td>DT</td> </tr> <tr> <td></td> <td>2.6/1.8</td> <td>HP</td> </tr> <tr> <td></td> <td>2.5/1.8</td> <td>IP</td> </tr> </tbody> </table> <p>* Contact Factory for Alternate Output Voltage Configurations.</p> <p>Temperature Range: V = -40°C to +125°C</p> <p>Package: MF = Dual Flat, No Lead (3x3 mm body), 8-lead UA = Plastic Micro Small Outline (MSOP), 8-lead</p> <p>Tube or Tape and Reel: Blank = Tube TR = Tape and Reel</p>							Standard Configurations: *	V <sub>OUT1</sub> /V <sub>OUT2</sub>	Configuration Code	TC1302A	3.0/1.65	DT	TC1302B	3.0/1.65	DT		2.6/1.8	HP		2.5/1.8	IP
Standard Configurations: *	V <sub>OUT1</sub> /V <sub>OUT2</sub>	Configuration Code																			
TC1302A	3.0/1.65	DT																			
TC1302B	3.0/1.65	DT																			
	2.6/1.8	HP																			
	2.5/1.8	IP																			
<b>Examples:</b>																					
a)	TC1302ADTVMF:	3.0, 1.65, 8LD DFN pkg.																			
a)	TC1302BDTVMF:	3.0, 1.65, 8LD DFN pkg.																			
b)	TC1302BHPVMFTR:	2.6, 1.8, 8LD DFN pkg, Tape and Reel.																			
c)	TC1302BIPVUA:	2.5, 1.8, 8LD MSOP pkg.																			

# TC1302A/B

---

NOTES:



---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

#### Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC<sup>32</sup> logo, rPIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MTP, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.


Analog-for-the-Digital Age, Application Maestro, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniclient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICtail, REAL ICE, rLAB, Select Mode, SQI, Serial Quad I/O, Total Endurance, TSHARC, UniWinDriver, WiperLock, ZENA and Z-Scale are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

GestIC and ULPP are registered trademarks of Microchip Technology Germany II GmbH & Co. & KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2003-2012, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

ISBN: 9781620767443

*Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC<sup>®</sup> MCUs and dsPIC<sup>®</sup> DSCs, KEELOQ<sup>®</sup> code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*

---

**QUALITY MANAGEMENT SYSTEM**  
**CERTIFIED BY DNV**  
**== ISO/TS 16949 ==**



# MICROCHIP

## Worldwide Sales and Service

### AMERICAS

**Corporate Office**  
2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://www.microchip.com/support>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

**Atlanta**  
Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

**Boston**  
Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

**Chicago**  
Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

**Cleveland**  
Independence, OH  
Tel: 216-447-0464  
Fax: 216-447-0643

**Dallas**  
Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

**Detroit**  
Farmington Hills, MI  
Tel: 248-538-2250  
Fax: 248-538-2260

**Indianapolis**  
Noblesville, IN  
Tel: 317-773-8323  
Fax: 317-773-5453

**Los Angeles**  
Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608

**Santa Clara**  
Santa Clara, CA  
Tel: 408-961-6444  
Fax: 408-961-6445

**Toronto**  
Mississauga, Ontario,  
Canada  
Tel: 905-673-0699  
Fax: 905-673-6509

### ASIA/PACIFIC

**Asia Pacific Office**  
Suites 3707-14, 37th Floor  
Tower 6, The Gateway  
Harbour City, Kowloon  
Hong Kong  
Tel: 852-2401-1200  
Fax: 852-2401-3431

**Australia - Sydney**  
Tel: 61-2-9868-6733  
Fax: 61-2-9868-6755

**China - Beijing**  
Tel: 86-10-8569-7000  
Fax: 86-10-8528-2104

**China - Chengdu**  
Tel: 86-28-8665-5511  
Fax: 86-28-8665-7889

**China - Chongqing**  
Tel: 86-23-8980-9588  
Fax: 86-23-8980-9500

**China - Hangzhou**  
Tel: 86-571-2819-3187  
Fax: 86-571-2819-3189

**China - Hong Kong SAR**  
Tel: 852-2401-1200  
Fax: 852-2401-3431

**China - Nanjing**  
Tel: 86-25-8473-2460  
Fax: 86-25-8473-2470

**China - Qingdao**  
Tel: 86-532-8502-7355  
Fax: 86-532-8502-7205

**China - Shanghai**  
Tel: 86-21-5407-5533  
Fax: 86-21-5407-5066

**China - Shenyang**  
Tel: 86-24-2334-2829  
Fax: 86-24-2334-2393

**China - Shenzhen**  
Tel: 86-755-8203-2660  
Fax: 86-755-8203-1760

**China - Wuhan**  
Tel: 86-27-5980-5300  
Fax: 86-27-5980-5118

**China - Xian**  
Tel: 86-29-8833-7252  
Fax: 86-29-8833-7256

**China - Xiamen**  
Tel: 86-592-2388138  
Fax: 86-592-2388130

**China - Zhuhai**  
Tel: 86-756-3210040  
Fax: 86-756-3210049

### ASIA/PACIFIC

**India - Bangalore**  
Tel: 91-80-3090-4444  
Fax: 91-80-3090-4123

**India - New Delhi**  
Tel: 91-11-4160-8631  
Fax: 91-11-4160-8632

**India - Pune**  
Tel: 91-20-2566-1512  
Fax: 91-20-2566-1513

**Japan - Osaka**  
Tel: 81-66-152-7160  
Fax: 81-66-152-9310

**Japan - Yokohama**  
Tel: 81-45-471-6166  
Fax: 81-45-471-6122

**Korea - Daegu**  
Tel: 82-53-744-4301  
Fax: 82-53-744-4302

**Korea - Seoul**  
Tel: 82-2-554-7200  
Fax: 82-2-558-5932 or  
82-2-558-5934

**Malaysia - Kuala Lumpur**  
Tel: 60-3-6201-9857  
Fax: 60-3-6201-9859

**Malaysia - Penang**  
Tel: 60-4-227-8870  
Fax: 60-4-227-4068

**Philippines - Manila**  
Tel: 63-2-634-9065  
Fax: 63-2-634-9069

**Singapore**  
Tel: 65-6334-8870  
Fax: 65-6334-8850

**Taiwan - Hsin Chu**  
Tel: 886-3-5778-366  
Fax: 886-3-5770-955

**Taiwan - Kaohsiung**  
Tel: 886-7-213-7828  
Fax: 886-7-330-9305

**Taiwan - Taipei**  
Tel: 886-2-2508-8600  
Fax: 886-2-2508-0102

**Thailand - Bangkok**  
Tel: 66-2-694-1351  
Fax: 66-2-694-1350

### EUROPE

**Austria - Wels**  
Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

**Denmark - Copenhagen**  
Tel: 45-4450-2828  
Fax: 45-4485-2829

**France - Paris**  
Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

**Germany - Munich**  
Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

**Italy - Milan**  
Tel: 39-0331-742611  
Fax: 39-0331-466781

**Netherlands - Drunen**  
Tel: 31-416-690399  
Fax: 31-416-690340

**Spain - Madrid**  
Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

**UK - Wokingham**  
Tel: 44-118-921-5869  
Fax: 44-118-921-5820

10/26/12