

Features

- Pin and function compatible with CY7C1010CV33
- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low active power
 - $I_{CC} = 90 \text{ mA}$ at 10 ns
- Low CMOS standby power
 - $I_{SB2} = 10 \text{ mA}$
- 2.0 V data retention
- Automatic power down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Available in Pb-free 36-pin SOJ and 44-pin TSOP II packages

Functional Description

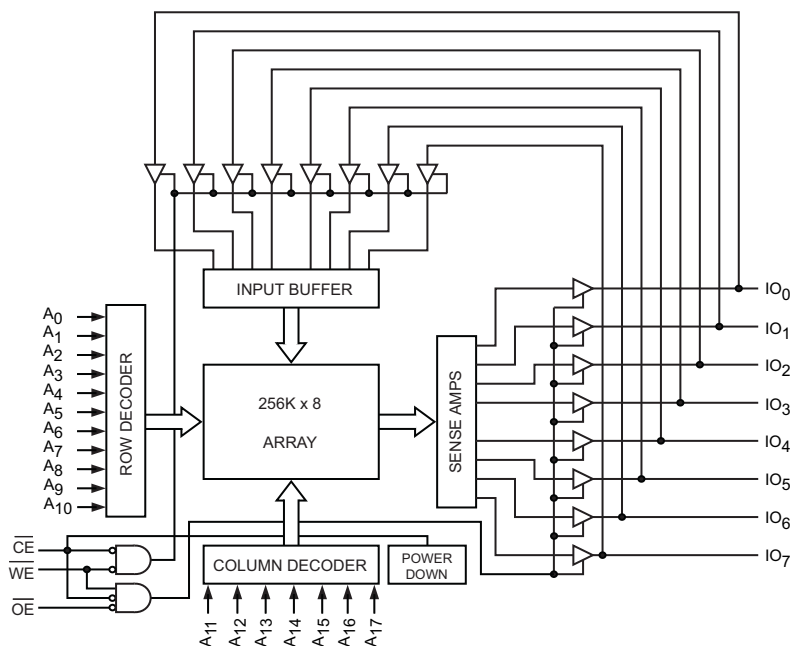
The CY7C1010DV33 is a high performance CMOS Static RAM organized as 256 K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}), an active LOW Output Enable (\overline{OE}), and three-state drivers. Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a Write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY7C1010DV33 is available in 36-pin SOJ and 44-pin TSOP II packages with center power and ground (revolutionary) pinout.

Logic Block Diagram



Contents

Selection Guide	3	Ordering Information	11
Pin Configuration	3	Ordering Code Definitions	11
Maximum Ratings	4	Package Diagrams	12
Operating Range	4	Acronyms	14
Electrical Characteristics	4	Document Conventions	14
Capacitance	5	Units of Measure	14
Thermal Resistance	5	Document History Page	15
AC Test Loads and Waveforms	5	Sales, Solutions, and Legal Information	16
Data Retention Characteristics	6	Worldwide Sales and Design Support	16
Data Retention Waveform	6	Products	16
AC Switching Characteristics	7	PSoC® Solutions	16
Switching Waveforms	8	Cypress Developer Community	16
Truth Table	10	Technical Support	16

Selection Guide

Description	-10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	90	mA
Maximum CMOS Standby Current	10	mA

Pin Configuration

Figure 1. 36-pin SOJ pinout [1]

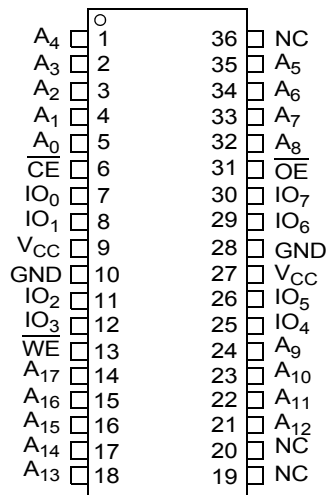
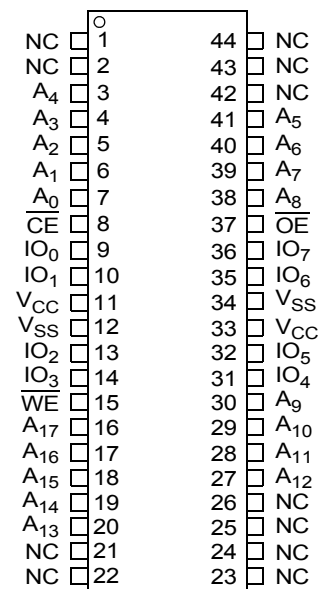


Figure 2. 44-pin TSOP II pinout [1]



Note

1. NC pins are not connected on the die.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature	-65 °C to +150 °C
Ambient Temperature with Power Applied	-55 °C to +125 °C
Supply Voltage on V _{CC} Relative to GND [2]	-0.5 V to +4.6 V
DC Voltage Applied to Outputs in High Z State [2]	-0.3 V to V _{CC} + 0.3 V

DC Input Voltage [2]	-0.3 V to V _{CC} + 0.3 V
Current into Outputs (LOW)	20 mA
Static Discharge Voltage (MIL-STD-883, Method 3015)	> 2001 V
Latch Up Current	> 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Industrial	-40 °C to +85 °C	3.3V ± 0.3V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10		Unit	
			Min	Max		
V _{OH}	Output HIGH Voltage	V _{CC} = Min; I _{OH} = -4.0 mA	2.4	-	V	
V _{OL}	Output LOW Voltage	V _{CC} = Min; I _{OL} = 8.0 mA	-	0.4	V	
V _{IH}	Input HIGH Voltage		2.0	V _{CC} + 0.3	V	
V _{IL}	Input LOW Voltage [2]		-0.3	0.8	V	
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1	+1	μA	
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled	-1	+1	μA	
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max, f = f _{MAX} = 1/t _{RC}	100 MHz	-	90	mA
			83 MHz	-	80	
			66 MHz	-	70	
			40 MHz	-	60	
I _{SB1}	Automatic CE Power-down Current – TTL Inputs	Max V _{CC} , $\overline{CE} \geq V_{IH}$; V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	-	20	mA	
I _{SB2}	Automatic CE Power-down Current – CMOS Inputs	Max V _{CC} , $\overline{CE} \geq V_{CC} - 0.3 V$, V _{IN} ≥ V _{CC} - 0.3 V, or V _{IN} ≤ 0.3 V, f = 0	-	10	mA	

Note

2. V_{IL} (min.) = -2.0V and V_{IH} (max.) = V_{CC} + 2.0V for pulse durations of less than 20 ns.

Capacitance

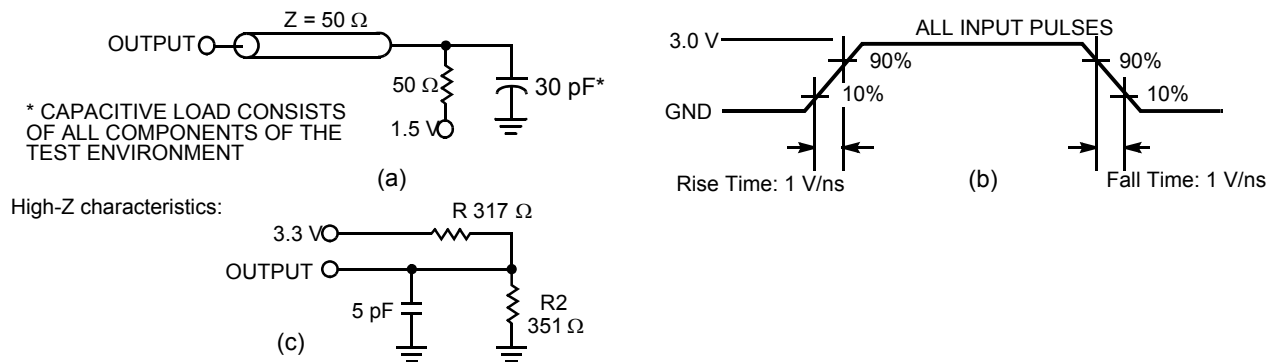
Parameter ^[3]	Description	Test Conditions	36-pin SOJ	44-pin TSOP II	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 3.3 V	8	8	pF
C _{OUT}	I/O capacitance		8	8	pF

Thermal Resistance

Parameter ^[3]	Description	Test Conditions	36-pin SOJ	44-pin TSOP II	Unit
Θ _{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	59.17	50.66	°C/W
Θ _{JC}	Thermal resistance (junction to case)		32.63	17.77	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms ^[4]



Notes

- 3. Tested initially and after any design or process changes that may affect these parameters.
- 4. AC characteristics (except High Z) are tested using the load conditions shown in Figure 3 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 3 (c).

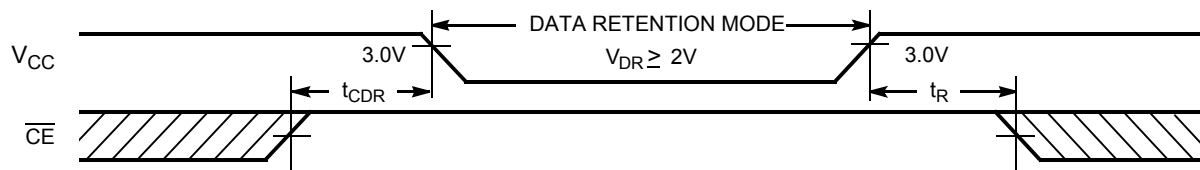
Data Retention Characteristics

Over the Operating Range

Parameter ^[5]	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention		2	–	V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0\text{ V}$, $\overline{CE} \geq V_{CC} - 0.3\text{ V}$, $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	–	10	mA
t_{CDR} ^[6]	Chip Deselect to Data Retention Time		0	–	ns
t_R ^[7]	Operation Recovery Time		t_{RC}	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

5. No inputs may exceed $V_{CC} + 0.3\text{ V}$.
6. Tested initially and after any design or process changes that may affect these parameters.
7. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50\ \mu\text{s}$ or stable at $V_{CC(min.)} \geq 50\ \mu\text{s}$.

AC Switching Characteristics

Over the Operating Range

Parameter ^[8]	Description	-10		Unit
		Min	Max	
Read Cycle				
$t_{power}^{[9]}$	V_{CC} (typical) to the first access	100	–	μ s
t_{RC}	Read Cycle Time	10	–	ns
t_{AA}	Address to Data Valid	–	10	ns
t_{OHA}	Data Hold from Address Change	3	–	ns
t_{ACE}	\overline{CE} LOW to Data Valid	–	10	ns
t_{DOE}	\overline{OE} LOW to Data Valid	–	5	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[10]	0	–	ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[10, 11]	–	5	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[10]	3	–	ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[10, 11]	–	5	ns
t_{PU}	\overline{CE} LOW to Power-up	0	–	ns
t_{PD}	\overline{CE} HIGH to Power-down	–	10	ns
Write Cycle^[12, 13]				
t_{WC}	Write Cycle Time	10	–	ns
t_{SCE}	\overline{CE} LOW to Write End	7	–	ns
t_{AW}	Address Set-up to Write End	7	–	ns
t_{HA}	Address Hold from Write End	0	–	ns
t_{SA}	Address Set-up to Write Start	0	–	ns
t_{PWE}	\overline{WE} Pulse Width	7	–	ns
t_{SD}	Data Set-up to Write End	5	–	ns
t_{HD}	Data Hold from Write End	0	–	ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[10]	3	–	ns
t_{HZWE}	\overline{WE} LOW to High Z ^[10, 11]	–	5	ns

Notes

8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
9. t_{POWER} gives the minimum amount of time that the power supply should be at stable, typical V_{CC} values until the first memory access can be performed.
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
11. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of Figure 3 on page 5. Transition is measured when the outputs enter a high impedance state.
12. The internal Write time of the memory is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
13. The minimum Write cycle time for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 5. Read Cycle No. 1 [14, 15]

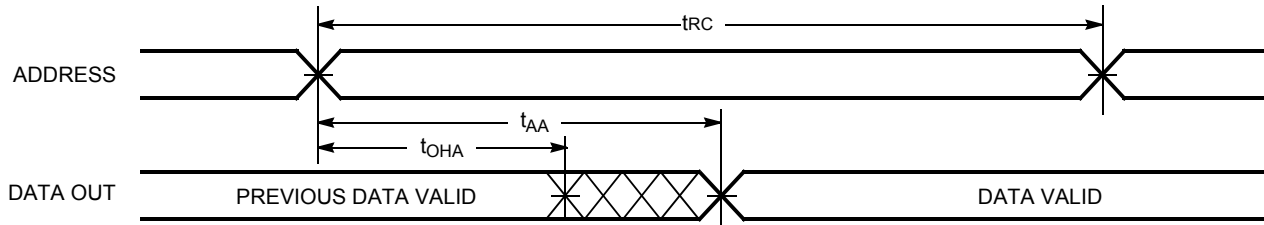
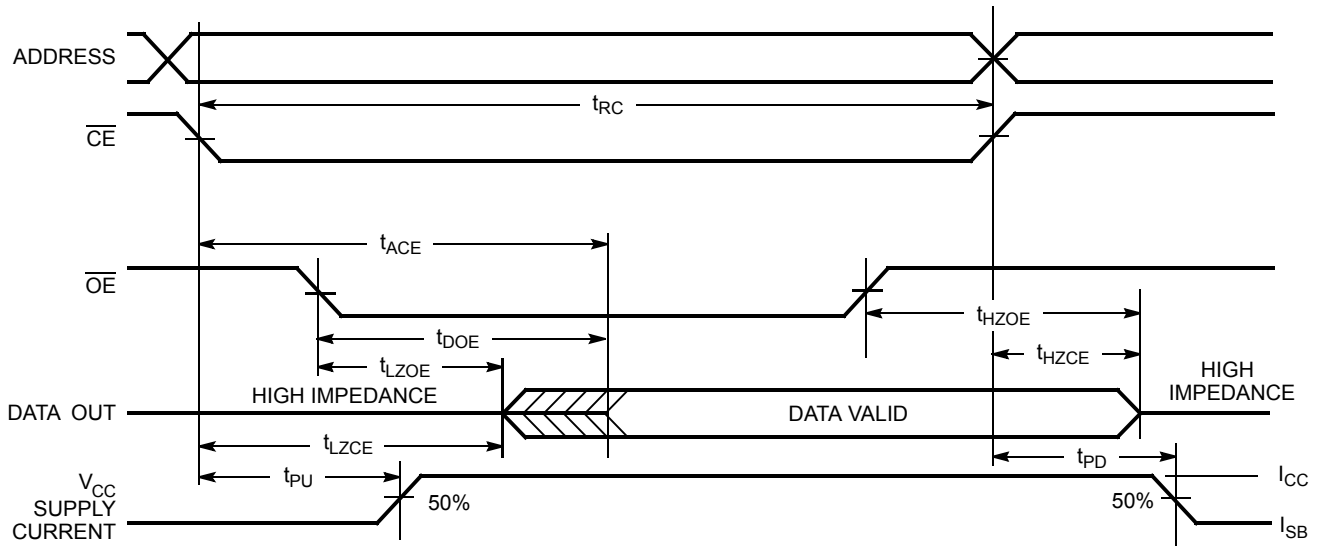


Figure 6. Read Cycle No. 2 (\overline{OE} Controlled) [15, 16]



Notes

- 14. The device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
- 15. \overline{WE} is HIGH for read cycle.
- 16. Address valid before or similar to \overline{CE} transition LOW.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 (\overline{WE} Controlled, \overline{OE} HIGH During Write) [17, 18]

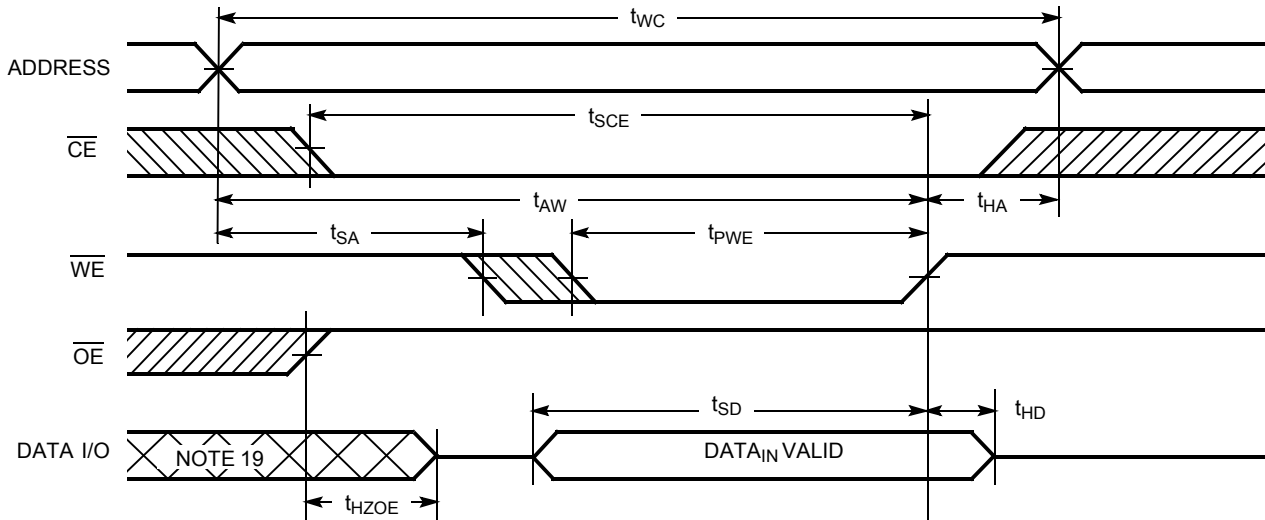
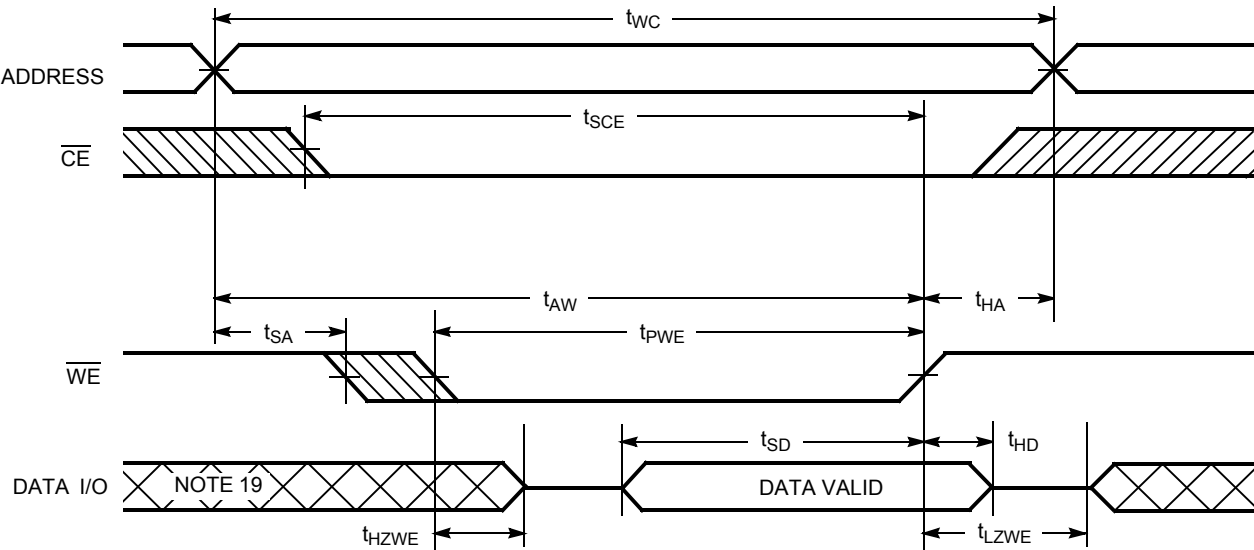


Figure 8. Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} LOW) [18]



Notes

- 17. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 18. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high impedance state.
- 19. During this period, the I/Os are in output state and input signals should not be applied.

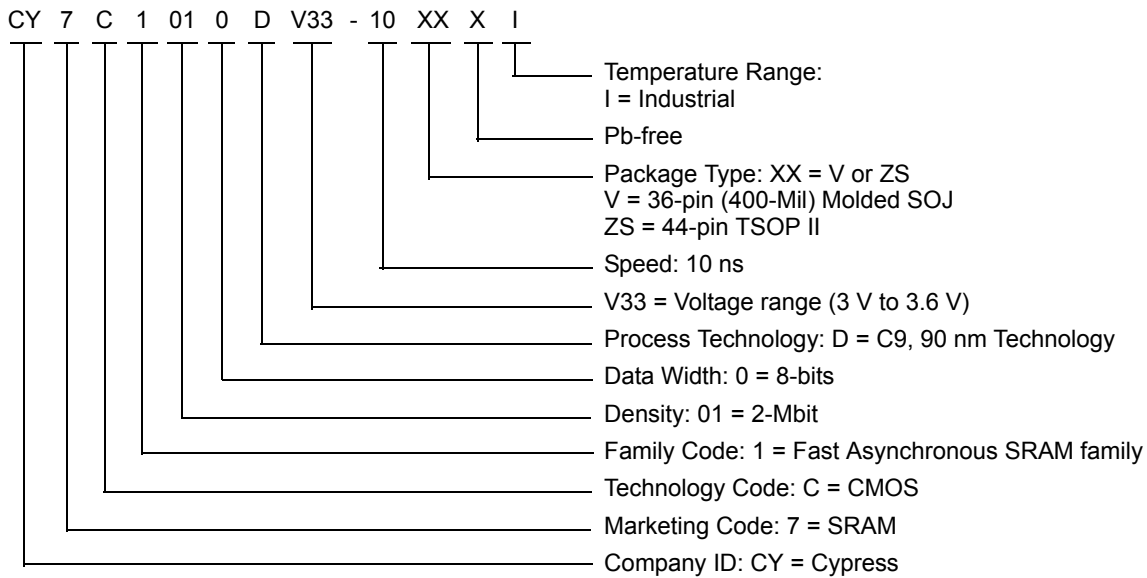
Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	I/O ₀ -I/O ₇	I/O ₈ -I/O ₁₅	Mode	Power
H	X	X	High Z	High Z	Power Down	Standby (I _{SB})
L	L	H	Data Out	Data Out	Read All Bits	Active (I _{CC})
L	X	L	Data In	Data In	Write All Bits	Active (I _{CC})
L	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I _{CC})

Ordering Information

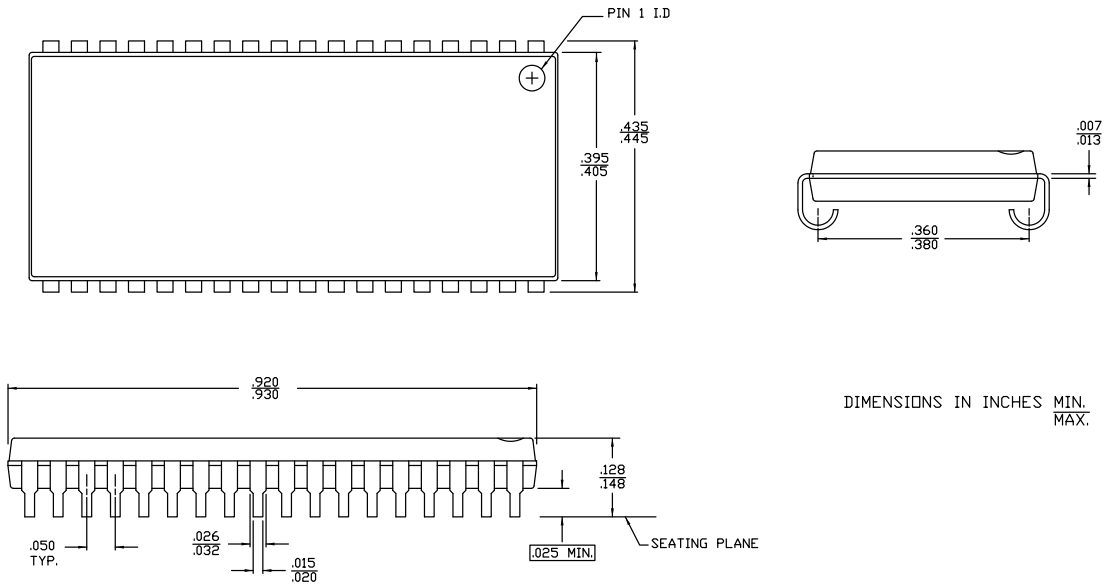
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1010DV33-10VXI	51-85090	36-pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1010DV33-10ZSXI	51-85087	44-pin TSOP II (Pb-free)	

Ordering Code Definitions



Package Diagrams

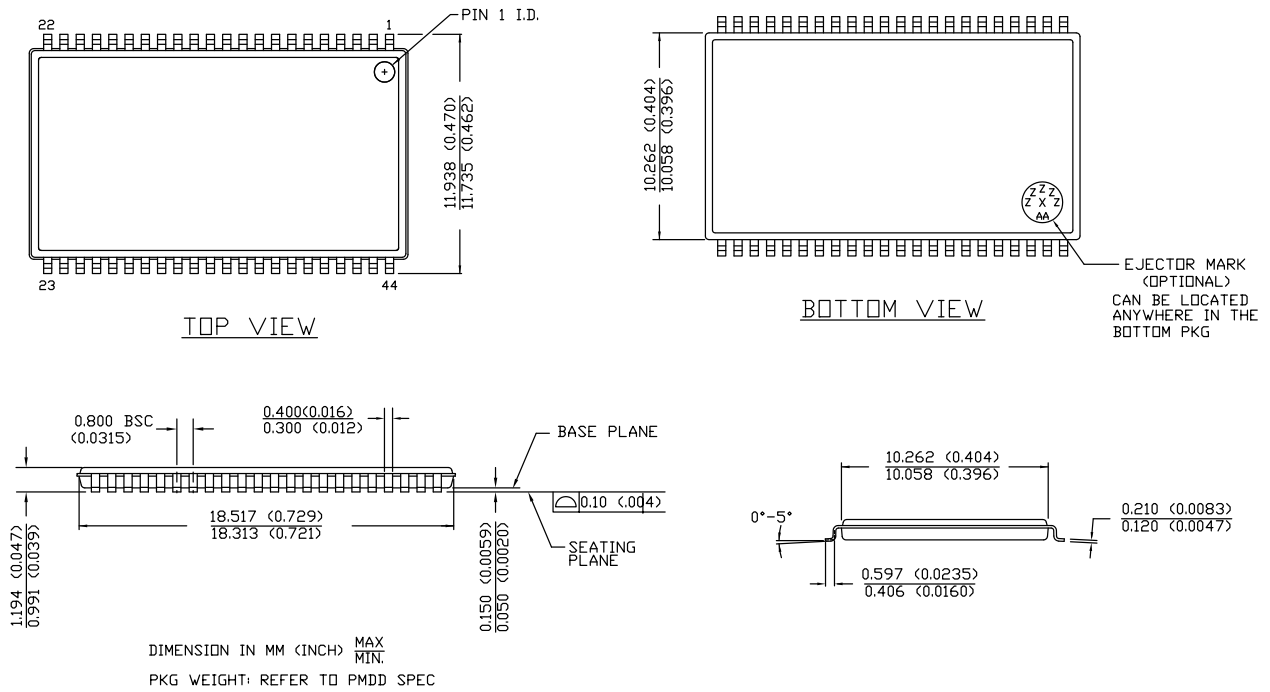
Figure 9. 36-pin SOJ V36.4 (Molded) Package Outline, 51-85090



51-85090 *F

Package Diagrams (continued)

Figure 10. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 *E

Acronyms

Acronym	Description
\overline{CE}	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
\overline{OE}	Output Enable
SOJ	Small Outline J-lead
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
\overline{WE}	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1010DV33, 2-Mbit (256 K × 8) Static RAM				
Document Number: 001-00062				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	342195	See ECN	PCI	New data sheet.
*A	459073	See ECN	NXR	<p>Converted Preliminary to Final.</p> <p>Removed Commercial Operating Range from product offering.</p> <p>Removed -8 ns and -12 speed bin</p> <p>Removed the Pin definitions table.</p> <p>Modified Maximum Ratings for DC input voltage from -0.5V to -0.3V and $V_{CC} + 0.5V$ to $V_{CC} + 0.3V$</p> <p>Changed I_{CC} max from 65 mA to 90 mA</p> <p>Changed the description of I_{IX} from "Input Load Current" to "Input Leakage Current"</p> <p>Updated the Thermal Resistance table.</p> <p>Updated footnote #7 on High-Z parameter measurement</p> <p>Added footnote #12</p> <p>Updated the Ordering Information and replaced Package Name column with Package Diagram in the Ordering Information table.</p>
*B	2602853	11/07/08	VKN / PYRS	Added 36-pin SOJ package and its related information
*C	3059211	10/14/2010	PRAS	<p>Added Ordering Code Definitions.</p> <p>Updated Package Diagrams.</p>
*D	3272897	06/07/2011	AJU	<p>Updated Functional Description (Removed "Refer to the Cypress application note AN1064, SRAM System Guidelines for best practice recommendations.").</p> <p>Added Acronyms and Units of Measure.</p> <p>Updated in new template.</p>
*E	4207615	12/02/2013	MEMJ	<p>Updated Package Diagrams:</p> <p>spec 51-85090 – Changed revision from *E to *F.</p> <p>spec 51-85087 – Changed revision from *C to *E.</p> <p>Updated in new template.</p> <p>Completing Sunset Review.</p>

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC[®] Solutions

[psoc.cypress.com/solutions](#)
[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

Technical Support

[cypress.com/go/support](#)

© Cypress Semiconductor Corporation, 2005-2013. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.