



FEATURES

- Access time : 35/70ns (max.)
- Low power consumption:
Operating : 40/30 mA (typical.)
Standby : 2uA (typ.) L-version
1uA (typ.) LL-version
- Single 5V power supply
- Extended temperature : -20°C~80°C
- All inputs and outputs are TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage : 2V (min.)
- Package : 28-pin 600 mil PDIP
28-pin 330 mil SOP
28-pin 8mmx13.4mm STSOP

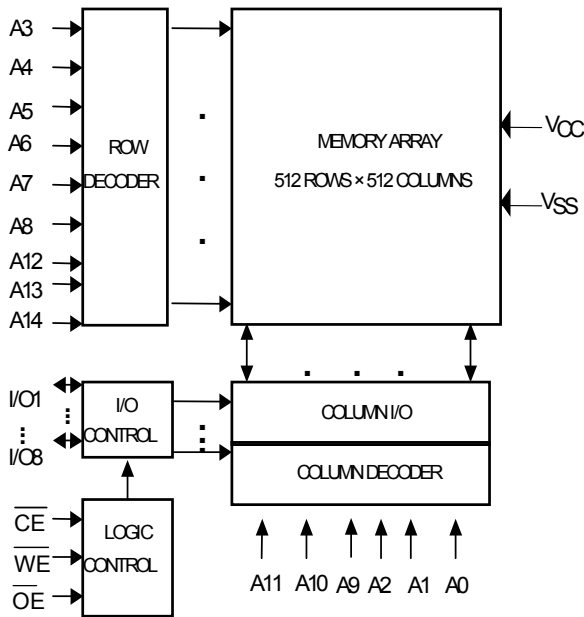
GENERAL DESCRIPTION

The UT62256C(E) is a 262,144-bit low power CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

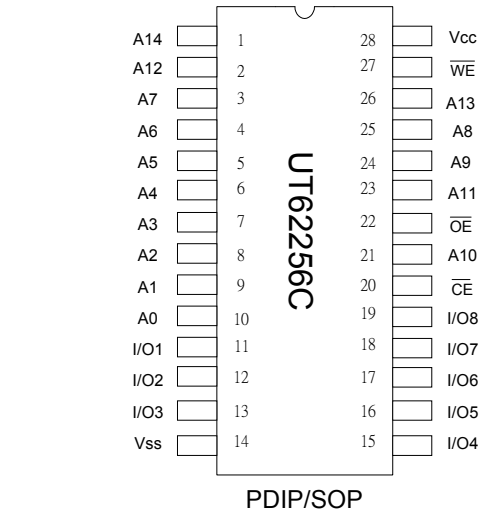
The UT62256C(E) is designed for high-speed and low power application. It is particularly well suited for battery back-up nonvolatile memory application.

The UT62256C(E) operates from a single 5V power supply and all inputs and outputs are fully TTL compatible

FUNCTIONAL BLOCK DIAGRAM

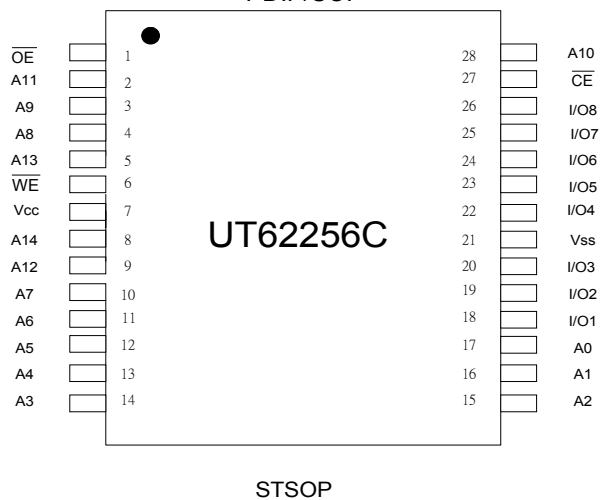


PIN CONFIGURATION



PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|-----------------|---------------------|
| A0 - A14 | Address Inputs |
| I/O1 - I/O8 | Data Inputs/Outputs |
| \overline{CE} | Chip Enable Input |
| \overline{WE} | Write Enable Input |
| \overline{OE} | Output Enable Input |
| V _{CC} | Power Supply |
| V _{SS} | Ground |



**ABSOLUTE MAXIMUM RATINGS***

| PARAMETER | SYMBOL | RATING | UNIT |
|---|--------------|--------------|-------------|
| Terminal Voltage with Respect to V_{SS} | V_{TERM} | -0.5 to +7.0 | V |
| Operating Temperature | T_A | 0 to +70 | $^{\circ}C$ |
| Storage Temperature | T_{STG} | -65 to +150 | $^{\circ}C$ |
| Power Dissipation | P_D | 1 | W |
| DC Output Current | I_{OUT} | 50 | mA |
| Soldering Temperature (under 10 secs) | T_{solder} | 260 | $^{\circ}C$ |

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

| MODE | \overline{CE} | \overline{OE} | \overline{WE} | I/O OPERATION | SUPPLY CURRENT |
|----------------|-----------------|-----------------|-----------------|---------------|----------------------------|
| Standby | H | X | X | High - Z | I_{SB}, I_{SB1} |
| Output Disable | L | H | H | High - Z | I_{CC}, I_{CC1}, I_{CC2} |
| Read | L | L | H | D_{OUT} | I_{CC}, I_{CC1}, I_{CC2} |
| Write | L | X | L | D_{IN} | I_{CC}, I_{CC1}, I_{CC2} |

Note: H = V_{IH} , L = V_{IL} , X = Don't care.

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_A = -20^{\circ}C \sim 80^{\circ}C$)

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|--------------------------------|---|--|------|------|----------------|---------|
| Input High Voltage | V_{IH} | | 2.2 | - | $V_{CC} + 0.5$ | V |
| Input Low Voltage | V_{IL} | | -0.5 | - | 0.8 | V |
| Input Leakage Current | I_{LI} | $V_{SS} \leq V_{IN} \leq V_{CC}$ | -1 | - | 1 | μA |
| Output Leakage Current | I_{LO} | $V_{SS} \leq V_{IO} \leq V_{CC}$ $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ | -1 | - | 1 | μA |
| Output High Voltage | V_{OH} | $I_{OH} = -1mA$ | 2.4 | - | - | V |
| Output Low Voltage | V_{OL} | $I_{OL} = 4mA$ | - | - | 0.4 | V |
| Operating Power Supply Current | I_{CC} | Cycle time=Min | -35 | 40 | 50 | mA |
| | | $\overline{CE} = V_{IL}, I_{IO} = 0mA, .$ | -70 | 30 | 40 | mA |
| | I_{CC1} | Cycle time=1 μs , $\overline{CE} = 0.2V$; $I_{IO} = 0mA$, other pins at 0.2V or $V_{CC} - 0.2V$ | - | - | 10 | mA |
| I_{CC2} | Cycle time=500ns, $\overline{CE} = 0.2V$; $I_{IO} = 0mA$, other pins at 0.2V or $V_{CC} - 0.2V$ | - | - | 20 | mA | |
| Standby Current(TTL) | I_{SB} | $\overline{CE} = V_{IH}$ | - | - | 3 | mA |
| Standby Current(CMOS) | I_{SB1} | $\overline{CE} \geq V_{CC} - 0.2V$ | -L | 2 | 100 | μA |
| | | | -LL | 1 | 50 | μA |

**CAPACITANCE** ($T_A=25^{\circ}\text{C}$, $f=1.0\text{MHz}$)

| PARAMETER | SYMBOL | MIN. | MAX | UNIT |
|--------------------------|-----------|------|-----|------|
| Input Capacitance | C_{IN} | - | 8 | pF |
| Input/Output Capacitance | $C_{I/O}$ | - | 10 | pF |

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

| | |
|--|---|
| Input Pulse Levels | 0V to 3.0V |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | $C_L = 100\text{pF}$, $I_{OH}/I_{OL} = -1\text{mA}/4\text{mA}$ |

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_A = -20^{\circ}\text{C} \sim 80^{\circ}\text{C}$)**(1) READ CYCLE**

| PARAMETER | SYMBOL | UT62256C(E)-35 | | UT62256C(E)-70 | | UNIT |
|------------------------------------|-------------|----------------|------|----------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| Read Cycle Time | t_{RC} | 35 | - | 70 | - | ns |
| Address Access Time | t_{AA} | - | 35 | - | 70 | ns |
| Chip Enable Access Time | t_{ACE} | - | 35 | - | 70 | ns |
| Output Enable Access Time | t_{OE} | - | 25 | - | 35 | ns |
| Chip Enable to Output in Low Z | t_{CLZ}^* | 10 | - | 10 | - | ns |
| Output Enable to Output in Low Z | t_{OLZ}^* | 5 | - | 5 | - | ns |
| Chip Disable to Output in High Z | t_{CHZ}^* | - | 25 | - | 35 | ns |
| Output Disable to Output in High Z | t_{OHZ}^* | - | 25 | - | 35 | ns |
| Output Hold from Address Change | t_{OH} | 5 | - | 5 | - | ns |

(2) WRITE CYCLE

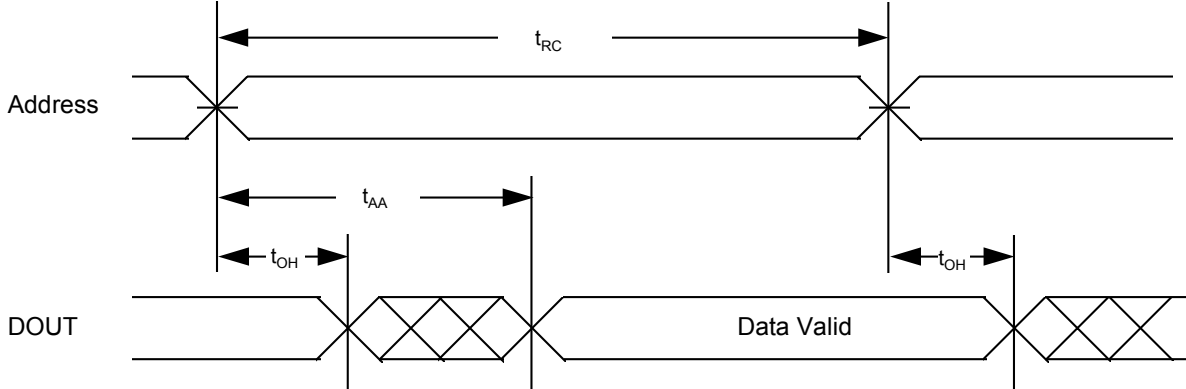
| PARAMETER | SYMBOL | UT62256C(E)-35 | | UT62256C(E)-70 | | UNIT |
|----------------------------------|-------------|----------------|------|----------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| Write Cycle Time | t_{WC} | 35 | - | 70 | - | ns |
| Address Valid to End of Write | t_{AW} | 30 | - | 60 | - | ns |
| Chip Enable to End of Write | t_{CW} | 30 | - | 60 | - | ns |
| Address Set-up Time | t_{AS} | 0 | - | 0 | - | ns |
| Write Pulse Width | t_{WP} | 25 | - | 50 | - | ns |
| Write Recovery Time | t_{WR} | 0 | - | 0 | - | ns |
| Data to Write Time Overlap | t_{DW} | 20 | - | 30 | - | ns |
| Data Hold from End of Write Time | t_{DH} | 0 | - | 0 | - | ns |
| Output Active from End of Write | t_{OW}^* | 5 | - | 5 | - | ns |
| Write to Output in High Z | t_{WHZ}^* | - | 15 | - | 25 | ns |

*These parameters are guaranteed by device characterization, but not production tested.

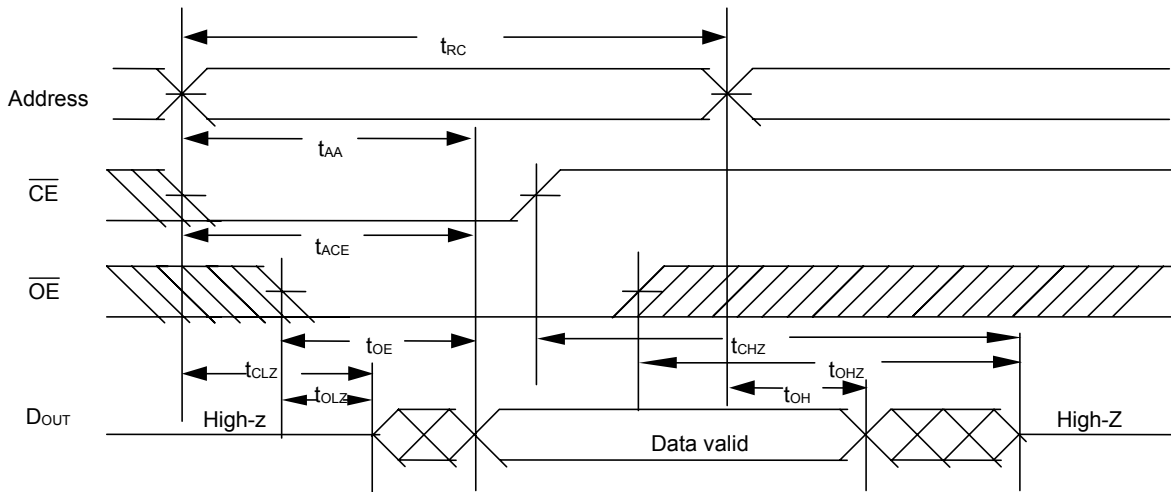


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



READ CYCLE 2 (\overline{CE} and \overline{OE} Controlled) (1,3,5,6)

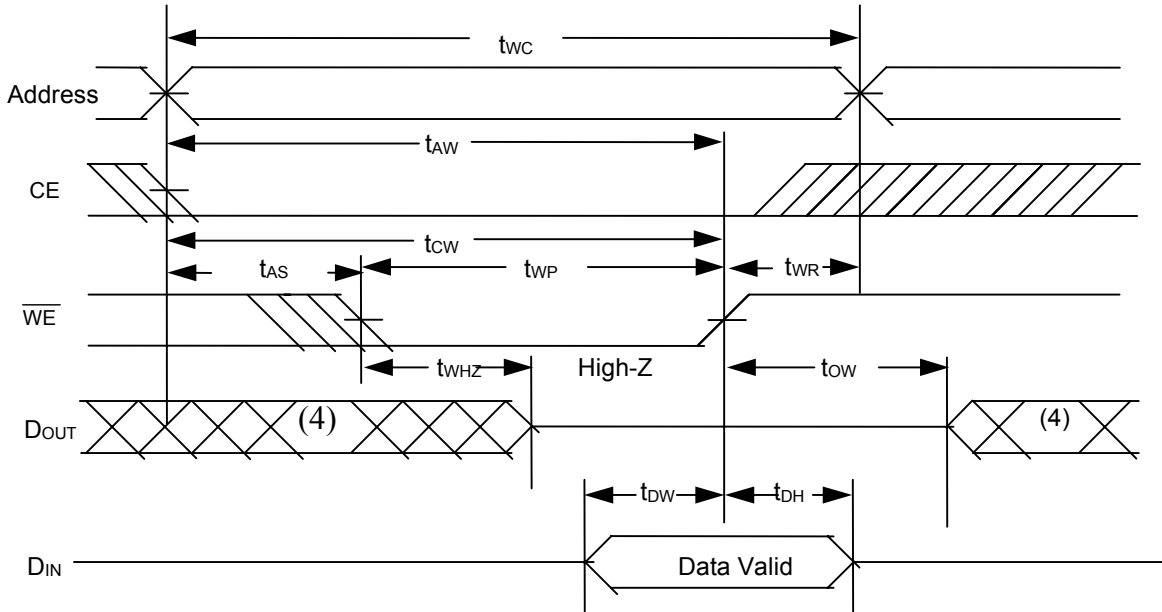


Notes :

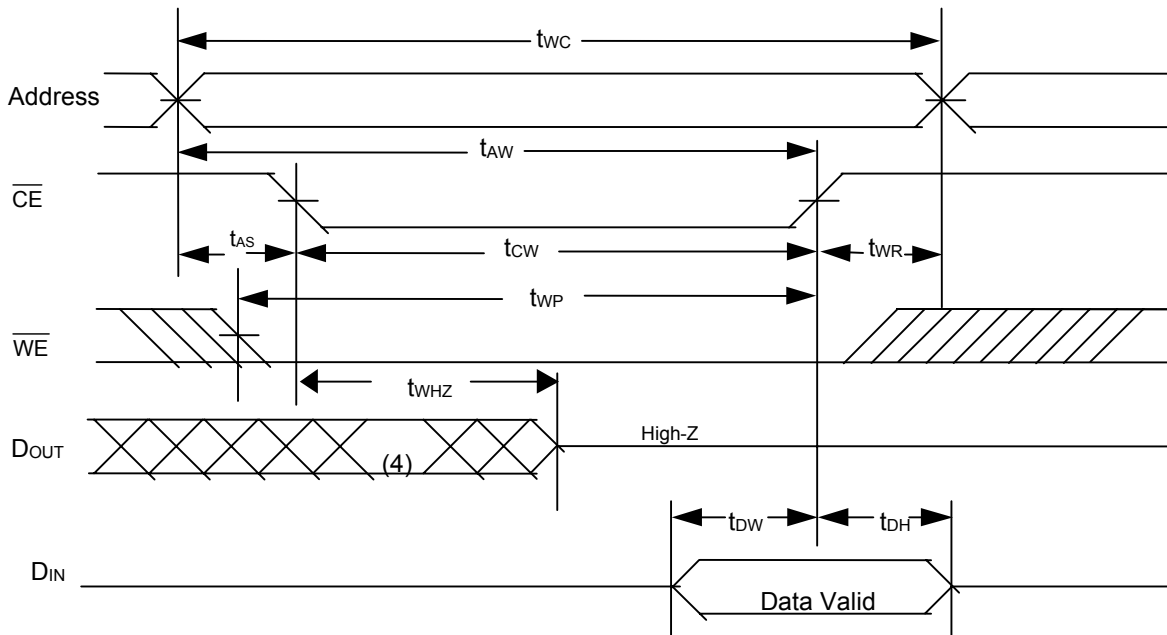
1. \overline{WE} is HIGH for read cycle.
2. Device is continuously selected $\overline{CE} = V_{IL}$.
3. Address must be valid prior to or coincident with \overline{CE} transition; otherwise t_{AA} is the limiting parameter.
4. \overline{OE} is LOW.
5. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
6. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (\overline{WE} Controlled) (1,2,3,5)



WRITE CYCLE 2 (\overline{CE} Controlled) (1,2,5)



Notes :

1. \overline{WE} or \overline{CE} must be HIGH during all address transitions.
2. A write occurs during the overlap of a low \overline{CE} and a low \overline{WE} .
3. During a \overline{WE} controlled with write cycle with \overline{OE} LOW, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the \overline{CE} LOW transition occurs simultaneously with or after \overline{WE} LOW transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.

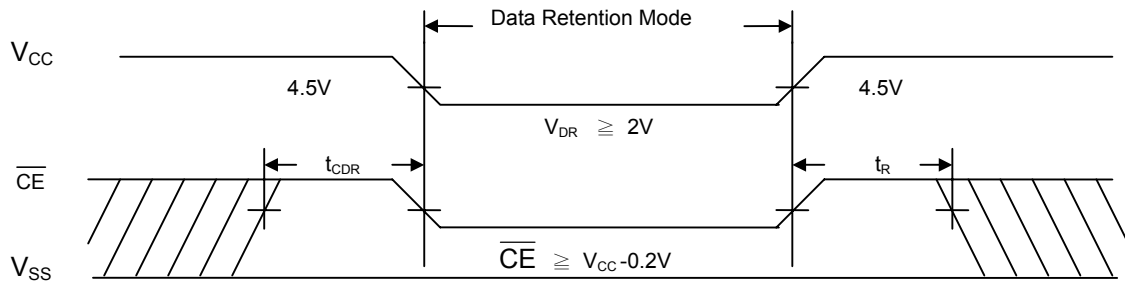


DATA RETENTION CHARACTERISTICS (TA = -20°C~80°C)

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT | |
|-------------------------------------|------------------|---|------------------|------|------|------|----|
| V _{CC} for Data Retention | V _{DR} | $\overline{CE} \geq V_{CC}-0.2V$ | 2.0 | - | 5.5 | V | |
| Data Retention Current | I _{DR} | V _{CC} =3V $\overline{CE} \geq V_{CC}-0.2V$ | - L | - | 1 | 50 | μA |
| | | | - LL | - | 0.5 | 20 | μA |
| Chip Disable to Data Retention Time | t _{CDR} | See Data Retention Waveforms (below) | 0 | - | - | ns | |
| Recovery Time | t _R | | t _{RC*} | - | - | ns | |

t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM





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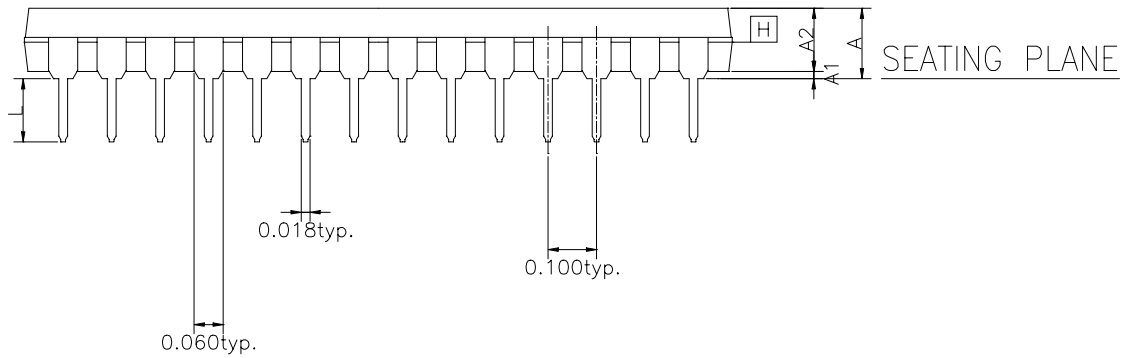
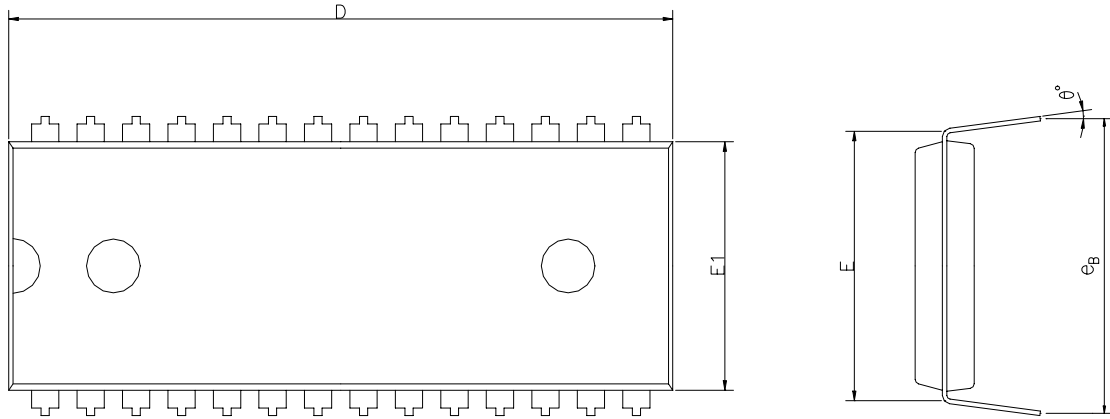
UT62256C(E)

Rev. 1.0

32K X 8 BIT LOW POWER CMOS SRAM

PACKAGE OUTLINE DIMENSION

28 pin 600 mil PDIP PACKAGE OUTLINE DIMENSION



| SYMBOL \ UNIT | INCH(MIN) | INCH(MAX) |
|---------------|-----------|-----------|
| A | - | 0.220 |
| A1 | 0.015 | - |
| D | 1.455 | 1.47 |
| E | 0.6 | 0.6 |
| E1 | 0.54 | 0.54 |
| eB | 0.63 | 0.67 |
| θ | 0° | 15° |

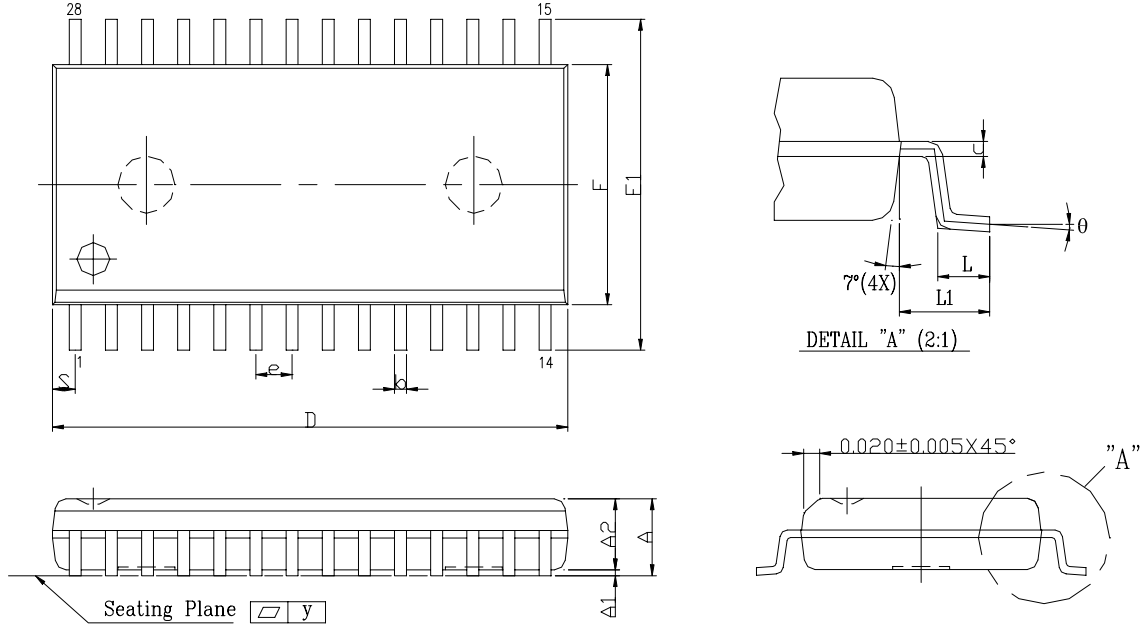


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UT62256C(E)
32K X 8 BIT LOW POWER CMOS SRAM

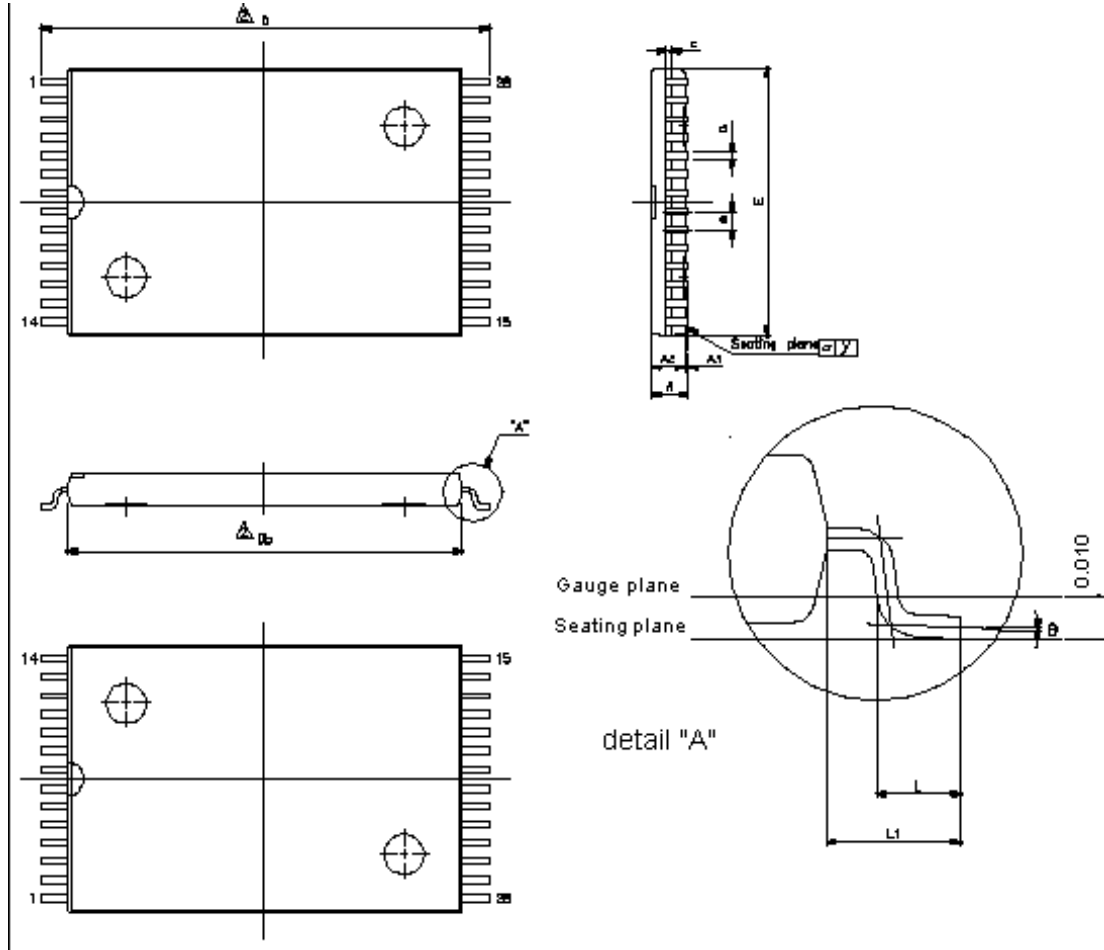
28 pin 330 mil SOP PACKAGE OUTLINE DIMENSION



| SYMBOL | UNIT | INCH(BASE) | MM(REF) |
|--------|------|--------------|--------------|
| A | | 0.120 (MAX) | 3.048 (MAX) |
| A1 | | 0.002(MIN) | 0.05(MIN) |
| A2 | | 0.098±0.005 | 2.489±0.127 |
| b | | 0.0016 (TYP) | 0.406(TYP) |
| c | | 0.010 (TYP) | 0.254(TYP) |
| D | | 0.728 (MAX) | 18.491 (MAX) |
| E | | 0.340 (MAX) | 8.636 (MAX) |
| E1 | | 0.465±0.012 | 11.811±0.305 |
| e | | 0.050 (TYP) | 1.270(TYP) |
| L | | 0.05 (MAX) | 1.270 (MAX) |
| L1 | | 0.067±0.008 | 1.702 ±0.203 |
| S | | 0.047 (MAX) | 1.194 (MAX) |
| y | | 0.003(MAX) | 0.076(MAX) |
| θ | | 0°~10° | 0°~10° |



28 pin 8x13.4mm STSOP PACKAGE OUTLINE DIMENSION



Note :
E dimension is not including end flash
the total of both sides' end flash
is not above 0.3mm.



| SYMBOL | UNIT | INCH(BASE) | MM(REF) |
|--------|------|--------------|------------|
| A | | 0.047 (MAX) | 1.20 (MAX) |
| A1 | | 0.004±0.002 | 0.10±0.05 |
| A2 | | 0.039±0.002 | 1.00±0.05 |
| b | | 0.006 (TYP) | 0.15(TYP) |
| c | | 0.010 (TYP) | 0.254(TYP) |
| Db | | 0.465±0.004 | 11.80±0.10 |
| E | | 0.315±0.004 | 8.00±0.10 |
| e | | 0.022 (TYP) | 0.55(TYP) |
| D | | 0.528±0.008 | 13.40±0.20 |
| L | | 0.020±0.004 | 0.50±0.10 |
| L1 | | 0.0315±0.004 | 0.80±0.10 |
| y | | 0.08(MAX) | 0.003(MAX) |
| θ | | 0°~5° | 0°~5° |



Rev. 1.0

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UT62256C(E) 32K X 8 BIT LOW POWER CMOS SRAM

ORDERING INFORMATION

| PART NO. | ACCESS TIME (ns) | STANDBY CURRENT (μ A) | PACKAGE |
|------------------|---------------------|-------------------------------|-------------|
| UT62256CPC-70E | 70 | 5 mA | 28PIN PDIP |
| UT62256CPC-70LE | 70 | 100 μ A | 28PIN PDIP |
| UT62256CPC-70LLE | 70 | 40 μ A | 28PIN PDIP |
| UT62256CSC-35E | 35 | 5 mA | 28PIN SOP |
| UT62256CSC-35LE | 35 | 100 μ A | 28PIN SOP |
| UT62256CSC-35LLE | 35 | 40 μ A | 28PIN SOP |
| UT62256CSC-70E | 70 | 5 mA | 28PIN SOP |
| UT62256CSC-70LE | 70 | 100 μ A | 28PIN SOP |
| UT62256CSC-70LLE | 70 | 40 μ A | 28PIN SOP |
| UT62256CLS-35LE | 35 | 100 μ A | 28PIN STSOP |
| UT62256CLS-35LLE | 35 | 50 μ A | 28PIN STSOP |
| UT62256CLS-70LE | 70 | 100 μ A | 28PIN STSOP |
| UT62256CLS-70LLE | 70 | 40 μ A | 28PIN STSOP |



Rev. 1.0

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UT62256C(E)
32K X 8 BIT LOW POWER CMOS SRAM

REVISION HISTORY

| REVISION | DESCRIPTION | DATE |
|----------|--------------|-------------|
| Rev. 1.0 | 1. Original. | Sep 3 ,2001 |



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