Analog Sound Processors series

Sound Processor for car audio built-in 2^{nd} order post filter

BD37067FV-M

Structure

It is built-in input selector of 6 stereo source and output to ADC after adjusting signal level. And built-in 2^{nd} order post filter to reduce out of band noise and 6ch Volume circuit. Moreover, it is simple to design set by built-in TDMA noise reduction systems.

Feature

- Built-in differential input selector that can select single-ended / differential input
- Reduce the shock noise when switching gain due to built-in advanced switch circuit
- Decrease the out of band noise of DAC by built-in 2nd order post filter.
- Built-in buffered ground isolation amplifier to realize high CMRR characteristics
- No need to countermeasure using external components built-in TDMA noise reduction circuit
- Package is SSOP-B40. Putting same direction input-terminals and output-terminals make PCB layout easier and PCB area smaller.
- It is possible to control by 3.3V for I^2C-BUS controller
- AEC-Q100 Qualified.

Applications

It is the optimal for the car audio. Besides, it is possible to use for the audio equipment of mini Compo, micro Compo, TV.

Key Specifications

- Total harmonic distortion : 0.003%
- Maximum input voltage : 2.2Vrms(Typ)
- Common mode rejection ratio : 55dB(Min)
- Maximum output voltage : 2.1Vrms(Typ)
- Output noise voltage : 8μVrms(Typ)
- Residual output noise voltage : 2.5μVrms(Typ)
- Ripple rejection: -70dB (Typ)
- Operating temperature range: -40℃ to +85℃

Package

	W(Typ) x D(Typ) x H(Max.)
SSOP-B40	13.60mm x 7.80mm x 2.00mm

SSOP-B40

Typical Application Circuit

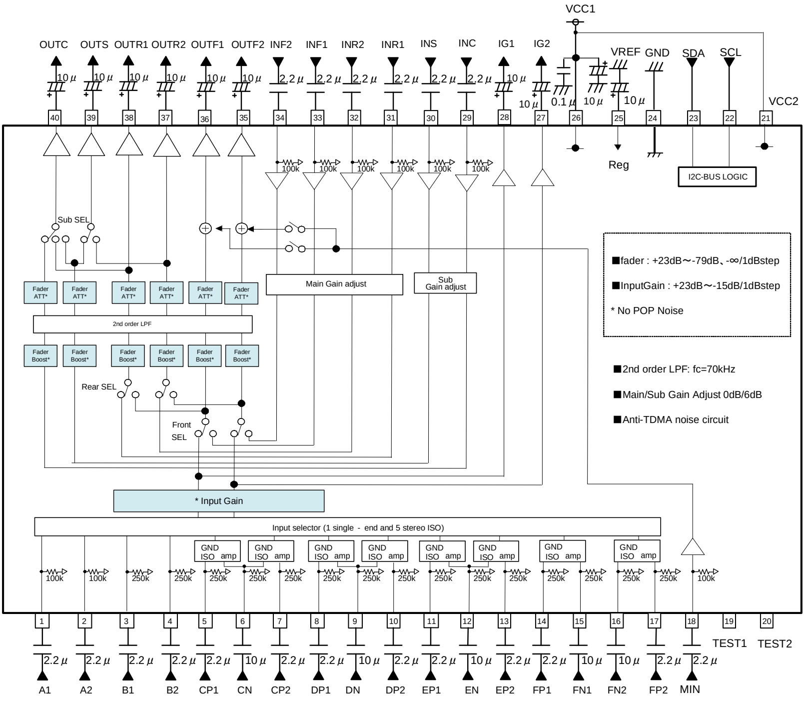


Figure 1. Application Circuit Diagram

○Product structure：Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

Pin Configuration

SSOP-B40
(TOP VIEW)

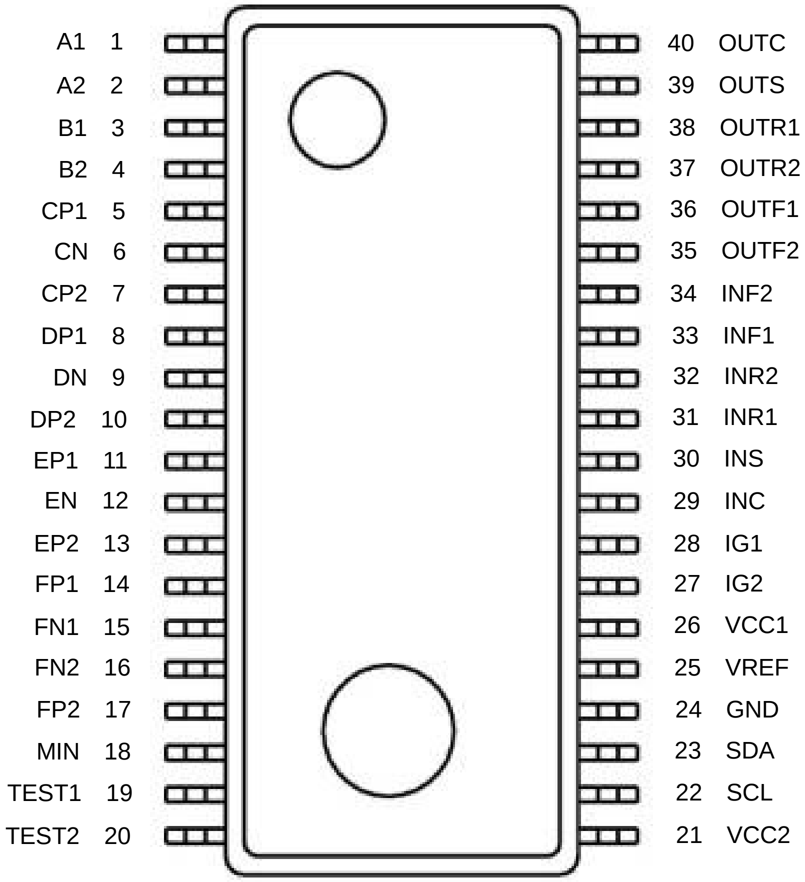


Figure 2. Pin configuration

Descriptions of terminal

Terminal No.	Terminal Name	Description	Terminal No.	Terminal Name	Description
1	A1	A input terminal of 1ch	21	VCC2	VCC2 terminal for power supply
2	A2	A input terminal of 2ch	22	SCL	I^{2}C Communication clock terminal
3	B1	B input terminal of 1ch	23	SDA	I^{2}C Communication data terminal
4	B2	B input terminal of 2ch	24	GND	GND terminal
5	CP1	C positive input terminal of 1ch	25	VREF	BIAS terminal
6	CN	C negative input terminal	26	VCC1	VCC1 terminal for power supply
7	CP2	C positive input terminal of 2ch	27	IG2	Input gain output terminal of 2ch
8	DP1	D positive input terminal of 1ch	28	IG1	Input gain output terminal of 1ch
9	DN	D negative input terminal	29	INC	Center input terminal
10	DP2	D positive input terminal of 2ch	30	INS	Subwoofer input terminal
11	EP1	E positive input terminal of 1ch	31	INR1	Rear input terminal of 1ch
12	EN	E negative input terminal	32	INR2	Rear input terminal of 2ch
13	EP2	E positive input terminal of 2ch	33	INF1	Front input terminal of 1ch
14	FP1	F positive input terminal of 1ch	34	INF2	Front input terminal of 2ch
15	FN1	F negative input terminal of 1ch	35	OUTF2	Front output terminal of 2ch
16	FN2	F negative input terminal of 2ch	36	OUTF1	Front output terminal of 1ch
17	FP2	F positive input terminal of 2ch	37	OUTR2	Rear output terminal of 2ch
18	MIN	Mixing input terminal	38	OUTR1	Rear output terminal of 1ch
19	TEST1	TEST terminal	39	OUTS	Subwoofer output terminal
20	TEST2	TEST terminal	40	OUTC	Center output terminal

Terminal layout drawing

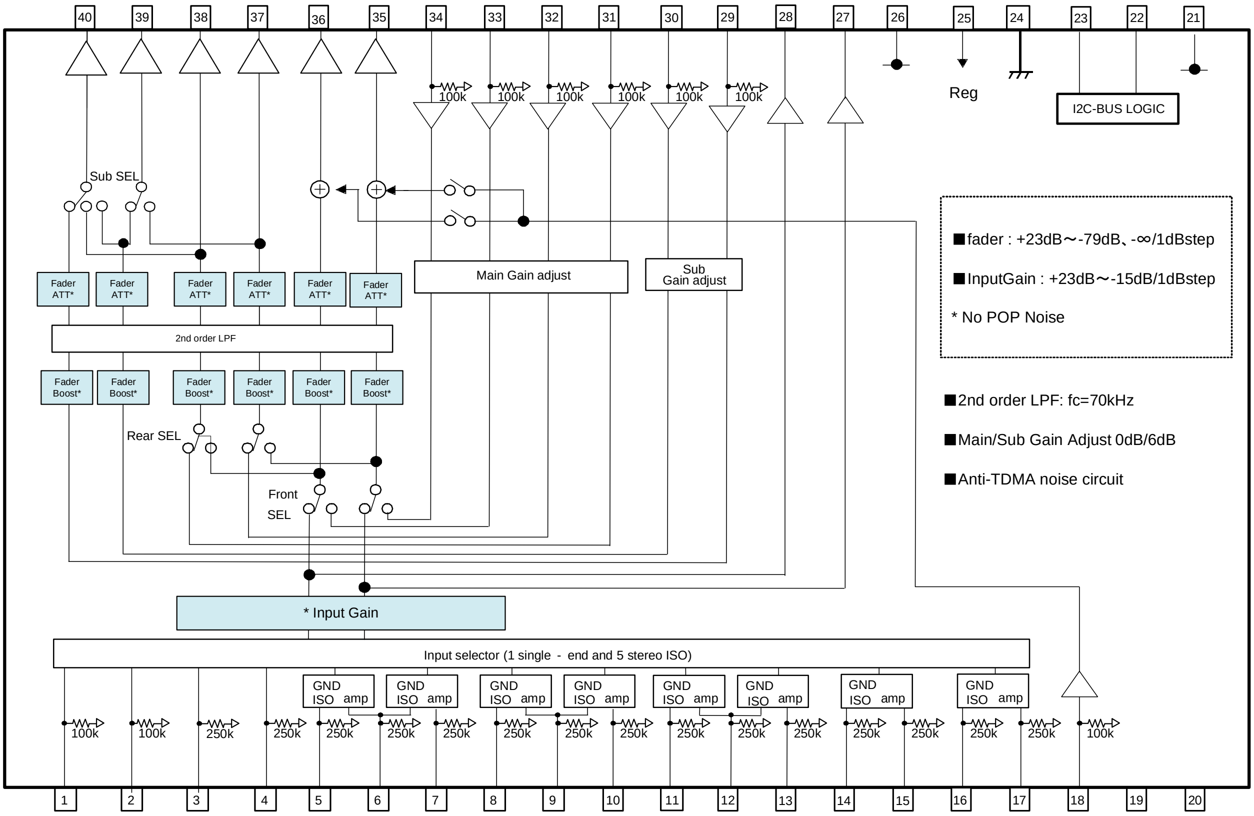


Figure 3. Block diagram and pin assign

Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Rating	Unit
Power supply Voltage	VCC (VCC1,2)	10	V
Input voltage	Vin	VCC+0.3 to GND-0.3 Only SCL, SDA 7 to GND-0.3	V
Power Dissipation	Pd	1.125 ※1	W
Storage Temperature	Tastg	-55 to +150	℃

※1 This value decreases 9mW/℃ for Ta=25℃ or more.
ROHM standard board shall be mounted. Thermal resistanceθja = 111.1(℃/W)。
ROHM Standard board size：70x70x1.6(㎣)
material：A FR4 grass epoxy board(3% or less of copper foil area)

Operating Range

Item	Symbol	MIN	TYP	MAX	Unit
Power supply Voltage	VCC (VCC1,2)	7.0	8.5	9.5	V
Temperature	Topr	-40	-	+85	℃

Electrical Characteristic

(Unless specified particularly, Ta=25℃, VCC1,2=8.5V, f=1kHz, Vin=1Vrms, Rg=600Ω, RL=10kΩ,
A input, Input gain 0dB, Gain Adjust +6dB, LPF ON, Fader 0dB, Input point=A1/A2, Monitor point=IG1/IG2)

BLOCK	Item	Symbol	Limit			Unit	Condition
			Min	Typ	Max		
GENERAL	Current upon no signal (VCC1+VCC2)	I_{Q_VCC}	—	35	53	mA	No signal
INPUT SELECTOR	Input impedance (A)	R_{IN_S}	70	100	130	kΩ	
	Input impedance (B, C, D, E, F)	R_{IN_D}	175	250	325	kΩ	
	Voltage gain	G_V	-1.5	+0	+1.5	dB	Gv=20log(VOUT/VIN)
	Channel balance	CB	-1.5	+0	+1.5	dB	CB = GV1-GV2
	Total harmonic distortion	THD+N	—	0.003	0.05	%	VOUT=1Vrms BW=400-30KHz
	Output noise voltage	V_{NO1}	—	3.1	8.0	μVrms	Rg = 0Ω BW = IHF-A
	Maximum input voltage	V_{IM}	2.0	2.2	—	Vrms	VIM at THD+N(VOUT)=1% BW=400-30KHz
	Cross-talk between channels	CTC	—	-100	-90	dB	Rg = 0Ω CTC=20log(VOUT/VOUT´) BW = IHF-A
	Cross-talk between selectors	CTS	—	-100	-90	dB	Rg = 0Ω CTS=20log(VOUT/VOUT´) BW = IHF-A
	Common mode rejection ratio (C, D, E, F)	CMRR	55	65	—	dB	XP1 and XN input XP2 and XN input CMRR=20log(VIN/VOUT) BW = IHF-A, [X=C,D,E,F]
INPUT GAIN	Minimum input gain	$G_{IN\ MIN}$	-17	-15	-13	dB	Input gain -15dB VIN=100mVrms Gin=20log(VOUT/VIN)
	Maximum input gain	$G_{IN\ MAX}$	21	23	25	dB	Input gain 23dB VIN=100mVrms Gin=20log(VOUT/VIN)
	Gain set error	$G_{IN\ ERR}$	-2	+0	+2	dB	GAIN=-15 to +23dB
	Output impedance	R_{OUT}	-	—	50	Ω	VIN=100mVrms
	Maximum output voltage	V_{OM}	2.0	2.2	—	Vrms	THD+N=1% BW=400-30KHz

(Unless specified particularly, Ta=25℃, VCC1,2=8.5V, f=1kHz, Vin=0.9Vrms, Rg=600Ω, RL=10kΩ,
A input, Input gain 0dB, Gain Adjust +6dB, LPF ON, Fader 0dB,
Input point=INF1/INF2/INR1/INR2/INC/INS, Monitor point=OUTF1/OUTF2/OUTR1/OUTR2/OUTC/OUTS)

BLOCK	Item	Symbol	Limit			Unit	Condition
			Min	Typ	Max		
OUTPUT	output impedance	R_{OUT}	-	—	50	Ω	VIN=100mVrms
	Maximum output voltage	V_{OM}	2.0	2.1	—	Vrms	THD+N=1% BW=400-30KHz

(Unless specified particularly, Ta=25℃, VCC1,2=8.5V, f=1kHz, Vin=0.9Vrms, Rg=600Ω, RL=10kΩ,
A input, Input gain 0dB, Gain Adjust +6dB, LPF ON, Fader 0dB,
Input point=INF1/INF2/INR1/INR2/INC/INS, Monitor point=OUTF1/OUTF2/OUTR1/OUTR2/OUTC/OUTS)

BLOCK	Item	Symbol	Limit			Unit	Condition
			Min	Typ	Max		
FADER	Maximum boost gain	$G_{F\ BST}$	21	23	25	dB	Gain=23dB V_{IN}=100mVrms G_F=20log(VOUT/VIN)-G_{Hout} Gain Adjust=0dB
	Channel balance	CB	-1.5	+0	+1.5	dB	CB = GV1-GV2
	Total harmonic distortion	THD+N	―	0.003	0.05	%	BW=400-30KHz
	Output noise voltage	V_{NO1}	―	8	16	μVrms	Rg = 0Ω BW = IHF-A
	Residual output noise voltage	V_{NOR}	―	2.5	8.0	μVrms	Fader = -∞dB Rg = 0Ω BW = IHF-A
	Maximum input voltage	V_{IM}	2.0	2.1	―	Vrms	VIM at THD+N(VOUT)=1% BW=400-30KHz Gain Adjust = 0dB
	Cross-talk between channels	CTC	―	-100	-90	dB	Rg = 0Ω CTC=20log(VOUT/VOUT´) BW = IHF-A
	Maximum attenuation	$G_{F\ MIN}$	―	-100	-90	dB	Fader = -∞dB G_F=20log(VOUT/VIN) BW = IHF-A
	Gain set error	$G_{F\ ERR}$	-2	+0	+2	dB	Gain=+1 to +23dB
	Attenuation set error 1	$G_{F\ ERR1}$	-2	+0	+2	dB	ATT=0 to -15dB
	Attenuation set error 2	$G_{F\ ERR2}$	-3	+0	+3	dB	ATT=-16 to -47dB
	Attenuation set error 3	$G_{F\ ERR3}$	-4	+0	+4	dB	ATT=-48 to -79dB
	Ripple rejection	RR_{VCC}	―	-70	-40	dB	f=1kHz V_{RR}=100mVrms RR_{VCC}=20log(VOUT /VCC)
	Fader attenuation	G_{MINF}	―	-105	-85	dB	Fader -∞dB Gmute=20log(VOUT/VIN) BW = IHF-A
MIXING	Input impedance	R_{IN_M}	70	100	130	kΩ	
	Maximum input voltage	V_{IM_M}	2.0	2.2	-	Vrms	VIM at THD+N(VOUT)=1% BW=400-30KHz MIN input
	Maximum attenuation	$G_{MX\ MIN}$	-	-100	-85	dB	MIX=OFF G_{MX}=20log(VOUT/VIN) BW=IHF-A MIN input
	Mixing gain	G_{MX}	-2	+0	+2	dB	MIX=ON G_{MX}=20log(VOUT/VIN)-G_{Hout}
GAIN ADJUST	Input impedance	R_{IN_M}	70	100	130	kΩ	
	Boost gain	$G_{F\ BST}$	4	6	8	dB	Gain=6dB V_{IN}=100mVrms G_F=20log(VOUT/VIN)-G_{Hout}
	Channel balance	CB	-1.5	+0	+1.5	dB	CB = GV1-GV2

※Phase between input / output is same.

Typical Performance Curve(s)

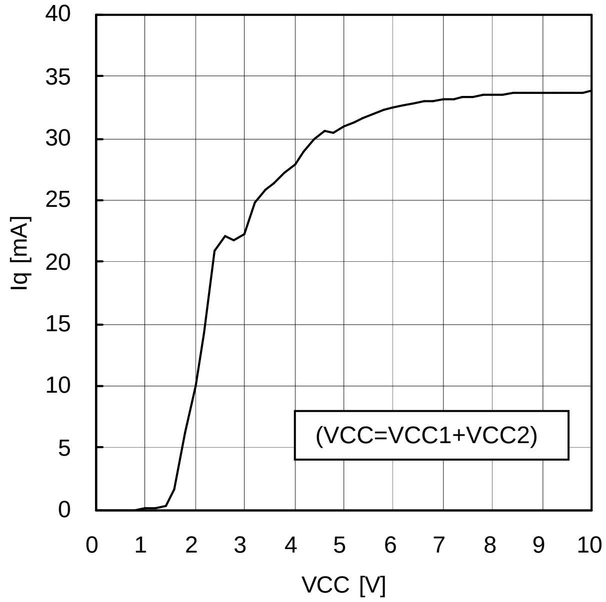


Figure 4. VCC vs Iq

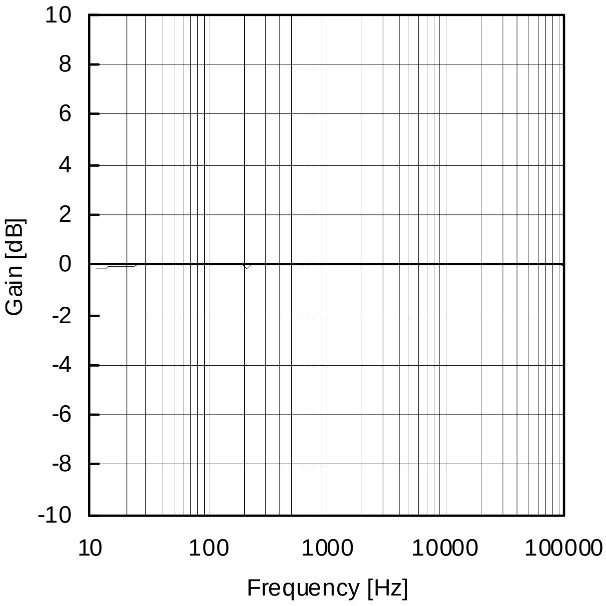


Figure 5. Gain vs frequency

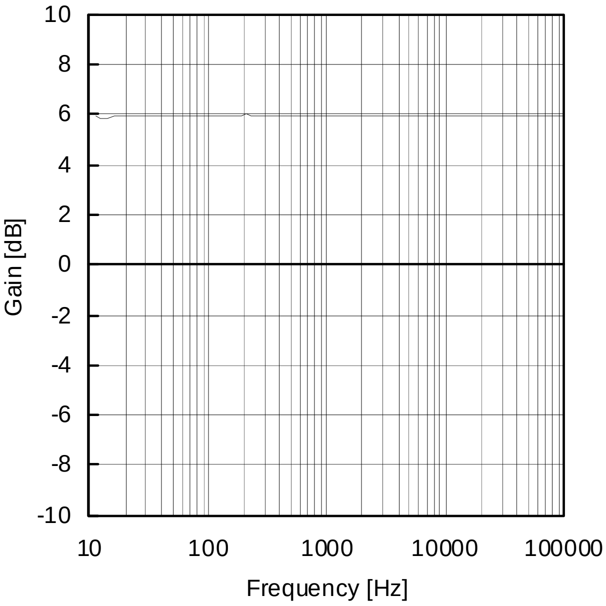


Figure 6. Gain vs frequency
(Gain Adjust=+6dB)

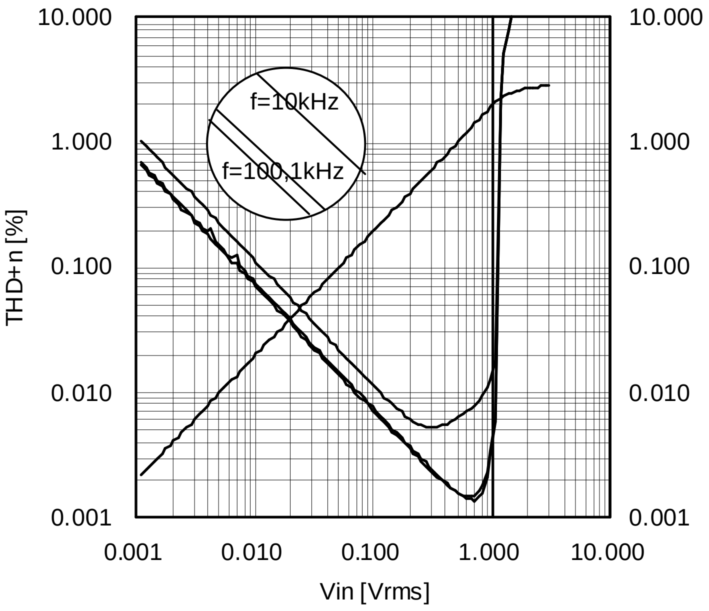


Figure 7. THD+n vs VIN / VO
(Gain Adjust=+6dB)

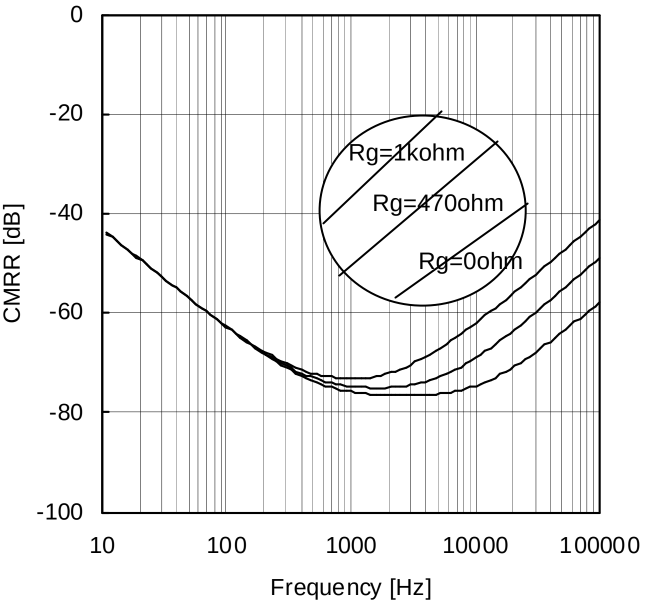


Figure 8. CMRR

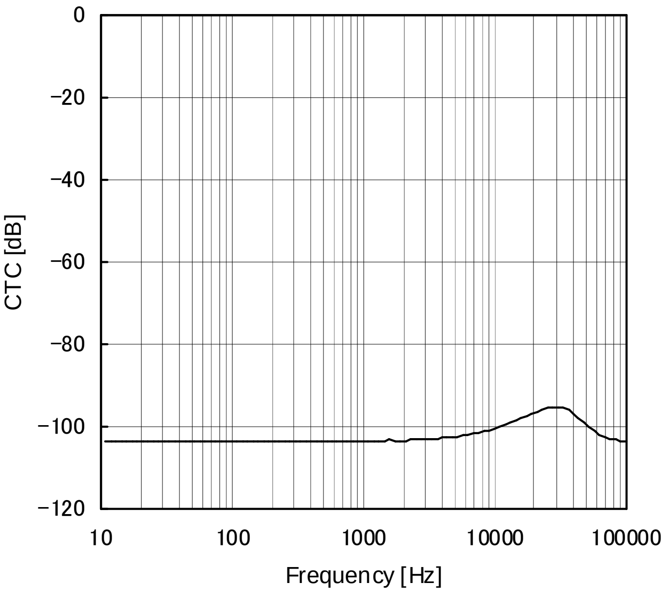


Figure 9. CTC

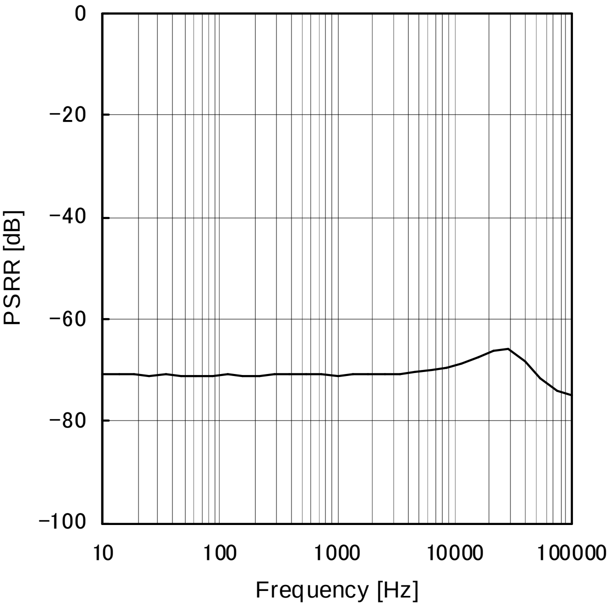


Figure 10. PSRR

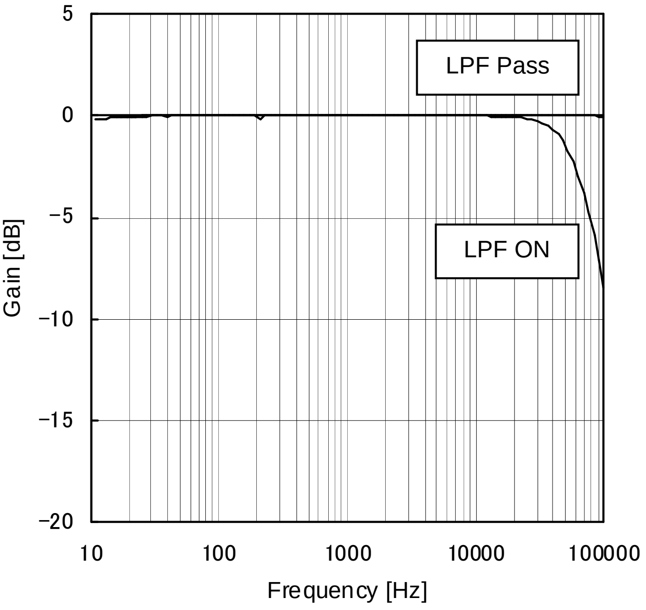


Figure 11. LPF ON/pass

I^{2}C-BUS CONTROL SIGNAL SPECIFICATION

(1) Electrical specifications and timing for bus lines and I/O stages

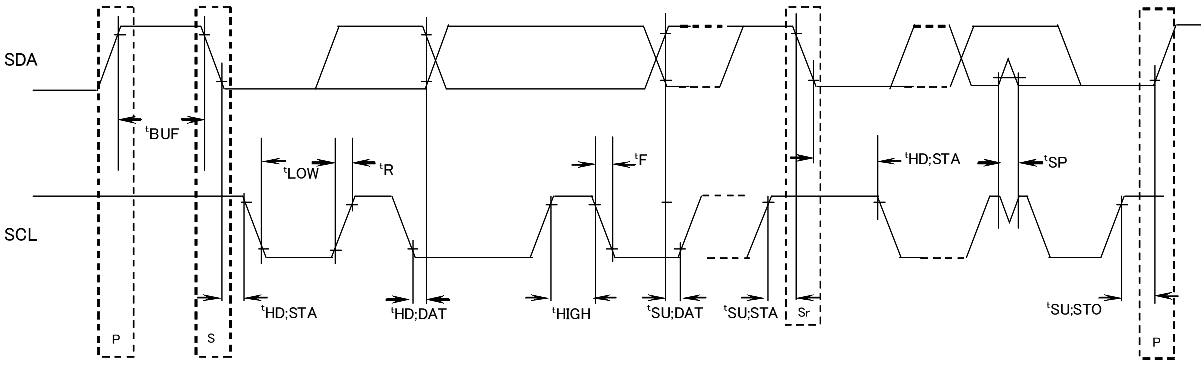


Figure 12. Definition of timing on the I^{2}C-BUS

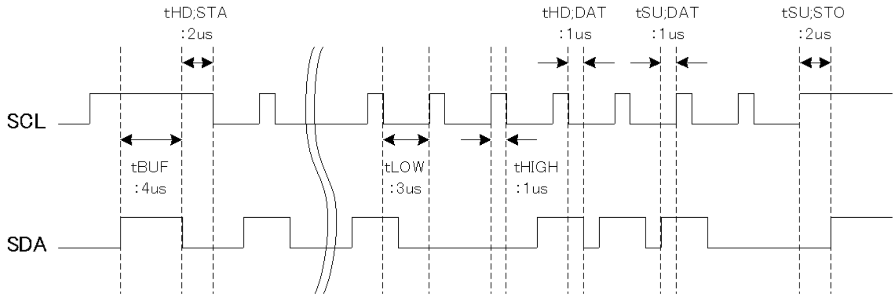
Table 1 Characteristics of the SDA and SCL bus lines for I^{2}C-BUS devices

Parameter		Symbol	Fast-mode I^{2}C-BUS		Unit
			Min.	Max.	
1	SCL clock frequency	fSCL	0	400	kHz
2	Bus free time between a STOP and START condition	tBUF	1.3	―	μs
3	Hold time (repeated) START condition. After this period, the first clock pulse is generated	tHD;STA	0.6	―	μs
4	LOW period of the SCL clock	tLOW	1.3	―	μs
5	HIGH period of the SCL clock	tHIGH	0.6	―	μs
6	Set-up time for a repeated START condition	tSU;STA	0.6	―	μs
7	Data hold time	tHD;DAT	0*	―	μs
8	Data set-up time	tSU;DAT	100	―	ns
9	Set-up time for STOP condition	tSU;STO	0.6	―	μs

All values referred to VIH min. and VIL max. Levels (see Table 2).

Table 2 Characteristics of the SDA and SCL I/O stages for I^{2}C-BUS devices

Parameter		Symbol	Fast-mode I^{2}C-BUS		Unit
			Min.	Max.	
10	LOW level input voltage: Fixed input levels	VIL	-0.5	1	V
11	HIGH level input voltage: Fixed input levels	VIH	2.3	-	V
12	Pulse width of spikes, which must be suppressed by the input filter.	tSP	0	50	ns
13	LOW level output voltage (open drain or open collector): At 3mA sink current	VOL1	0	0.4	V
14	Input current each I/O pin with an input voltage between 0.4V and 0.9 VDD max.	Ii	-10	10	μA



SCL clock frequency:250kHz

Figure 13. I^{2}C data transmission timing

(2) I^{2}C-BUS FORMAT

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	P
1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit

S	= Start conditions (Recognition of start bit)
Slave Address	= Recognition of slave address. 7 bits in upper order are voluntary. The least significant bit is “L” due to writing.
A	= ACKNOWLEDGE bit (Recognition of acknowledgement)
Select Address	= Select every of volume, bass and treble.
Data	= Data on every volume and tone.
P	= Stop condition (Recognition of stop bit)

(3) I^{2}C-BUS Interface Protocol

1)Basic form

S	Slave Address	A	Select Address	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		

2）Automatic increment (Select Address increases (+1) according to the number of data.)

S	Slave Address	A	Select Address	A	Data1	A	Data2	A	‥‥	DataN	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB			MSB LSB		

(Example)① Data1 shall be set as data of address specified by Select Address.
② Data2 shall be set as data of address specified by Select Address +1.
③ DataN shall be set as data of address specified by Select Address +N-1.

3）Configuration unavailable for transmission (In this case, only Select Address1 is set.)

S	Slave Address	A	Select Address1	A	Data	A	Select Address 2	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB		MSB LSB		

（Note）If any data is transmitted as Select Address 2 next to data,
It is recognized as data, not as Select Address 2.

(4) Slave address

MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	0	0

80H

(5) Select Address & Data

Items	Select Address (hex)	MSB	Data						LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Initial setup 1	01	Advanced switch ON/OFF	0	Advanced switch time of Input Gain/Fader		0	0	0	0
Initial setup 2	02	0	0	Sub selector		0	0	Rear selector	Front selector
Input Selector	05	0	0	0	0	Input selector			
Input gain	06	0	0	Input Gain					
Fader 1ch Front	28	Fader Gain / Attenuation							
Fader 2ch Front	29	Fader Gain / Attenuation							
Fader 1ch Rear	2A	Fader Gain / Attenuation							
Fader 2ch Rear	2B	Fader Gain / Attenuation							
Fader Center	2C	Fader Gain / Attenuation							
Fader Subwoofer	2D	Fader Gain / Attenuation							
LPF setup Mixing	30	Front mixing ON/OFF	LPF fc	0	0	0	0	Sub Gain adjust	Main Gain adjust
System Reset	FE	1	0	0	0	0	0	0	1

▨ Advanced switch

Notes on data format

1. In function changing of the hatching part, it works advanced switch.

2. Upon continuous data transfer, the Select Address is circulated by the automatic increment function, as shown below.

→01→02→05→06→28→29→2A→2B→2C→2D→30

3. For the function of input selector, it is not corresponded for advanced switch. Therefore, please apply mute on the side of a set when changes these setting.

4. Such as when switching to the IC input selector set to be -∞, sending data without careful consideration of advanced switch time.

Select address 01 (hex)

Mode	MSB	※ Advanced switch time of Input gain/Fader					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
4.7 msec	Advanced Switch ON/OFF	0	0	0	0	0	0	0
7.1 msec			0	1				
11.2 msec			1	0				
14.4 msec			1	1				

Mode	MSB	Advanced switch ON/OFF						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	0	Advanced switch time of Input gain/Fader		0	0	0	0
ON	1							

Select address 02 (hex)

Mode	MSB	Front Selector						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
FRONT	0	0	Sub Selector		0	0	Rear Selector	0
INSIDE THROUGH								1

Mode	MSB	Rear Selector						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
REAR	0	0	Sub Selector		0	0	0	Front Selector
FRONT COPY							1	

Mode※1	MSB	Sub Selector						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Cch(Sub)/Sch(Sub)	0	0	0	0	0	0	Rear Selector	Front Selector
Cch(R1)/Sch(R2)			0	1				
Cch(INC)/Sch(INS)			1	0				
Prohibition			1	1				

※1.SUB terminals output description signal inside ( ).

▒ : Initial condition

Select address 05(hex)

Mode	MSB			Input Selector				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
A	0	0	0	0	0	0	0	0
B					0	0	0	1
C single					0	0	1	0
D single					0	0	1	1
E single					0	1	0	0
F single					0	1	0	1
C diff					0	1	1	0
D diff					0	1	1	1
E diff					1	0	0	0
F full-diff					1	0	0	1
Prohibition					1	0	1	0
					:	:	:	:
					1	1	1	1

▨ : Initial condition

List of active input terminal when set input selector

Mode	Lch positive input terminal	Lch negative input terminal	Rch positive input terminal	Rch negative input terminal
A	1pin(A1)	-	2pin(A2)	-
B	3pin(B1)	-	4pin(B2)	-
C single	5pin(CP1)	-	7pin(CP2)	-
D single	8pin(DP1)	-	10pin(DP2)	-
E single	11pin(EP1)	-	13pin(EP2)	-
F single	14pin(FP1)	-	17pin(FP2)	-
C diff	5pin(CP1)	6pin(CN)	7pin(CP2)	6pin(CN)
D diff	8pin(DP1)	9pin(DN)	10pin(DP2)	9pin(DN)
E diff	11pin(EP1)	12pin(EN)	13pin(EP2)	12pin(EN)
F full-diff	14pin(FP1)	15pin(FN1)	17pin(FP2)	16pin(FN2)

Select address 06 (hex)

Mode	MSB			Input Gain			LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Prohibition	0	0	0	0	0	0	0	0
			:	:	:	:	:	:
			0	0	1	0	0	0
+23dB			0	0	1	0	0	1
+22dB			0	0	1	0	1	0
+21dB			0	0	1	0	1	1
+20dB			0	0	1	1	0	0
+19dB			0	0	1	1	0	1
+18dB			0	0	1	1	1	0
+17dB			0	0	1	1	1	1
+16dB			0	1	0	0	0	0
+15dB			0	1	0	0	0	1
+14dB			0	1	0	0	1	0
+13dB			0	1	0	0	1	1
+12dB			0	1	0	1	0	0
+11dB			0	1	0	1	0	1
+10dB			0	1	0	1	1	0
+9dB			0	1	0	1	1	1
+8dB			0	1	1	0	0	0
+7dB			0	1	1	0	0	1
+6dB			0	1	1	0	1	0
+5dB			0	1	1	0	1	1
+4dB			0	1	1	1	0	0
+3dB			0	1	1	1	0	1
+2dB			0	1	1	1	1	0
+1dB			0	1	1	1	1	1
0dB			1	0	0	0	0	0
-1dB			1	0	0	0	0	1
-2dB			1	0	0	0	1	0
-3dB			1	0	0	0	1	1
-4dB			1	0	0	1	0	0
-5dB			1	0	0	1	0	1
-6dB			1	0	0	1	1	0
-7dB			1	0	0	1	1	1
-8dB			1	0	1	0	0	0
-9dB			1	0	1	0	0	1
-10dB			1	0	1	0	1	0
-11dB			1	0	1	0	1	1
-12dB			1	0	1	1	0	0
-13dB			1	0	1	1	0	1
-14dB			1	0	1	1	1	0
-15dB			1	0	1	1	1	1
Prohibition			1	1	0	0	0	0
			:	:	:	:	:	:
			1	1	1	1	1	1

▨ : Initial condition

Select address 28, 29, 2A, 2B, 2C, 2D (hex)

Gain & ATT	MSB			Fader Gain / Attenuation				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Prohibition	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1
	:	:	:	:	:	:	:	:
	0	1	1	0	1	0	0	0
+23dB	0	1	1	0	1	0	0	1
+22dB	0	1	1	0	1	0	1	0
+21dB	0	1	1	0	1	0	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
+10dB	0	1	1	1	0	1	1	0
+9dB	0	1	1	1	0	1	1	1
+8dB	0	1	1	1	1	0	0	0
+7dB	0	1	1	1	1	0	0	1
+6dB	0	1	1	1	1	0	1	0
+5dB	0	1	1	1	1	0	1	1
+4dB	0	1	1	1	1	1	0	0
+3dB	0	1	1	1	1	1	0	1
+2dB	0	1	1	1	1	1	1	0
+1dB	0	1	1	1	1	1	1	1
0dB	1	0	0	0	0	0	0	0
-1dB	1	0	0	0	0	0	0	1
-2dB	1	0	0	0	0	0	1	0
-3dB	1	0	0	0	0	0	1	1
: :	: :	: :	: :	: :	: :	: :	: :	: :
-78dB	1	1	0	0	1	1	1	0
-79dB	1	1	0	0	1	1	1	1
Prohibition	1	1	0	1	0	0	0	0
	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	0
-∞dB	1	1	1	1	1	1	1	1

▨ : Initial condition

Select address 30(hex)

Mode	MSB			Main Gain Adjust				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	Front Mixing	LPF fc	0	0	0	0	Sub Gain Adjust	0
+6dB								1

Mode	MSB			Sub Gain Adjust				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	Front Mixing	LPF fc	0	0	0	0	0	Main Gain Adjust
+6dB							1	

Mode	MSB			LPF fc				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
70kHz	Front Mixing	0	0	0	0	0	Sub Gain Adjust	Main Gain Adjust
PASS		1						

Mode	MSB			Front Mixing				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	LPF fc	0	0	0	0	Sub Gain Adjust	Main Gain Adjust
ON	1							

▨ : Initial condition

(6) About power on reset

At on of supply voltage circuit made initialization inside IC is built-in. Please send data to all address as initial data at supply voltage on. And please supply mute at set side until this initial data is sent.

Item	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Rise time of VCC1,2	Trise	33	ー	ー	usec	VCC rise time from 0V to 5V
VCC1,2 voltage of release power on reset	Vpor	ー	4.1	ー	V	

(7) About start-up and power off sequence on IC

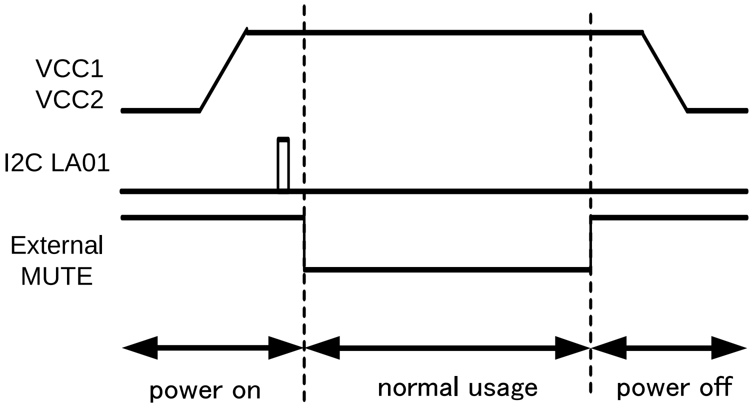


Figure 14. Power off and start-up sequence in each mode

I^2C LA01 is to send data to address LA01 immediately after start-up, set the active state of the IC. Therefore, this command must always send in start-up sequence. In addition, External MUTE means recommended period that the muting outside IC.

About output terminal(27,28,35 to 40pin) vs. VCC

Bias voltage of output terminal (27,28,35 to 40pin) keep fixed voltage in operational range of VCC.

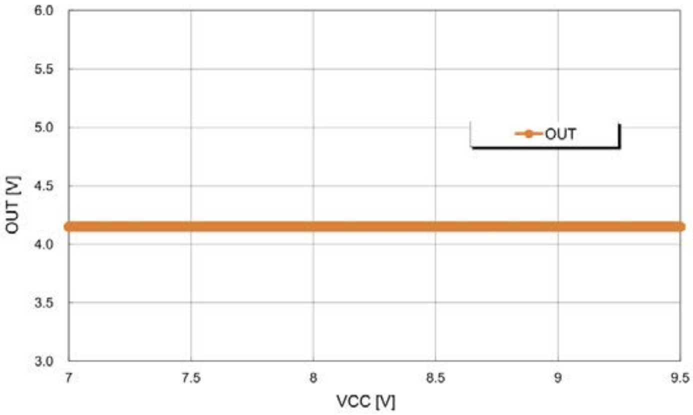


Figure 15. OUT(27,28,35～40pin)_DC-Bias = 4.15V fixed.

Fader volume attenuation of the details

(dB)	D7	D6	D5	D4	D3	D2	D1	D0
+23	0	1	1	0	1	0	0	1
+22	0	1	1	0	1	0	1	0
+21	0	1	1	0	1	0	1	1
+20	0	1	1	0	1	1	0	0
+19	0	1	1	0	1	1	0	1
+18	0	1	1	0	1	1	1	0
+17	0	1	1	0	1	1	1	1
+16	0	1	1	1	0	0	0	0
+15	0	1	1	1	0	0	0	1
+14	0	1	1	1	0	0	1	0
+13	0	1	1	1	0	0	1	1
+12	0	1	1	1	0	1	0	0
+11	0	1	1	1	0	1	0	1
+10	0	1	1	1	0	1	1	0
+9	0	1	1	1	0	1	1	1
+8	0	1	1	1	1	0	0	0
+7	0	1	1	1	1	0	0	1
+6	0	1	1	1	1	0	1	0
+5	0	1	1	1	1	0	1	1
+4	0	1	1	1	1	1	0	0
+3	0	1	1	1	1	1	0	1
+2	0	1	1	1	1	1	1	0
+1	0	1	1	1	1	1	1	1
0	1	0	0	0	0	0	0	0
-1	1	0	0	0	0	0	0	1
-2	1	0	0	0	0	0	1	0
-3	1	0	0	0	0	0	1	1
-4	1	0	0	0	0	1	0	0
-5	1	0	0	0	0	1	0	1
-6	1	0	0	0	0	1	1	0
-7	1	0	0	0	0	1	1	1
-8	1	0	0	0	1	0	0	0
-9	1	0	0	0	1	0	0	1
-10	1	0	0	0	1	0	1	0
-11	1	0	0	0	1	0	1	1
-12	1	0	0	0	1	1	0	0
-13	1	0	0	0	1	1	0	1
-14	1	0	0	0	1	1	1	0
-15	1	0	0	0	1	1	1	1
-16	1	0	0	1	0	0	0	0
-17	1	0	0	1	0	0	0	1
-18	1	0	0	1	0	0	1	0
-19	1	0	0	1	0	0	1	1
-20	1	0	0	1	0	1	0	0
-21	1	0	0	1	0	1	0	1
-22	1	0	0	1	0	1	1	0
-23	1	0	0	1	0	1	1	1
-24	1	0	0	1	1	0	0	0
-25	1	0	0	1	1	0	0	1
-26	1	0	0	1	1	0	1	0
-27	1	0	0	1	1	0	1	1
-28	1	0	0	1	1	1	0	0
-29	1	0	0	1	1	1	0	1
-30	1	0	0	1	1	1	1	0
-31	1	0	0	1	1	1	1	1
-32	1	0	1	0	0	0	0	0
-33	1	0	1	0	0	0	0	1
-34	1	0	1	0	0	0	1	0
-35	1	0	1	0	0	0	1	1
-36	1	0	1	0	0	1	0	0
-37	1	0	1	0	0	1	0	1
-38	1	0	1	0	0	1	1	0
-39	1	0	1	0	0	1	1	1
-40	1	0	1	0	1	0	0	0
-41	1	0	1	0	1	0	0	1
-42	1	0	1	0	1	0	1	0
-43	1	0	1	0	1	0	1	1
-44	1	0	1	0	1	1	0	0
-45	1	0	1	0	1	1	0	1
-46	1	0	1	0	1	1	1	0
-47	1	0	1	0	1	1	1	1
-48	1	0	1	1	0	0	0	0
-49	1	0	1	1	0	0	0	1
-50	1	0	1	1	0	0	1	0
-51	1	0	1	1	0	0	1	1
-52	1	0	1	1	0	1	0	0
-53	1	0	1	1	0	1	0	1
-54	1	0	1	1	0	1	1	0
-55	1	0	1	1	0	1	1	1
-56	1	0	1	1	1	0	0	0
-57	1	0	1	1	1	0	0	1
-58	1	0	1	1	1	0	1	0
-59	1	0	1	1	1	0	1	1
-60	1	0	1	1	1	1	0	0
-61	1	0	1	1	1	1	0	1
-62	1	0	1	1	1	1	1	0
-63	1	0	1	1	1	1	1	1
-64	1	1	0	0	0	0	0	0
-65	1	1	0	0	0	0	0	1
-66	1	1	0	0	0	0	1	0
-67	1	1	0	0	0	0	1	1
-68	1	1	0	0	0	1	0	0
-69	1	1	0	0	0	1	0	1
-70	1	1	0	0	0	1	1	0
-71	1	1	0	0	0	1	1	1
-72	1	1	0	0	1	0	0	0
-73	1	1	0	0	1	0	0	1
-74	1	1	0	0	1	0	1	0
-75	1	1	0	0	1	0	1	1
-76	1	1	0	0	1	1	0	0
-77	1	1	0	0	1	1	0	1
-78	1	1	0	0	1	1	1	0
-79	1	1	0	0	1	1	1	1
-∞	1	1	1	1	1	1	1	1

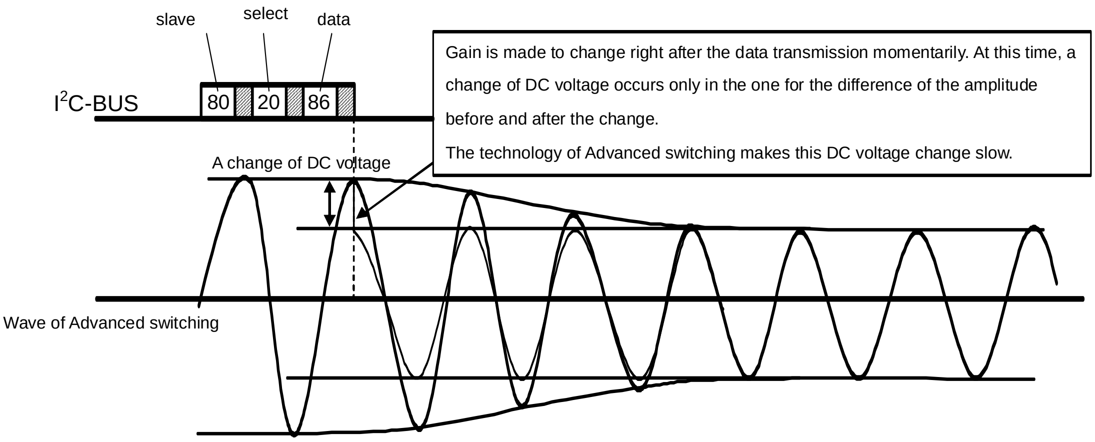
▨ : Initial condition

About Advanced switching circuit

【1】About Advanced switch

1-1. Effect of Advanced switch

It is the ROHM original technology for prevention of switching noise. When gain switching such as volume is done momentarily, a music signal isn't continuous, and unpleasant shock noise is made. Advanced switch can reduce shock noise with the technology which signal wave shape is complemented so that a music signal may not continue drastically.



Gain is made to change right after the data transmission momentarily. At this time, a change of DC voltage occurs only in the one for the difference of the amplitude before and after the change.

The technology of Advanced switching makes this DC voltage change slow.

Advanced switch starts switching after the control data from a microcomputer are received. It takes one fixed time, and wave shape transits as the above figure. The data transmitted by a microcomputer are processed inside, and the most suitable movement is done inside the IC so that switching shock noise may not be made.

But, it presumes by the transmitting timing when it doesn't become intended switching wave shape because it is the function which needs time. The example in which there are relation with the switching time of the data transmitting timing and the reality are shown in the following. It asks for design when it is confirmed well.

1-2. About a kind of transmission method

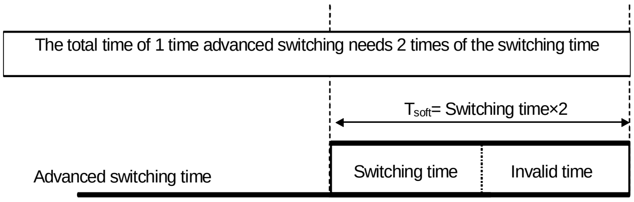
・A data setup except for the item for advanced switch
(p10 select address and the data format, the thing which isn't indicated by gray)
There is no regulation in transmission specially.

・The data setup of the item for advanced switch
（p10 select address and the data format,, the thing which is　indicated by gray）
Though there is no regulation in data transmission, the switching order when data are transmitted to several blocks follows the next 2.

【2】About transmission DATA of advanced switching item

2-1. About switching time of advanced switch

Advanced switching time are equivalent to the switching time and invalid time(effect-less time) inside the IC, and switching time and invalid time is equal to 11.2msec x (1±0.4(dispersion margin))
Therefore, actual Advanced switching time (T_{soft}) is defined as follows.

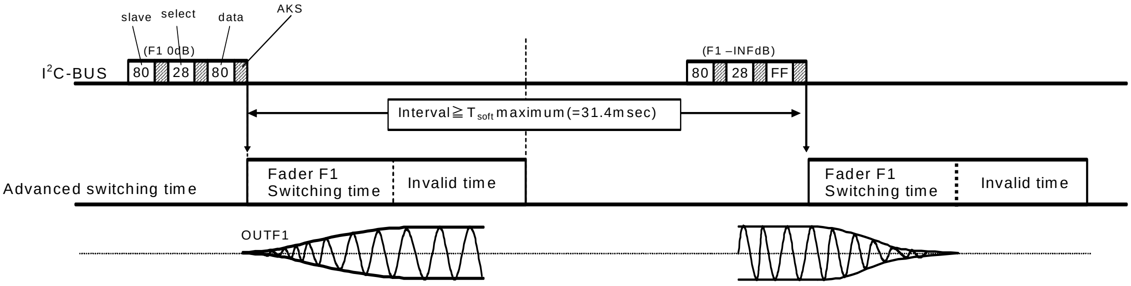


Advanced switching time T_{soft} is, T_{soft} = switching time and invalid time(= switching time x 2).

2-2. About the data transmitting timing in same block state and the switching movement

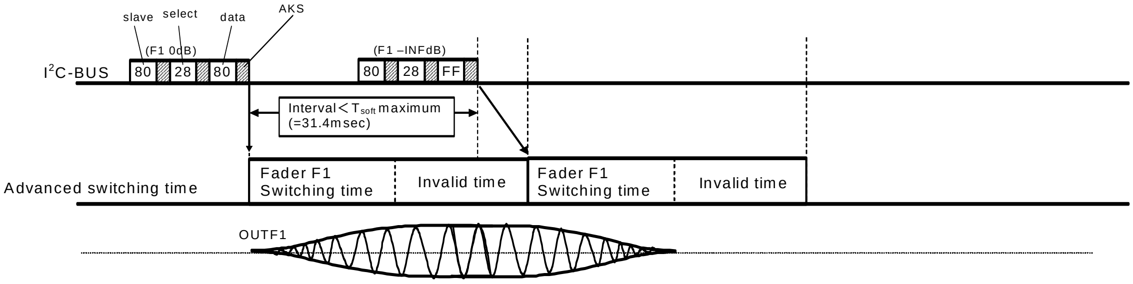
■ Transmitting example 1

A time chart to the start of switching from the data transmission is as following.
At first, the example are shown as below when the interval time is sufficient in which transmission of the same blocks.
(Sufficient interval means time which is more than T_{soft} maximum value, 11.2msec x 1.4(dispersion margin) x 2 = 31.4msec



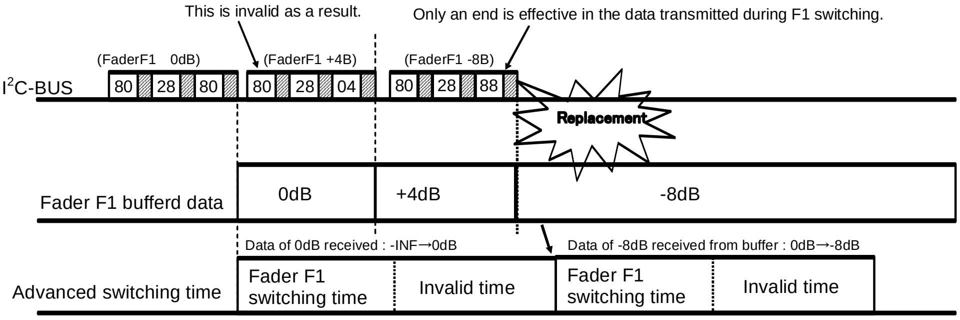
■ Transmitting example 2

Next, when a transmitting interval isn't sufficient (when it is shorter than the above interval), the example is shown. In case data are transmitted during the first switching movement, the next switching movement is started in succession after the first switching movement is finished.



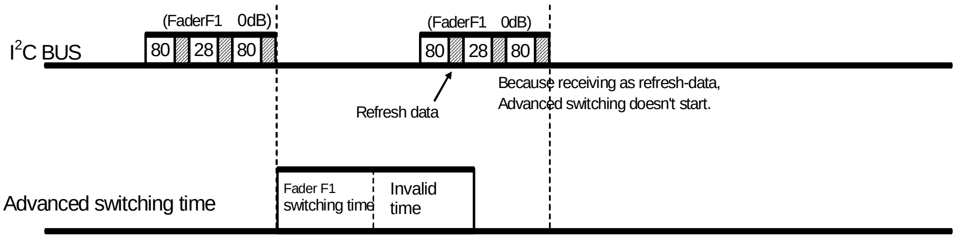
■ Transmitting example 3

Next, the example of the switching movement when a transmitting interval was shortened more is shown.
Inside the IC, It has the buffer which memorizes data, and a buffer always does transmitting data.
But, data of +4dB which transmitted to the second become invalid with this example because the buffer holds only the latest data.



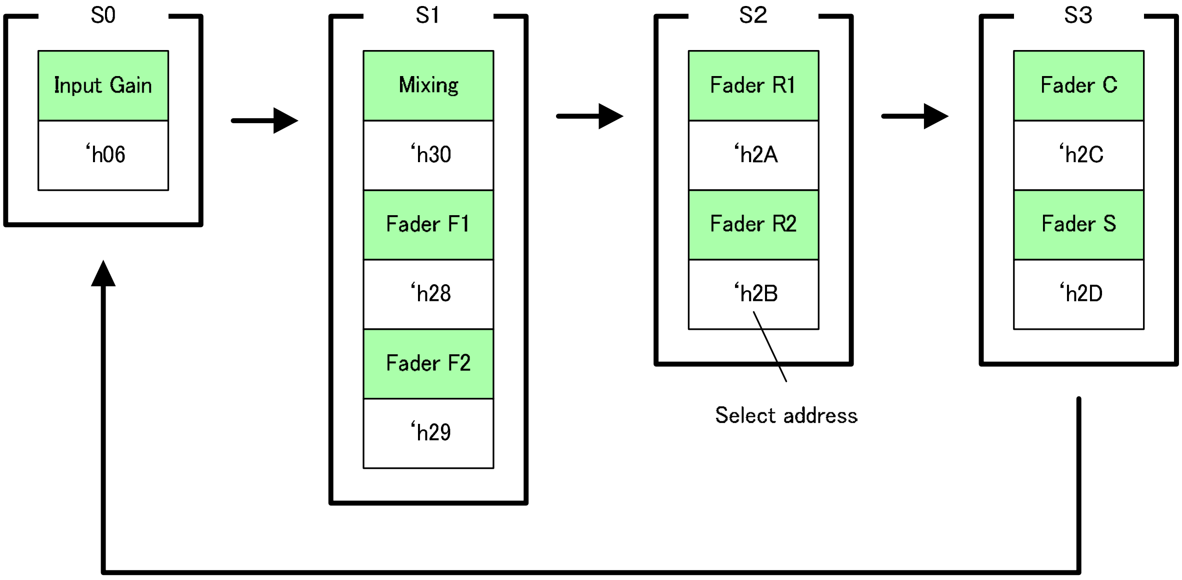
■ Transmitting example 4

At first, transmitting data are stored in the maintenance data, and next it is written in the setup data in which gain is set up to. But, in case there is no difference between the transmitting data and the setup data as a refresh data, Advanced switch movement isn't started.



2-3. About the data transmitting timing and the switching movement in several block state

When data are transmitted to several blocks, treatment in the BS (block state) unit is carried out inside the IC. The order of advanced switch movement start is decided in advance dependent on BS.



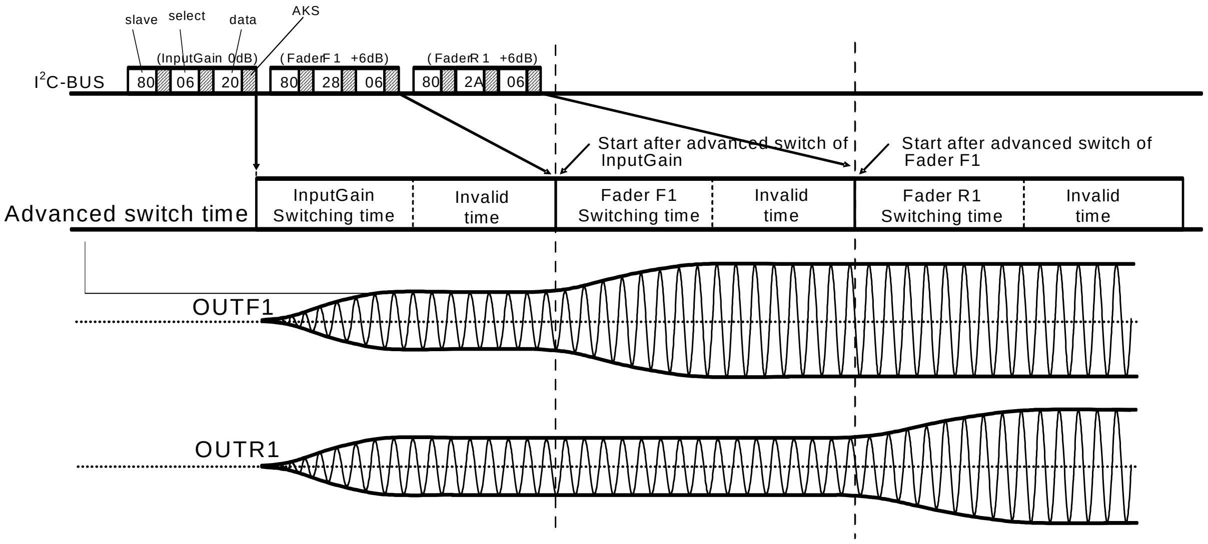
The order of advanced switch start
※It is possible that blocks in the same BS start switching at the same timing.

■ Transmitting example 5

About the transmission to several blocks also, as explained in the previous section, though there is no restriction of the I^{2}C-BUS data transmitting timing, the start timing of switching follows the figure of previous page, The order of advanced switch start.

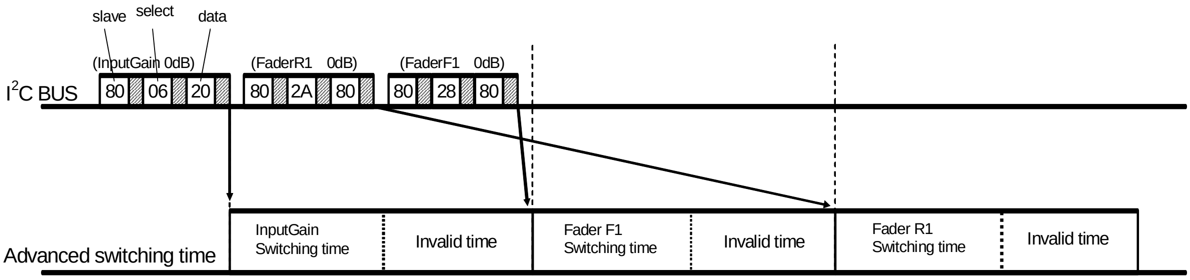
Therefore, it isn't based on the data transmitting order, and an actual switching order becomes as the figure of previous page, The order of advanced switch start.(Transmitting example 6).

Each block data is being transmitted separately in the transmitting example 5, but it becomes the same result even if data are transmitted by automatic increment.



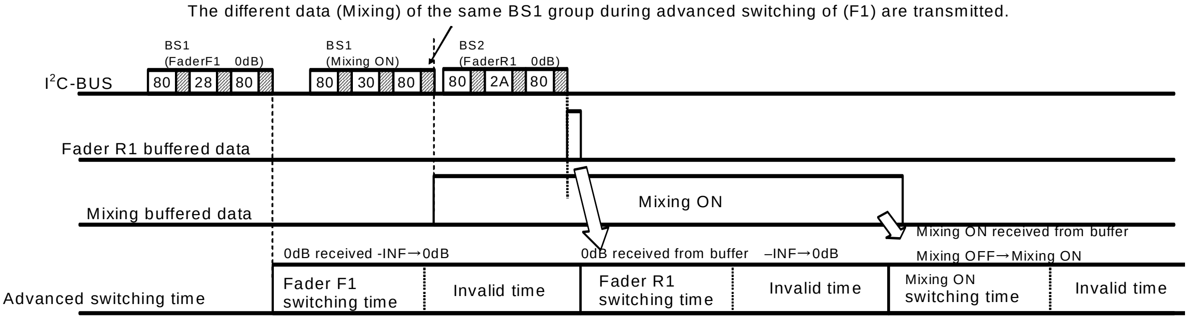
■ Transmitting example 6

When an actual switching order is different from the transmitting order or data except for the same BS are transmitted at the timing when advanced switch movement isn't finished, switching of the next BS is done after the present switching completion .



■ Transmitting example 7

In this example, data of BS1 and BS2 are transmitted during Advances switching of BS1(same BS1 group) .



【3】Advanced switch transmitting timing list

3-1. InputGain/Fader(F1,F2,R1,R2, S,C)/ Mixing

	Advanced switch stand by	Advanced switch active
Transmission timing	optional	optional
Start timing	Starts right after the data transmission	Starts right after present switching was finished.
Advanced switching time	T_{soft}※1	T_{soft}

※1　Advanced switching time T_{soft} equalls to 2times of swithcing time.

Application Circuit Diagram

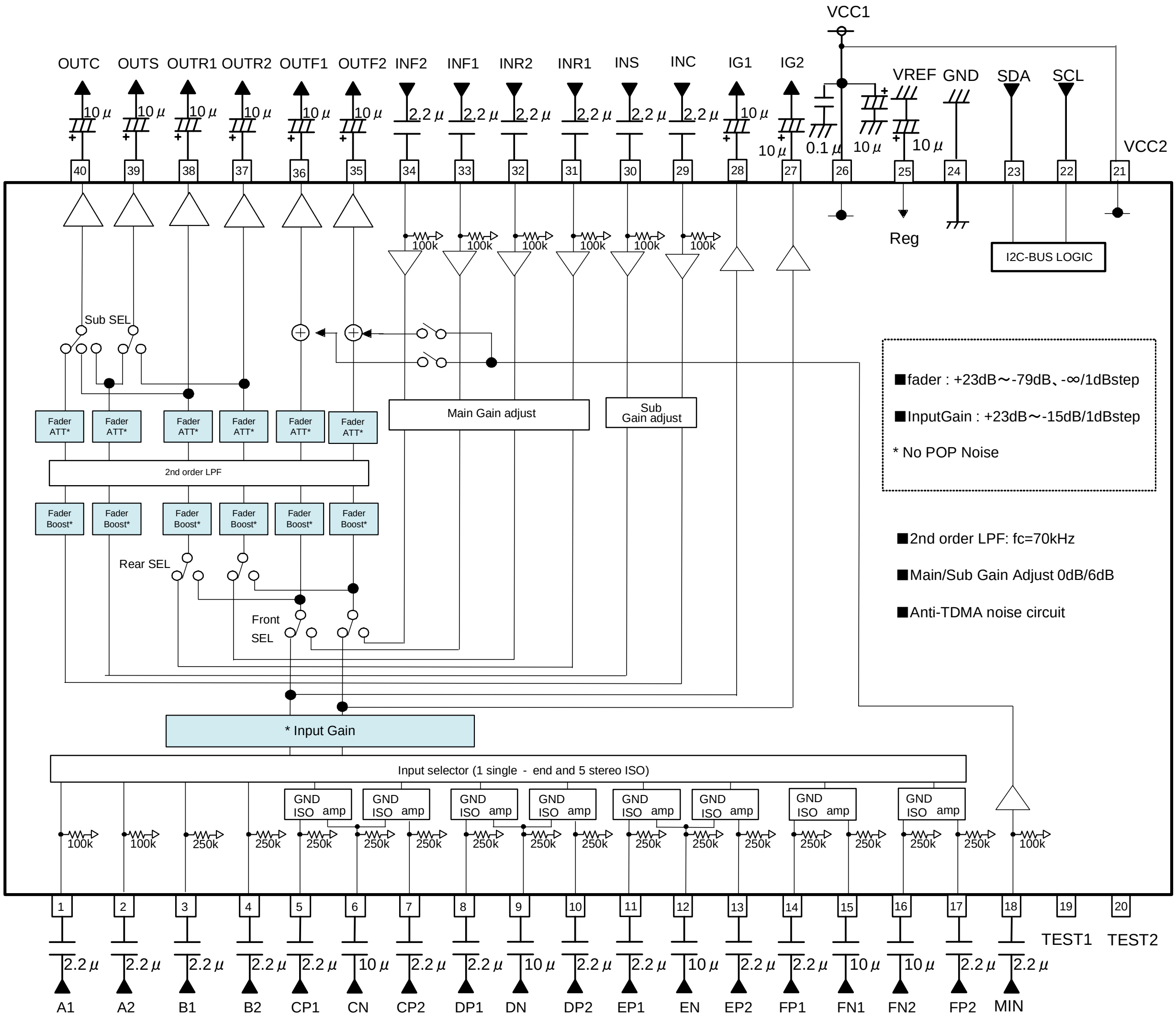


Figure 16. Application Circuit Diagram

UNIT
RESISTANCE: Ω
CAPACITANCE: F

Notes on wiring

①Please connect the decoupling capacitor of a power supply in the shortest distance as much as possible to GND.
②Lines of GND shall be one-point connected.
③Wiring pattern of Digital shall be away from that of analog unit and cross-talk shall not be acceptable.
④Lines of SCL and SDA of I^{2}C-BUS shall not be parallel if possible. The lines shall be shielded, if they are adjacent to each other.
⑤Lines of analog input shall not be parallel if possible. The lines shall be shielded, if they are adjacent to each other.
⑥About TEST1,2 terminal(19,20pin), please use with OPEN.

Thermal Derating Curve

About the thermal design by the IC
Characteristics of an IC have a great deal to do with the temperature at which it is used, and exceeding absolute maximum ratings may degrade and destroy elements. Careful consideration must be given to the heat of the IC from the two standpoints of immediate damage and long-term reliability of operation.

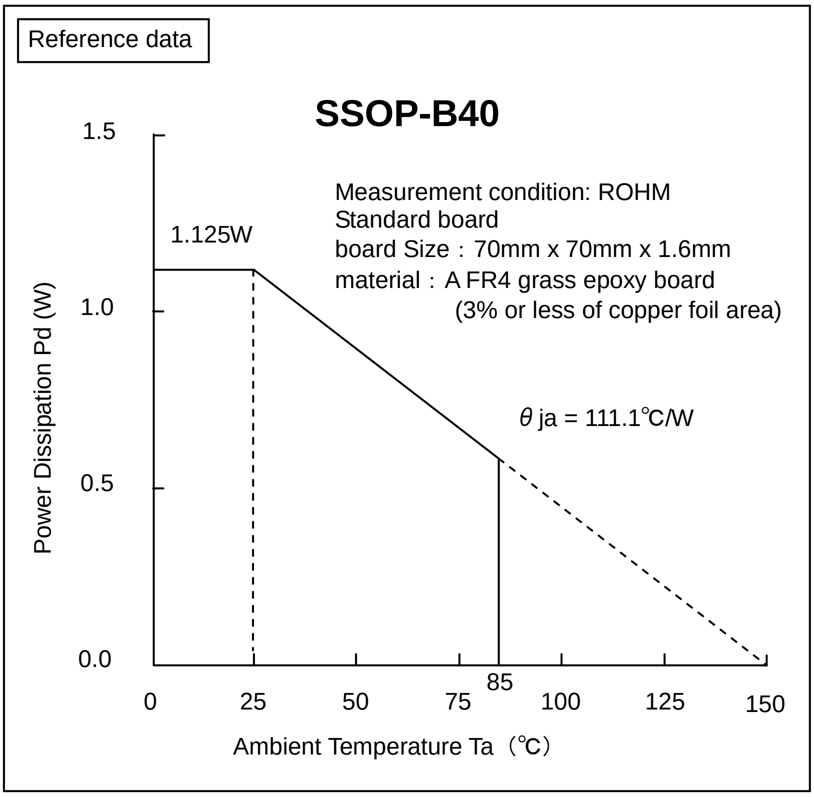
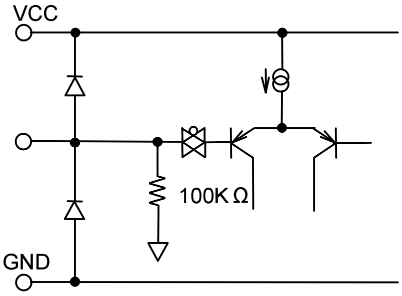
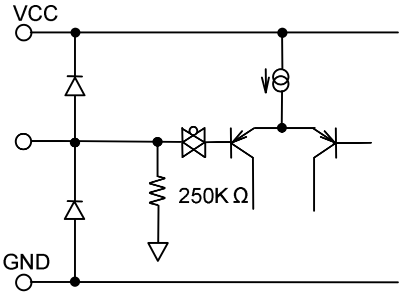
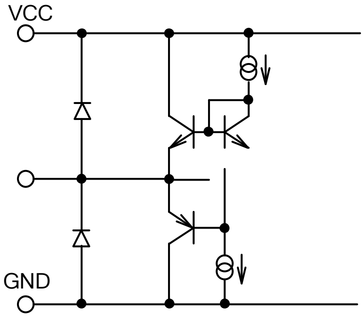
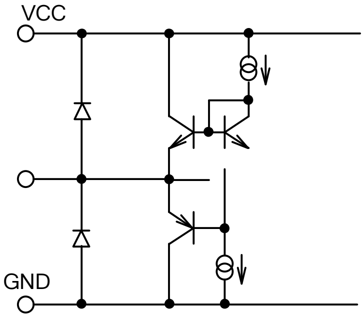


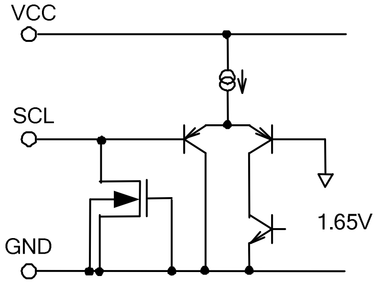
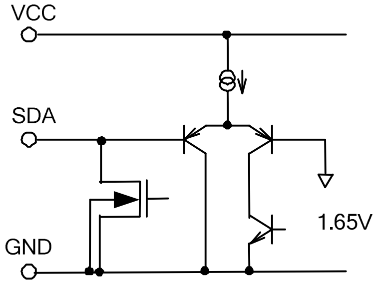
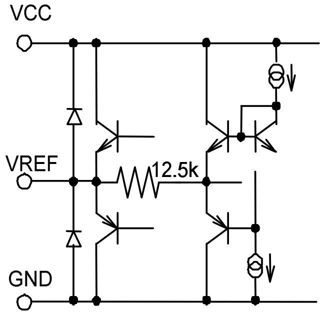
Figure 17. Temperature Derating Curve

Note) Values are actual measurements and are not guaranteed.
Note) Power dissipation values vary according to the board on which the IC is mounted.

Terminal Equivalent Circuit and Description

Terminal No	Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
1 2 29 30 31 32 33 34 18	A1 A2 INC INS INR1 INR2 INF1 INF2 MIN	4.15V		A terminal for signal input. The input impedance is 100kΩ(typ). .
3 4 5 6 7 8 9 10 11 12 13 14 15 16 17	B1 B2 CP1 CN CP2 DP1 DN DP2 EP1 EN EP2 FP1 FN1 FN2 FP2	4.15V		Input terminal available to Single/Differential mode. The input impedance is 250kΩ(typ).
27 28	IG2 IG1	4.15V		Input gain output terminal
35 36 37 38 39 40	OUTF2 OUTF1 OUTR2 OUTR1 OUTS OUTC	4.15V		Fader output terminal

The figures in the pin explanation and input/output equivalent circuit is reference value, it doesn’t guarantee the value.

Terminal No	Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
21,26	VCC (VCC1,2)	8.5V		Power supply terminal.
22	SCL	―		A terminal for clock input of I^2C-BUS communication.
23	SDA	―		A terminal for data input of I^2C-BUS communication.
24	GND	0		Ground terminal.
25	VREF	4.15V		BIAS terminal. Voltage for reference bias of analog signal system. The simple precharge circuit and simple discharge circuit for an external capacitor are built in.

The figures in the pin explanation and input/output equivalent circuit is reference value, it doesn’t guarantee the value.

Note on use

1. Absolute maximum rating voltage

When voltage is impressed to VCC exceeding absolute-maximum-rating voltage, circuit current increase rapidly, and it may result in property degradation and destruction of a device.

When impressed by a VCC terminal (21,26pin) especially by serge examination etc., even if it includes an of operation voltage +serge pulse component, be careful not to impress voltage (about 14V) greatly more than absolute-maximum-rating voltage.

2. About a signal input part

About constant set up of input coupling capacitor

In the signal input terminal, the constant setting of input coupling capacitor C(F) be sufficient input impedance R_{IN}(Ω) inside IC and please decide. The first HPF characteristic of RC is composed.

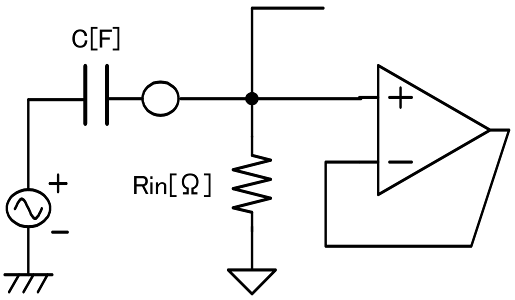
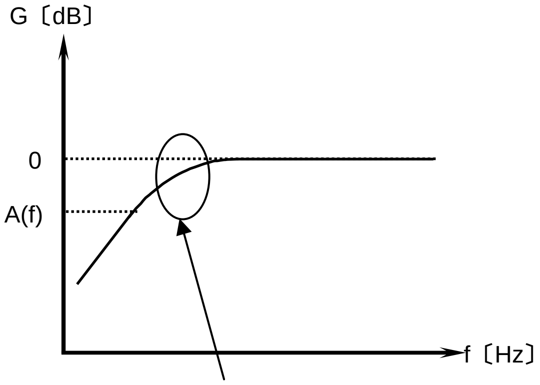


Figure 18. Input Equivalent Circuit



$$A(f) = \sqrt{\frac{(2\pi fCR_{IN})^2}{1+(2\pi fCR_{IN})^2}}$$

3. About output load characteristics

The usages of load for output are below (reference). Please use the load more than 10 kΩ(TYP).

Output terminal

Terminal No.	Terminal Name	Terminal No.	Terminal Name	Terminal No.	Terminal Name	Terminal No.	Terminal Name
28	IG1	36	OUTF1	38	OUTR1	40	OUTC
27	IG2	35	OUTF2	37	OUTR2	39	OUTS

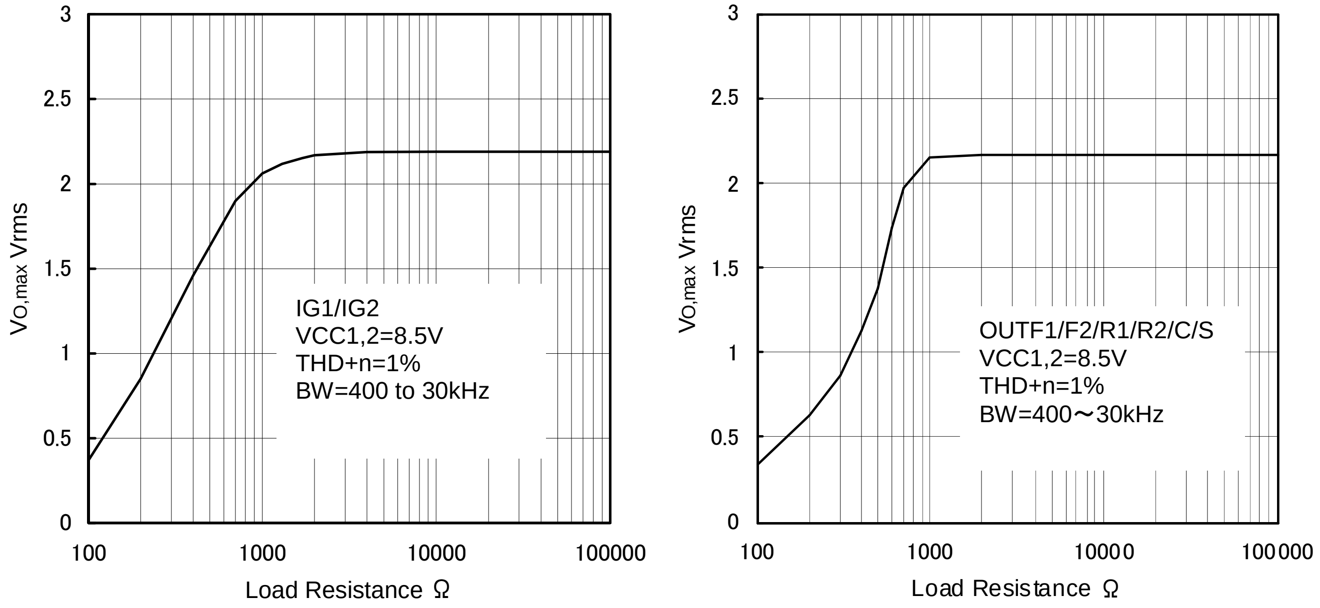


Figure 19. Output load characteristic at VCC1,2=8.5V (Reference)

4.About TEST1,2 terminal(19,20pin)

About TEST1,2 terminal(19,20pin), please use with OPEN.

5. About signal input terminals

Because the inner impedance of the terminal becomes 100 kΩ or 250 kΩ when the signal input terminal makes a terminal open, the plunge noise from outside sometimes becomes a problem.
When there is a signal input terminal not to use, design so as not to ground.

6. About changing gain of Input Gain and Fader Volume

In case of the boost of the input gain and fader volume when changing to the high gain which exceeds 20 dB especially, the switching shock noise sometimes becomes big.
In this case, we recommend changing every 1 dB step without changing a gain at once.
Also, the shock noise sometimes can reduce by making advanced switch time long, too.

Ordering Name Selection

B D 3 7 0 6 7 F V **ME 2**

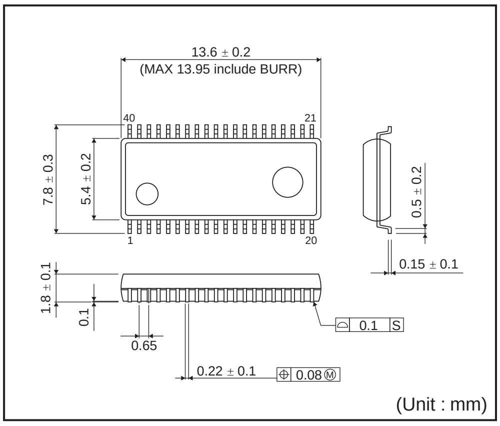
Part Number

Package
FV: SSOP-B40

Tape and Reel Information
E2: Reel type embossed taping
(SSOP-B40)

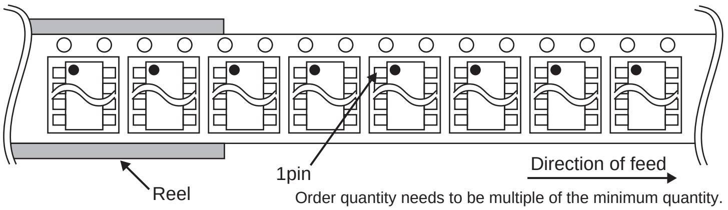
Physical Dimension Tape and Reel Information

SSOP-B40



<Tape and Reel information>

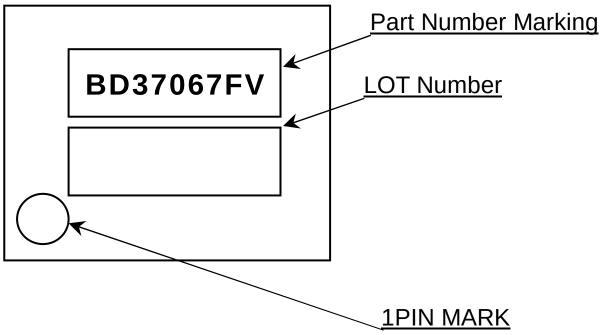
Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



Order quantity needs to be multiple of the minimum quantity.

Marking Diagram

SSOP-B40(TOP VIEW)



Revision History

Date	Revision	Changes
13.MAR.2014	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   - [a] Installation of protection circuits or other protective devices to improve system safety
   - [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   - [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   - [f] Sealing or coating our Products with resin or other coating materials
   - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   - [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM’s internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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