

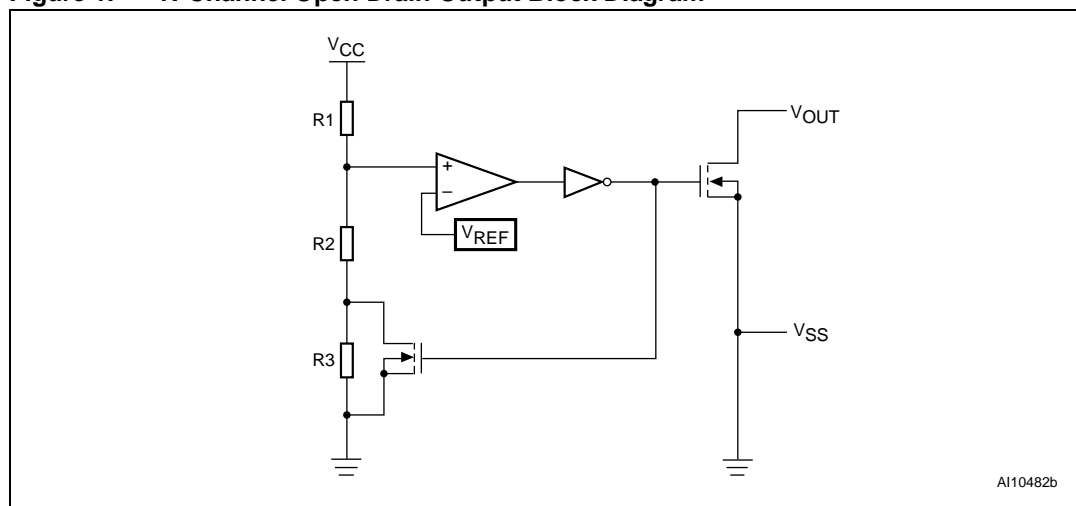
Using STMicroelectronics Voltage Detectors

1 Introduction

Voltage detectors are designed to monitor the system supply voltage and assert the output signal, \overline{OUT} , every time it goes below a defined voltage threshold.

The major advantages of these circuits are low current consumption and a precise temperature-compensated voltage reference, V_{REF} (see [Figure 1](#)). STMicroelectronics voltage detectors are also laser programmed to the desired voltage threshold over the range of 1.6V to 6.0V in 100mV steps and they have a good transient immunity (see [Figure 5](#)).

Figure 1. N-Channel Open Drain Output Block Diagram



Note that voltage detector output state simply indicates if the supply voltage is above or below a specific threshold, which can be used for early power fail warning. However microprocessors' inputs require some minimum input pulse width to register the change of signal on the logical input. In this case we recommend using reset circuits, which guarantee the minimum pulse width known as reset time-out period. Reset circuits have some other advantages compared to voltage detectors (e.g. specification across temperature, better voltage threshold accuracy, and lower temperature coefficient). On the other hand voltage detectors are usually able to operate at higher voltages, have lower current consumption, greater hysteresis and usually a lower price.

The qualities mentioned above cause voltage detectors to be preferentially used in the following applications:

- Battery Monitoring
- Power-Failure Monitoring
- Portable Medical Devices
- Power Fail Detection
- PDAs
- Notebook Computers
- Back-up Supply Switching
- Portable/Battery-Powered Electronics
- Cell Phones.

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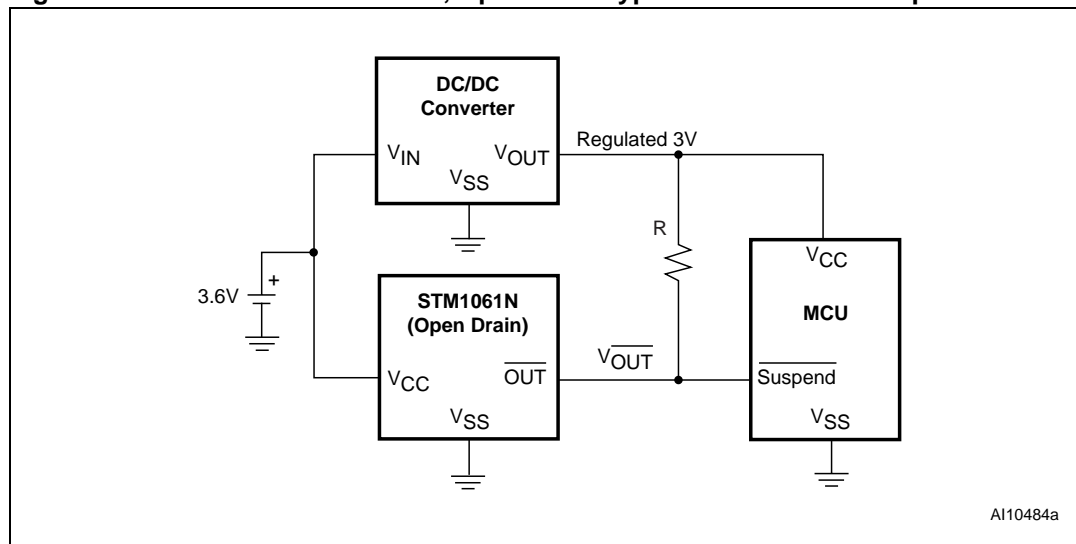
2 Description

STMicroelectronics offers e.g. the STM1061 voltage detector. One of its typical uses is shown in the [Figure 2](#).

The STM1061N open drain output voltage detector is monitoring the 3.6V battery. This allows the voltage detector to detect a voltage drop early, assert the output signal ($\overline{\text{OUT}}$) so the MCU can start safeguard routines even before the regulated supply voltage for the MCU starts to fall.

The voltage detector open drain output sinks current when the output is asserted. It is necessary to connect a pull-up resistor from $\overline{\text{OUT}}$ to any supply voltage (see [Figure 2](#)). The resistor value must be large enough to register a logic low and small enough to register a logic high while all of the input current and leakage paths connected to the reset output line are being supplied. A 10k Ω pull-up is sufficient in most applications.

Figure 2. STM1061N Active-Low, Open Drain typical Hardware Hookup

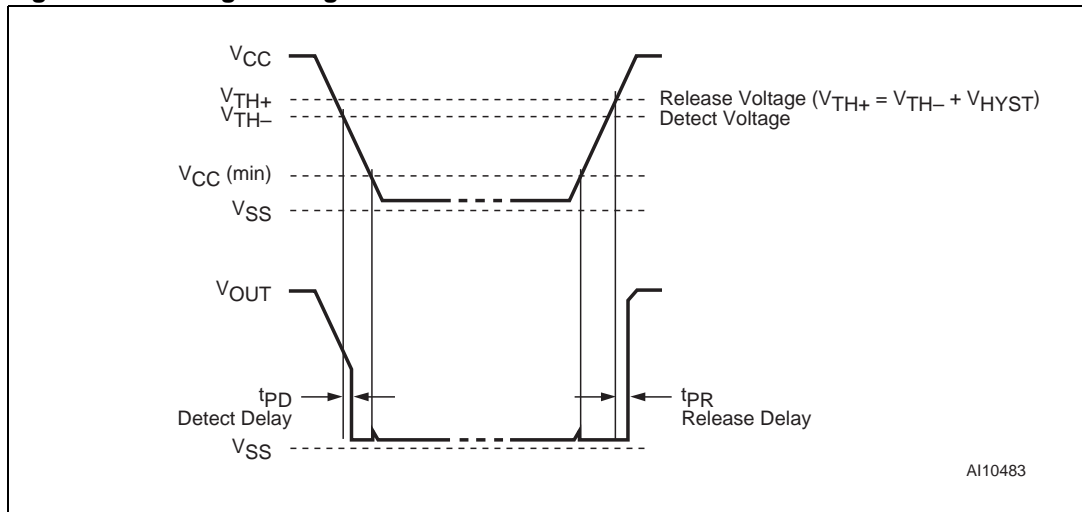


3 Operation

The voltage detector monitors V_{CC} voltage input continuously (see [Figure 1](#)) and compares it with the precision voltage reference, V_{REF} . When V_{CC} falls below a specified trip point threshold, the output (\overline{OUT}) is forced low and remains asserted as long as the V_{CC} input remains below V_{TH+} , where $V_{TH+} = V_{TH-} + V_{HYST}$ (hysteresis) see [Figure 3](#).

Remember that a pull-up resistor on the voltage detector open-drain output is required for proper functionality (see [Figure 2](#)).

Figure 3. Voltage timing waveform



4 Transient Immunity

The STM1061 device is relatively immune to negative-going V_{CC} transients (glitches). The graph (see [Figure 4](#)) indicates the maximum pulse width a negative V_{CC} transient can have without asserting output signal, \overline{OUT} . As the magnitude of the transient increases (further below the threshold), the maximum allowable pulse width decreases. Any combination of duration and overdrive which lies under the curve will NOT assert the output signal, \overline{OUT} .

A $0.1\mu\text{F}$ bypass capacitor, C_b , mounted as close as possible to the V_{CC} pin provides additional transient immunity (see [Figure 5](#)).

Figure 4. Maximum Transient Duration vs. Reset Threshold Overdrive

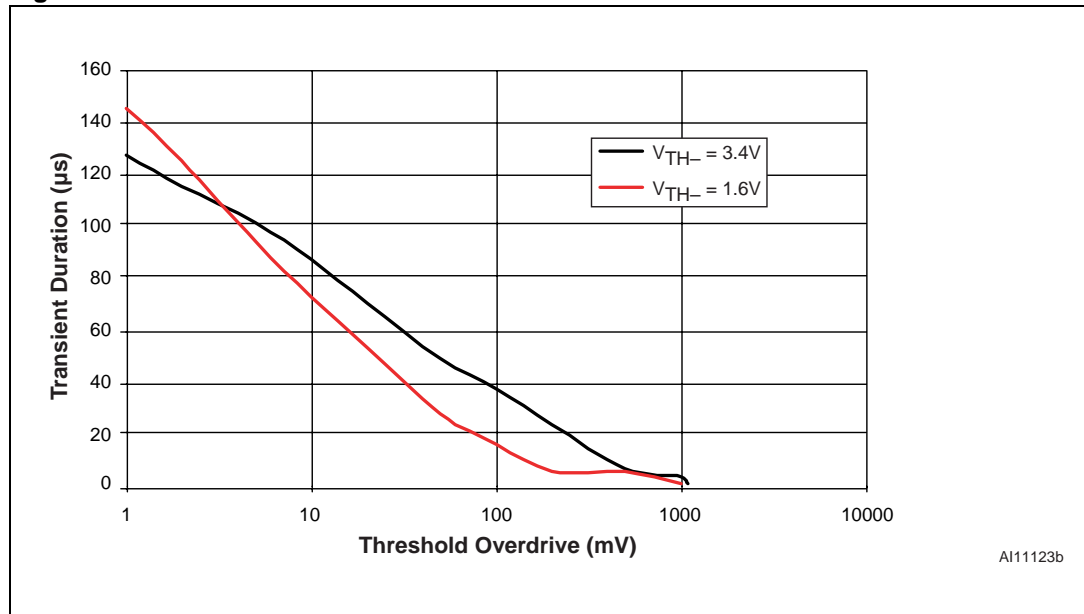
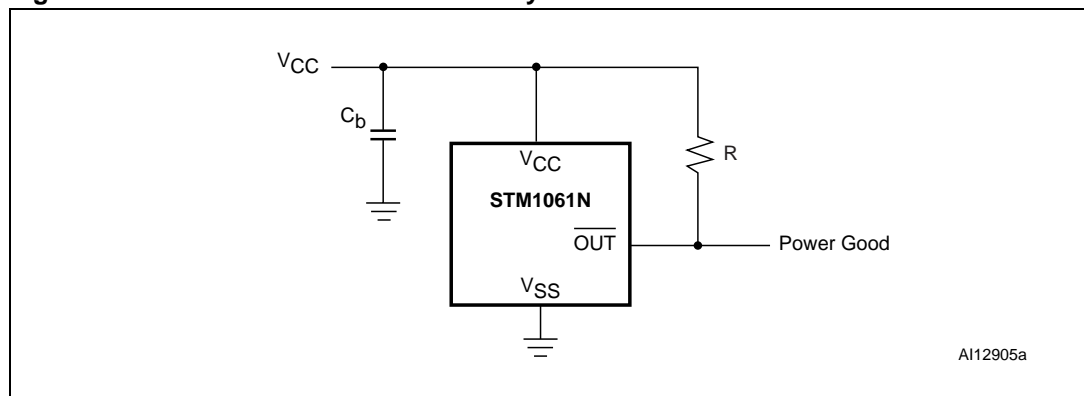


Figure 5. Additional Transient Immunity

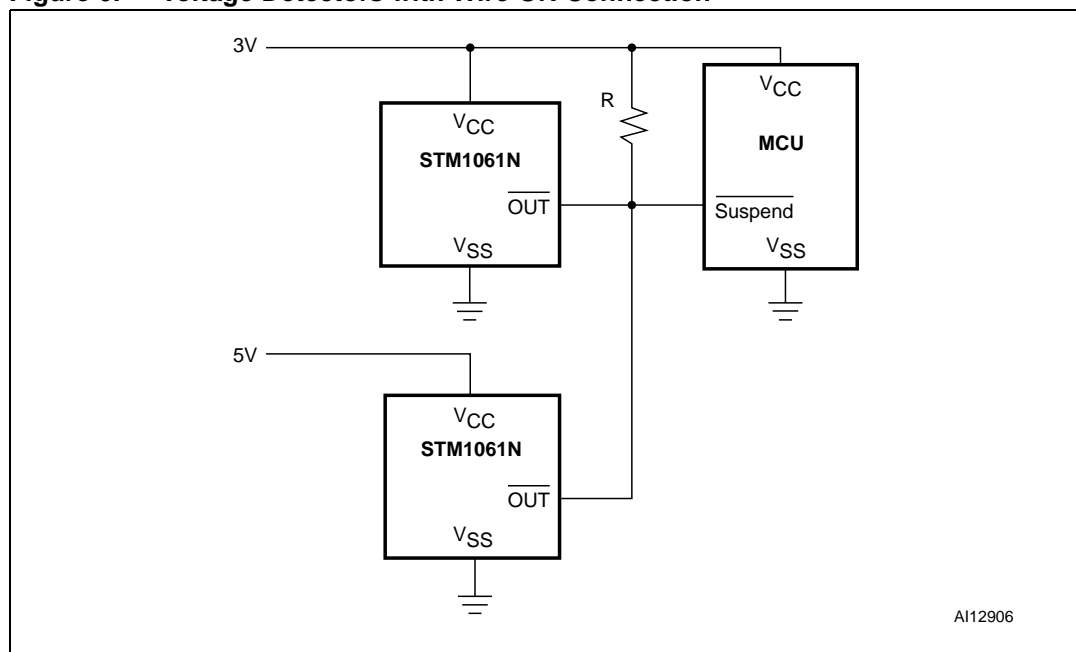


5 Open Drain Output Advantages

The advantages of open drain output are the ability to connect more open drain outputs in parallel (wired OR connections, see [Figure 6](#)) as well as connect the output to a power supply voltage different from V_{CC} (see [Figure 7](#)).

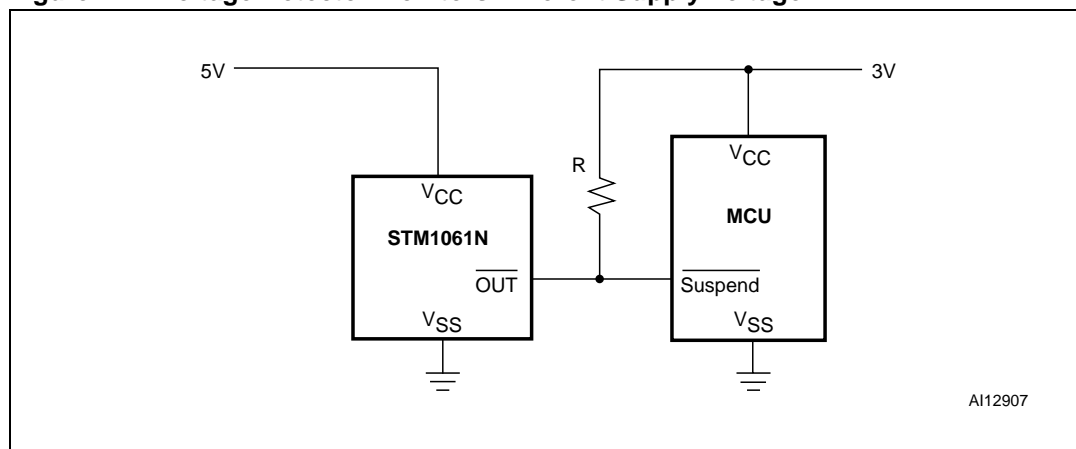
The hook up on [Figure 6](#) monitors 2 independent supply voltages (3V and 5V). Every time either the first OR the second supply voltage goes below defined threshold, the input signal of the MCU, $\overline{\text{Suspend}}$, goes low.

Figure 6. Voltage Detectors with Wire OR Connection



A voltage detector with an open drain output can also monitor supply voltages different from the MCU supply voltage (see [Figure 7](#)). The logic high on the MCU $\overline{\text{Suspend}}$ input is adequate to supply voltage of the MCU.

Figure 7. Voltage Detector Monitors Different Supply Voltage

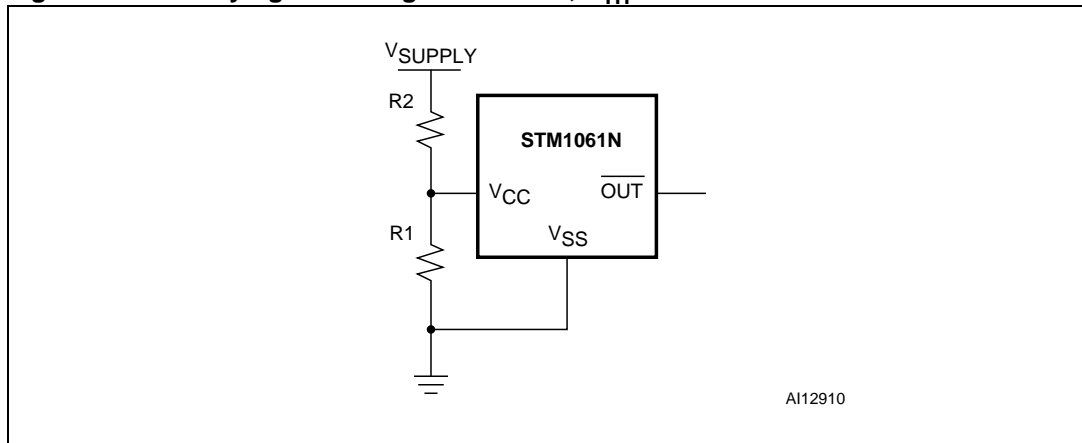


6 Modifying the Voltage Threshold, V_{TH-}

Although the STM1061 voltage thresholds, V_{TH-} , are adjusted in fine steps (100mV), it is sometimes necessary to make adjustments during prototyping. This can be achieved by connecting of external divider (see [Figure 8](#)). This hook up can be used if the required threshold of voltage detector is lower than the desired monitored voltage.

To maintain detector accuracy, the current flow through the divider should be significantly higher than the 0.9µA operating current required by the STM1061. A 90µA bleeder current is sufficient in most applications.

Figure 8. Modifying the Voltage Threshold, V_{TH-}



Example:

Threshold of STM1061 detector: $V_{TH-} = 1.6V$
 Desired threshold: $V_{SUPPLY} = 1.8V$
 Recommended bleeder current: $I = 90\mu A$

$R1+R2$ is then: $(R1+R2) = V_{SUPPLY}/I = 1.8V/90\mu A = 20k\Omega$

The voltage on the divider is:

$$V_{CC} = \frac{R_1}{R_1 + R_2} V_{SUPPLY} = V_{TH-}$$

That is why:

$$R_1 = \frac{V_{TH-}}{V_{SUPPLY}} (R_1 + R_2) = \frac{1.6V}{1.8V} 20k\Omega = 17.7k\Omega$$

The value of $R2$ resistor is then:

$$R_2 = 20k\Omega - 17.7k\Omega = 2.2k\Omega$$

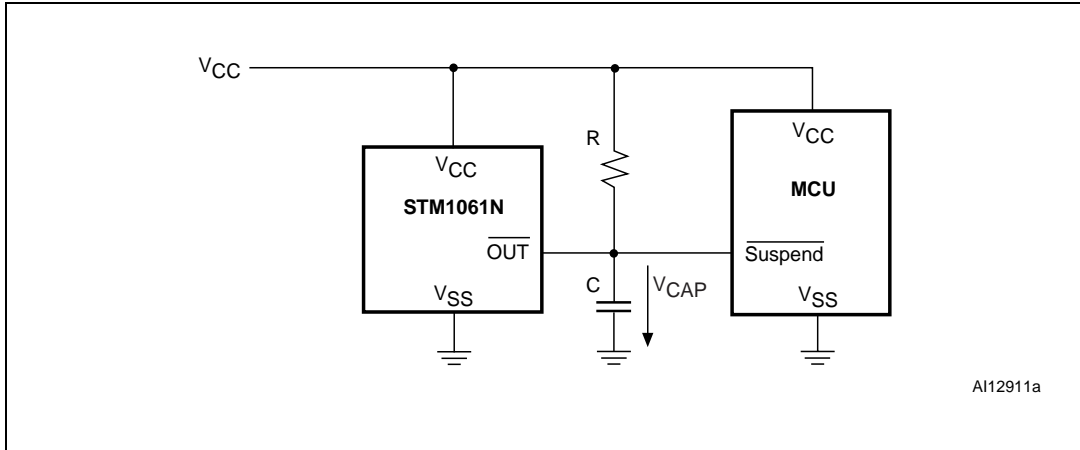
We will choose the nearest values of the resistors (e.g. from E24):

$R1 = 18k\Omega$, $R2 = 2.2k\Omega$

7 Simulation of the Reset Time-out Period

It is possible to simulate reset time-out period with an RC element on the output of voltage detector (see [Figure 9](#)).

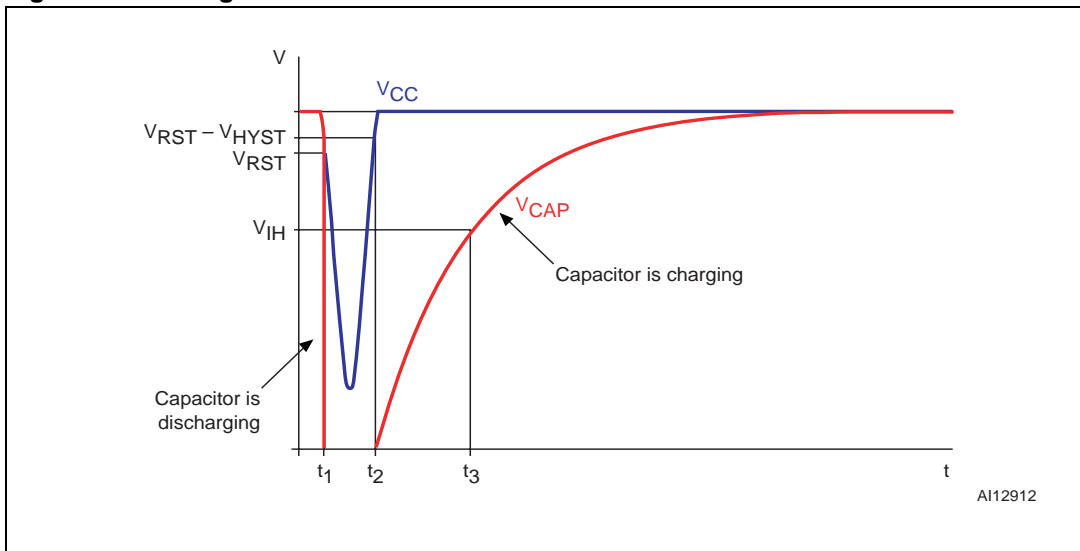
Figure 9. Hardware Hookup with RC element on the Voltage Detector Output



If the supply voltage, V_{CC} , drops below the defined voltage threshold, V_{RST} , the capacitor, C, is discharged through the output transistor of the voltage detector (see [Figure 10](#)).

When the supply voltage, V_{CC} , rises above the voltage threshold plus hysteresis, $V_{\text{RST}} + V_{\text{HYST}}$, the output transistor disconnects the output from the ground and the capacitor, C, is charged through the resistor, R.

Figure 10. Voltage Waveforms



The voltage on the STM1061N output resp. capacitor, V_{CAP} rises as capacitor is charged. When it reaches input high voltage trip point of the MCU (time t_3), the high state is detected. If there is no RC element on the output, the \overline{OUT} pin goes high at the time t_2 . That is why simulated reset time-out period is t_3-t_2 .

Use following formula for determining the correct capacitor value:

$$C = \frac{t}{R \cdot \ln \frac{V_{CC}}{V_{CC} - V_{IH}}}$$

where,

C = Capacitor of RC element in Farads,

R = resistor of RC element in Ohms,

t = desired time-out period (t_3-t_2) in seconds,

V_{CC} = supply voltage,

V_{IH} = input voltage trip point for the MCU

\ln = natural logarithm.

Example:

The STM1061N27WX6F is used to monitor a 3V supply voltage. The MCU detects input high state at $V_{IH} = 0.7 \cdot V_{CC} = 0.7 \cdot 3V = 2.1V$. Desired time-out period is 140ms. An $R = 100\Omega$ resistor is chosen.

The value of the capacitor is following:

$$C = \frac{t}{R \cdot \ln \frac{V_{CC}}{V_{CC} - V_{IH}}} = \frac{140 \cdot 10^{-3}}{100 \cdot 10^3 \cdot \ln \frac{3}{3 - 2.1}} = 1.16 \cdot 10^{-6} = 1.16\mu F$$

The closest higher capacitance value from the most common E12 series (i.e. $C = 1.2\mu F$) is chosen. The time-out delay will be slightly greater by choosing a higher value of capacitor.

Remember that this circuitry should be used only for temporary purposes. In the case of real need of time-out delay the usage of reset device is highly recommended as mentioned in the [Introduction](#).

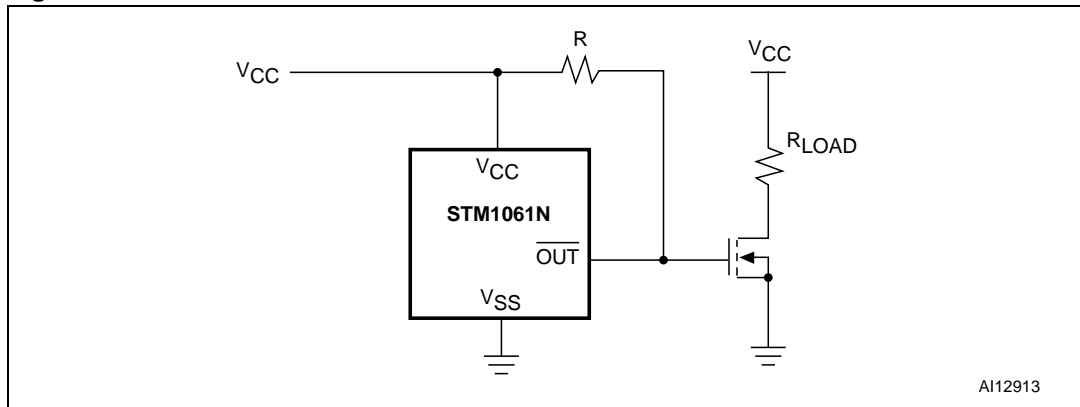
8 Output MOSFET protection

For applications requiring higher current drive capabilities an external MOSFET might be used, which protect the output of a voltage detector from overloading and destroying. It is possible to use either N channel or P channel transistor (see below).

8.1 External N-channel transistor

If the load should be connected to the supply voltage during the regular operation (output, $\overline{\text{OUT}}$, is not asserted), an external N-channel transistor will be needed (see [Figure 11](#)). When the supply voltage V_{CC} drops below the threshold of the voltage detector, the output signal, $\overline{\text{OUT}}$, is asserted, the external N-channel MOSFET is switched off and disconnects the load from the ground.

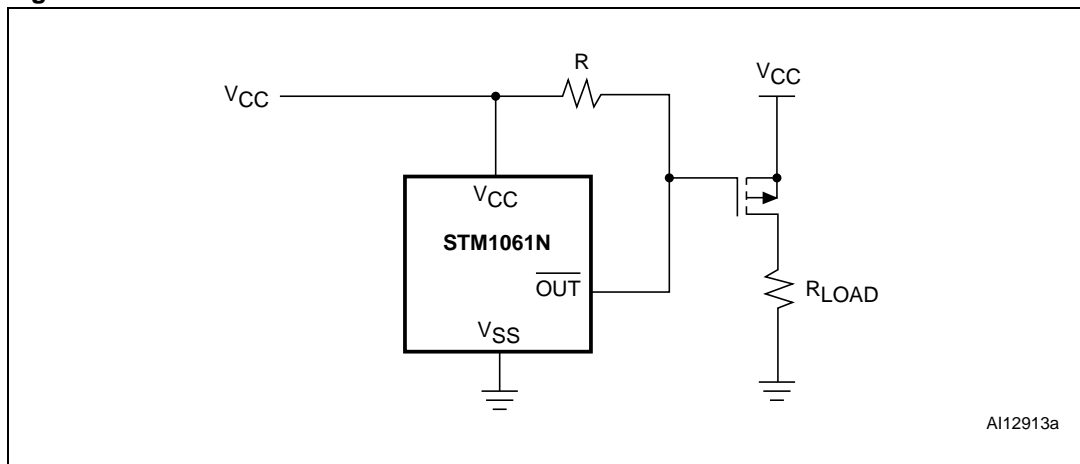
Figure 11. Circuit with external N-channel transistor



8.2 External P-channel transistor

If the load should be connected to the supply voltage during the output, $\overline{\text{OUT}}$, assertion, an external P-channel transistor will be needed (see [Figure 12](#)). When the supply voltage V_{CC} drops below the threshold of the voltage detector, the output signal, $\overline{\text{OUT}}$, is asserted, the external P-channel MOSFET is switched on and connects the load to the supply voltage, V_{CC} .

Figure 12. Circuit with external P-channel transistor



9 Revision history

Table 1. Document revision history

Date	Revision	Changes
06-Feb-2007	1	Initial release.

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