

NTMD2P01R2

Power MOSFET -2.3 Amps, -16 Volts Dual SO-8 Package

Features

- High Efficiency Components in a Single SO-8 Package
- High Density Power MOSFET with Low $R_{DS(on)}$
- Logic Level Gate Drive
- SO-8 Surface Mount Package,
Mounting Information for SO-8 Package Provided

Applications

- Power Management in Portable and Battery-Powered Products, i.e.:
Computers, Printers, PCMCIA Cards, Cellular and Cordless Telephones

MOSFET MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	-16	V
Gate-to-Source Voltage – Continuous	V_{GS}	± 10	V
Thermal Resistance – Junction-to-Ambient (Note 1)	$R_{\theta JA}$	175	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	0.71	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	I_D	-2.3	A
Continuous Drain Current @ $T_A = 100^\circ\text{C}$	I_D	-1.45	A
Pulsed Drain Current (Note 4)	I_{DM}	-9.0	A
Thermal Resistance – Junction-to-Ambient (Note 2)	$R_{\theta JA}$	105	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.19	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	I_D	-2.97	A
Continuous Drain Current @ $T_A = 100^\circ\text{C}$	I_D	-1.88	A
Pulsed Drain Current (Note 4)	I_{DM}	-12	A
Thermal Resistance – Junction-to-Ambient (Note 3)	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	2.0	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	I_D	-3.85	A
Continuous Drain Current @ $T_A = 100^\circ\text{C}$	I_D	-2.43	A
Pulsed Drain Current (Note 4)	I_{DM}	-15	A
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = -16$ Vdc, $V_{GS} = -4.5$ Vdc, Peak I_L $= -5.0$ Apk, $L = 28$ mH, $R_G = 25$ Ω)	E_{AS}	350	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

1. Minimum FR-4 or G-10 PCB, Steady State.
2. Mounted onto a 2" square FR-4 Board (1" sq. 2 oz Cu 0.06" thick single sided), Steady State.
3. Mounted onto a 2" square FR-4 Board (1" sq. 2 oz Cu 0.06" thick single sided), $t \leq 10$ seconds.
4. Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

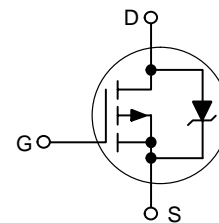


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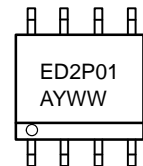
V_{DSS}	$R_{DS(on)}$ TYP	I_D MAX
-16 V	100 m Ω @ -4.5 V	-2.3 A

P-Channel



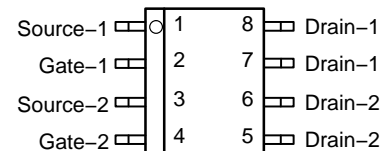
SO-8
CASE 751
STYLE 11

MARKING DIAGRAM



ED2P01 = Device Code
A = Assembly Location
Y = Year
WW = Work Week

PIN ASSIGNMENT



Top View

ORDERING INFORMATION

Device	Package	Shipping†
NTMD2P01R2	SO-8	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 5)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = -250 μAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	-16 -	- -12.7	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = -16 Vdc, V _{GS} = 0 Vdc, T _J = 25°C) (V _{DS} = -16 Vdc, V _{GS} = 0 Vdc, T _J = 125°C)	I _{DSS}	- -	- -	-1.0 -10	μAdc
Gate-Body Leakage Current (V _{GS} = -10 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	-	-	-100	nAdc
Gate-Body Leakage Current (V _{GS} = +10 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	-	-	100	nAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = -250 μAdc) Temperature Coefficient (Negative)	V _{GS(th)}	-0.5 -	-0.90 2.5	-1.5 -	Vdc mV/°C
Static Drain-to-Source On-State Resistance (V _{GS} = -4.5 Vdc, I _D = -2.4 Adc) (V _{GS} = -2.7 Vdc, I _D = -1.2 Adc) (V _{GS} = -2.5 Vdc, I _D = -1.2 Adc)	R _{DS(on)}	-	0.070 0.100 0.110	0.100 0.130 0.150	Ω
Forward Transconductance (V _{DS} = -10 Vdc, I _D = -1.2 Adc)	g _{FS}	-	4.2	-	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = -16 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	-	540	750	pF
Output Capacitance		C _{oss}	-	215	325	
Reverse Transfer Capacitance		C _{rss}	-	100	175	

SWITCHING CHARACTERISTICS (Notes 6 and 7)

Turn-On Delay Time	(V _{DD} = -10 Vdc, I _D = -2.4 Adc, V _{GS} = -4.5 Vdc, R _G = 6.0 Ω)	t _{d(on)}	-	10	20	ns
Rise Time		t _r	-	35	65	
Turn-Off Delay Time		t _{d(off)}	-	33	60	
Fall Time		t _f	-	29	55	
Turn-On Delay Time	(V _{DD} = -10 Vdc, I _D = -1.2 Adc, V _{GS} = -2.7 Vdc, R _G = 6.0 Ω)	t _{d(on)}	-	15	-	ns
Rise Time		t _r	-	40	-	
Turn-Off Delay Time		t _{d(off)}	-	35	-	
Fall Time		t _f	-	35	-	
Total Gate Charge	(V _{DS} = -16 Vdc, V _{GS} = -4.5 Vdc, I _D = -2.4 Adc)	Q _{tot}	-	10	18	nC
Gate-Source Charge		Q _{gs}	-	1.5	-	
Gate-Drain Charge		Q _{gd}	-	5.0	-	

BODY-DRAIN DIODE RATINGS (Note 6)

Diode Forward On-Voltage	(I _S = -2.4 Adc, V _{GS} = 0 Vdc) (I _S = -2.4 Adc, V _{GS} = 0 Vdc, T _J = 125°C)	V _{SD}	-	-0.88 -0.75	-1.0 -	Vdc
Reverse Recovery Time	(I _S = -2.4 Adc, V _{GS} = 0 Vdc, di _S /dt = 100 A/μs)	t _{rr}	-	37	-	ns
		t _a	-	16	-	
		t _b	-	21	-	
Reverse Recovery Stored Charge		Q _{RR}	-	0.025	-	μC

5. Handling precautions to protect against electrostatic discharge is mandatory.

6. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.

7. Switching characteristics are independent of operating junction temperature.

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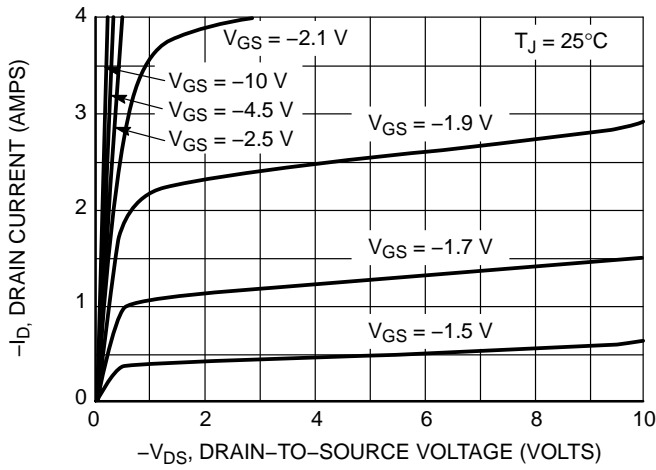


Figure 1. On-Region Characteristics.

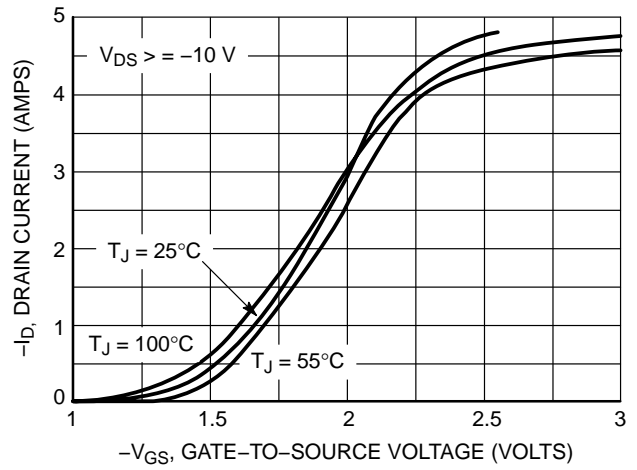


Figure 2. Transfer Characteristics.

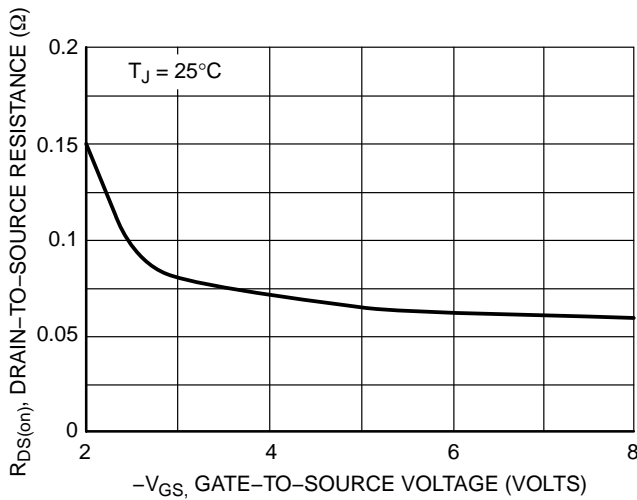


Figure 3. On-Resistance vs. Gate-to-Source Voltage.

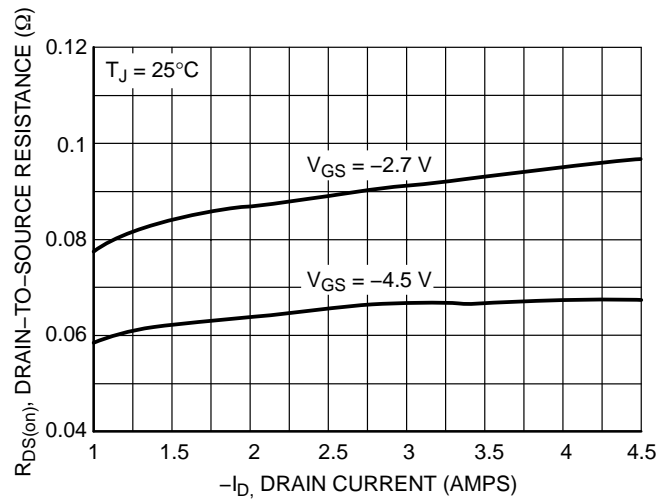


Figure 4. On-Resistance vs. Drain Current and Gate Voltage.

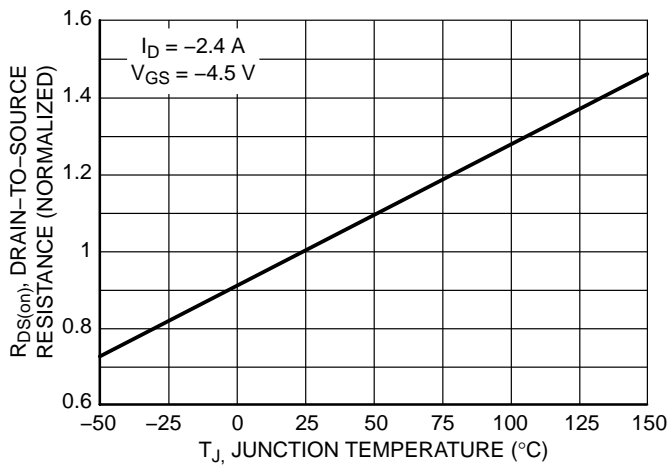


Figure 5. On-Resistance Variation with Temperature.

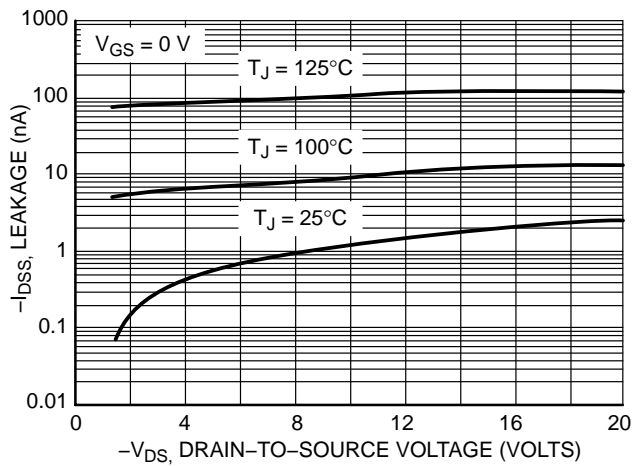


Figure 6. Drain-to-Source Leakage Current vs. Voltage.

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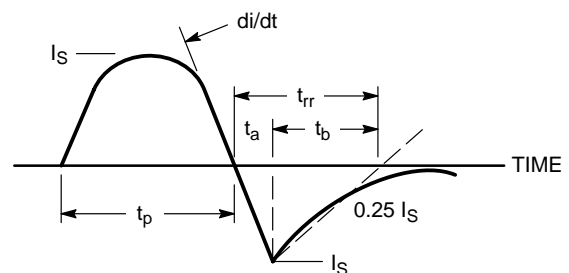
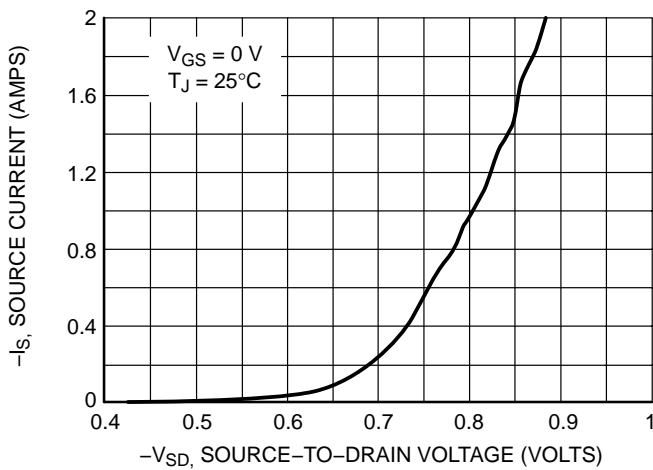
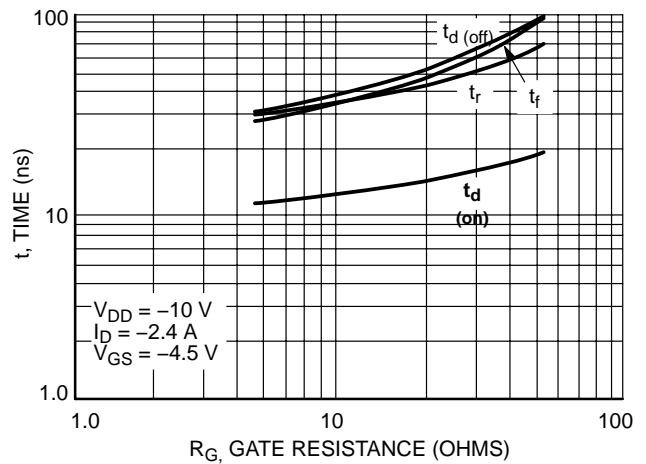
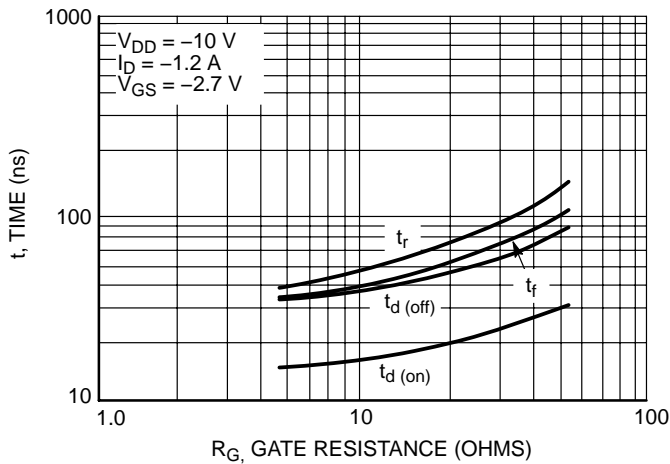
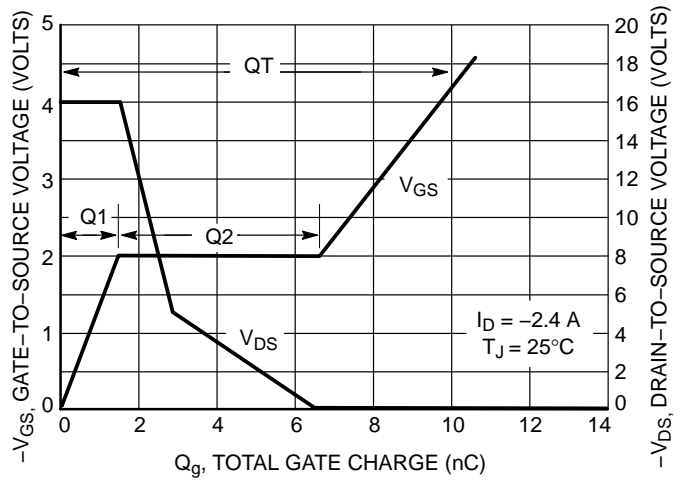
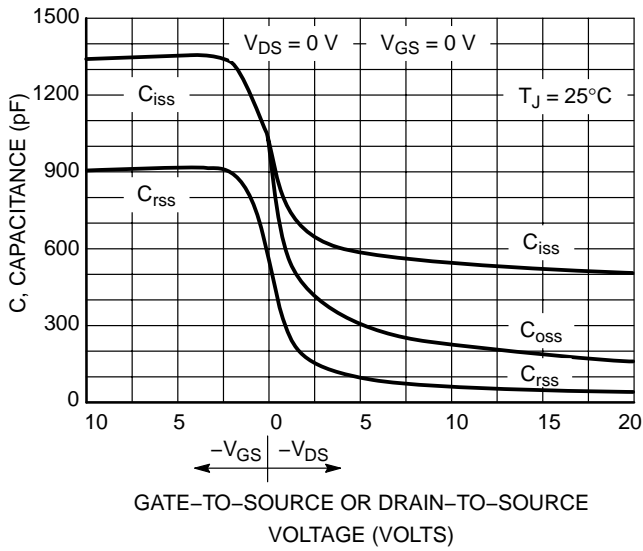


Figure 12. Diode Reverse Recovery Waveform

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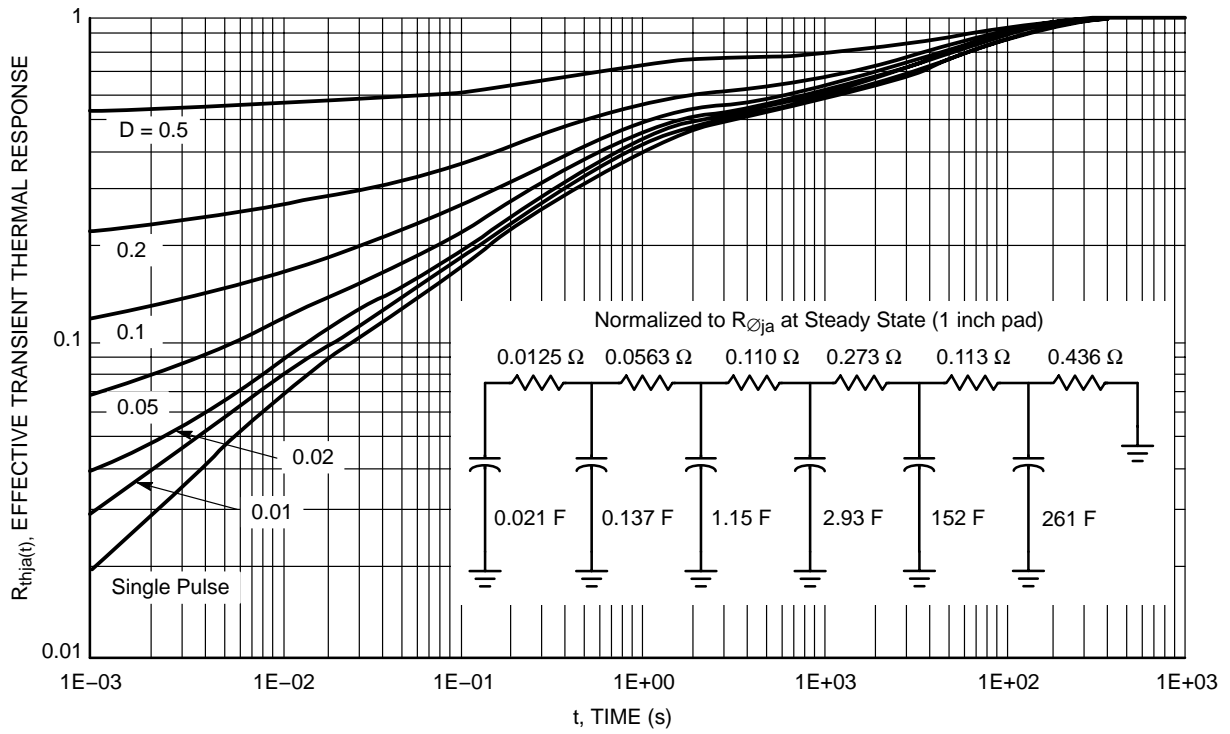
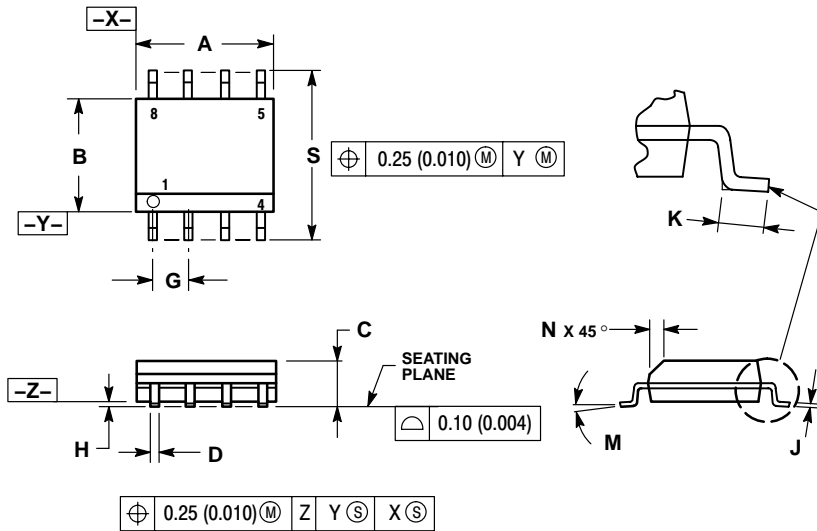


Figure 13. FET Thermal Response

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PACKAGE DIMENSIONS

SO-8
CASE 751-07
ISSUE AB



NOTES:

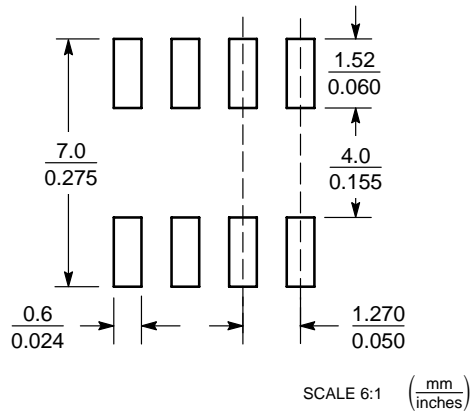
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 11:

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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