MN8355

Display Processor Unit(DPU)

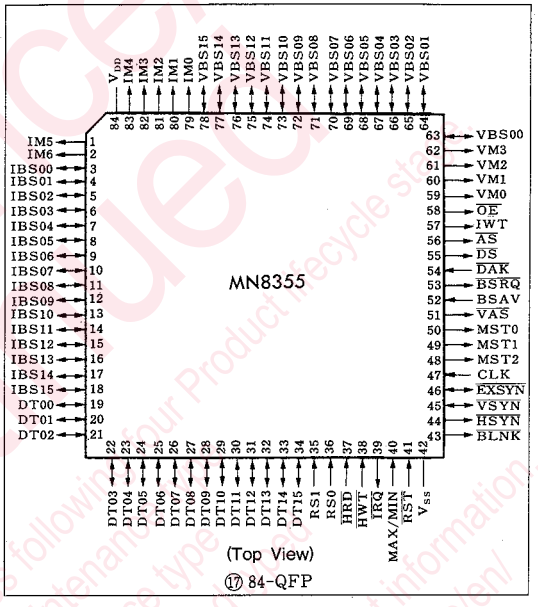
■ Outline

The DPU(Display Processor Unit)ME8355 is a basic LSI for a bit map multiwindow display unit which has realized flexible controls (non-interlace,interlace,interlace shrunk scan)for the CRT display unit,and high-speed data transfer control functions for the image memory,which stores original pictures,and the video memory,which stores CRT display data.

■ Features

- High-speed data transfer function
  High-speed transfer of rectangular area data in the video memory and image memory
  data enlargement/reduction
  8 kinds of operations for transfer-to data
- CRT display control function
  3 scan modes
- Cursor control function
  255 x 255 optionally shaped cursor display enabled
  Background data mask function at cursor display time
- Two dimensional coordiantes control function
  Specification of the two dimensional coordinates of data transfer control parameters for the video memory and image memory
- Flexible system configuration
  2 pin functions of MAX and MIN modes
- Memory space:1M words for the video memory,8M words for the image memory
- No.of display pixels:Max.4,096 x 4,096 dots
- Transfer control speed:500 ns/word(max.clock at 16 MHz)
- Internal and external buses of 16 bits/word
- 84-pin flag package

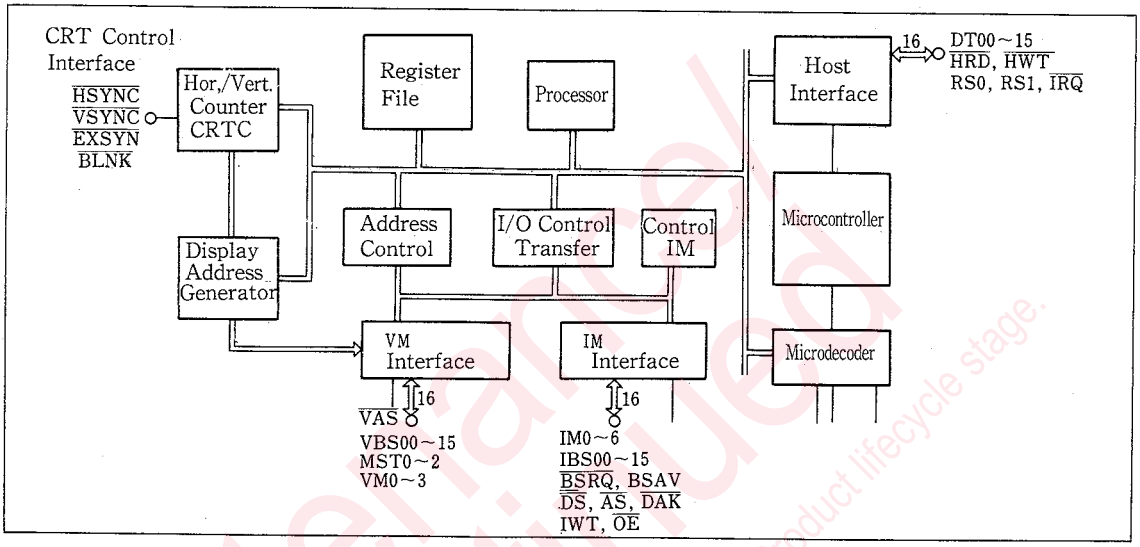
■ Pin Configuration



■ Applications

- Work stations
- Intelligent terminals
- Word processors
- Personal computers,etc.

■ Block Diagram



■ Absolute Maximum Ratings (T_a=95°C, T_j≦150°C)

Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3~7	V
Pin voltage	V_{IN}	−0.3~V_{DD}+0.3	V
Power consumption	P_D	400	mW
Operating ambient temperature	T_{opr}	0~+95	°C
Storage temperature	T_{stg}	−55~+150	°C

■ Recommended Operating Conditions

V_{DD}=5V±5%, V_{SS}=0V, T_{opr}=0 to 70°C

■ Electrical Characteristics

●DC Characteristics (V_{DD}=5V±5%, V_{SS}=0V, T_a=0 to 70°C)

Item		Symbol	Condition	min.	typ.	max.	Unit
Supply current		I_{DD}				80	mA
Power consumption		P_D				400	mW
Input voltage	Input pins other than CLK	V_{IH}	2.4 to V_{DD} for $\overline{HWT}$	2.0		V_{DD}	V
		V_{IL}		0		0.8	V
	CLK input	V_{ICH}		3.0		V_{DD}	V
		V_{ICL}		0		0.8	V
Input current	Input pin	I_{IN1}	V_{IN}=0.4V~V_{DD}	−10		10	μA
	3rd pin	I_{IN2}	V_{IN}=0.4V=V_{DD}	−10		10	μA
	Open drain	I_{IN3}		−150		10	μA
Output voltage	"H" output pin	V_{OH}	I_{OH}=−400μA	2.4		V_{DD}	V
	"L" 3rd pin	V_{OL}	I_{OL}=2mA	0		0.45	V
	"L" open drain	V_{OLOD}	I_{OL}=2mA	0		0.45	V
Input capacitance		C_T	f=1MHz, V_{offset}=2V		5		pF
Output capacitance		C_O	f=1MHz, V_{offset}=2V		10		pF

● AC Characteristics (V_{DD}=5V±5%, V_{SS}=0V, Ta=0 to 70°C)

1. Operating Conditions

Item	Symbol	Condition	min.	typ.	max.	Unit
Input clock cycle	t_{cyc}		62.5		1000	ns
Clock "H" level pulse width	t_{WH}		15			ns
Clock "L" level pulse width	t_{WL}		15			ns
Clock fall time	t_{CF}				10	ns
Clock rise time	t_{CR}				10	ns
$\overline{DS}$↘ $\overline{DAK}$↘	t_A		0			ns
$\overline{DAK}$↘ fall time	t_B				30	ns
$\overline{DS}$↗ ~$\overline{DAK}$↗	t_C		0			ns
$\overline{DAK}$↘ rise time	t_D				30	ns
Data delay time from $\overline{DAK}$↘	t_E	At read cycle time			50	ns
Data hold time to $\overline{DAK}$	t_F	At ready cycle time	0			ns
$\overline{BSRQ}$↘~$\overline{BSAV}$↗	t_G		0			ns
BSAV rise time	t_H				30	ns
$\overline{DS}$↘~$\overline{BSAV}$↘	t_I		0			ns
BSAV fall time	t_J			30	ns	
Setup time to CLK↗	t_a		40			ns
Hold time to CLK↗	t_b		3			ns
Setup time to CLK↗	t_c		30			ns
Setup time to CLK↗	t_d		30		ns	
RS0, RS1, setup time to $\overline{HWT}$, $\overline{HRD}$	t_{HA}		20			ns
RS0, RS1 hold time to $\overline{HWT}$, $\overline{HRD}$	t_{HB}		20			ns
Data setup time to $\overline{HWT}$	t_{HC}		20			ns
Data hold time to $\overline{HWT}$	t_{HD}		20			ns
$\overline{HWT}$ pulse width	t_{HE}		250			ns
$\overline{HRD}$ pulse width	t_{HF}		250			ns
$\overline{HWT}$, $\overline{HRD}$ fall time	t_{HG}			30	ns	
$\overline{HWT}$, $\overline{HRD}$ rise time	t_{HH}			30	ns	
Timer from $\overline{HWT}$↗ to $\overline{HRD}$↘	t_{HJ}		200			ns

2. Operation Characteristics (t_{cyc}=83.3ns (12MHz))

Item	Symbol	Condition	min.	typ.	max.	Unit
$\overline{BSRQ}$↘ through $\overline{AS}$↘	t_1	BSAV fixed at "H"	130		190	ns
Address setup time to $\overline{AS}$	t_2		50		100	ns
$\overline{OE}$↘~$\overline{AS}$↘	t_3		60		100	ns
IWT, IM0–6 preceding time to $\overline{AS}$	t_4		60		100	ns
$\overline{BSRQ}$ pulse width	t_5	BSAV fixed at "H"	130		190	ns
$\overline{AS}$↘~$\overline{DS}$↘	t_6		70		100	ns
Address hold time to $\overline{AS}$	t_7		70		120	ns
$\overline{AS}$↘~$\overline{OE}$↗	t_8	At read cycle time	70		100	ns
$\overline{DS}$ pulse width	t_9	$\overline{DAK}$ fixed at "L"	270		400	ns
$\overline{DAK}$↘~$\overline{DS}$↗	t_{10}		200		500	ns
$\overline{DS}$↗ through next $\overline{BSRQ}$↘	t_{11}		70			ns
$\overline{DS}$↗~$\overline{AS}$↗	t_{12}		70		100	ns

2. Operation Characteristics (tcyc = 83.3 ns (12MHz) (Continued))

Item	Symbol	Condition	min.	typ.	max.	Unit
IWT, IM0−6 hols time to $\overline{DS}$	t_{13}		70		110	ns
$\overline{DS}$ ↗ ~ $\overline{OE}$ ↗	t_{14}	At write cycle time	70		110	ns
Data hold time to $\overline{DS}$	t_{15}		70			ns
$\overline{AS}$ ↘ through data send	t_{16}	At write cycle	80		130	ns
BSAV ↗ through $\overline{AS}$ ↘	t_{17}		130		400	ns
CLK ↗ throgh $\overline{VAS}$ ↘	t_{20}		15		50	ns
Next CLK ↗ through $\overline{VAS}$ ↗	t_{21}		15		50	ns
CLK ↗ throgh address output	t_{22}		20		70	ns
Next CLK ↗ through address output stop	t_{23}		22		70	ns
CLK ↗ through MS0−2, VM0−3 send	t_{24}		20		70	ns
Next CLK ↗ through data output	t_{25}		22		70	ns
CLK ↗ through data stop	t_{26}		22		70	ns
CLK ↗ through MST0−2, VM0−3 stop	t_{27}		15		70	ns
CLK ↗ through $\overline{HSYN}$, $\overline{BLNK}$ output/stop	t_{28}				100	ns
CLK ↗ through $\overline{VSYN}$, $\overline{EXSYN}$ output/stop	t_{29}				150ns	
$\overline{BSRQ}$ ↘ ~ $\overline{ACT}$ ↘	t_{30}	BSAV fixed at "H"	70		110	ns
$\overline{ACT}$ ↘ ~ $\overline{DS}$ ↘	t_{31}		130		190	ns
Address setup time to $\overline{DS}$	t_{32}		110		190	ns
IWT, IM0−6 setup time to $\overline{DS}$	t_{33}		130		190	ns
Data setup time to $\overline{DS}$	t_{34}	At write cycle time	110		190	ns
$\overline{DS}$ ↗ through $\overline{ACT}$ ↗	t_{35}		70		100	ns
Address hold time to $\overline{DS}$	t_{36}		70		100	ns
Data hold time to $\overline{DS}$	t_{37}		70		100	ns
BSAV ↗ through $\overline{ACT}$ ↘	t_{38}		70		300	ns
Read access time	t_{40}	At read cycle time			150	ns
Data hold time	t_{41}	At read cycle time	5			ns

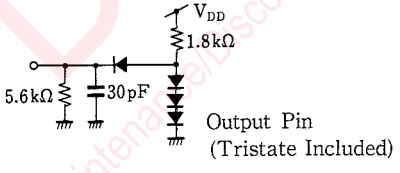
3. Operation Characteristics (tcyc = 62.5ns (16MHz))

Item	Symbol	Condition	min.	typ.	max.	Unit
$\overline{BSRQ}$ ↘ through $\overline{AS}$ ↘	t_1	BSAV fixed at "H"	100		150	ns
Address setup time to $\overline{AS}$	t_2		30		70	ns
$\overline{OE}$ ↘ ~ $\overline{AS}$ ↘	t_3		40		75	ns
IWT, IM0−6 preceding time to $\overline{AS}$	t_4		40		75	ns
$\overline{BSRQ}$ pulse width	t_5	BSAV fixed at "H"	100		150	ns
$\overline{AS}$ ↘ ~ $\overline{DS}$ ↘	t_6		40		75	ns
Address hold time to $\overline{AS}$	t_7		40		100	ns
$\overline{AS}$ ↘ ~ $\overline{OE}$ ↗	t_8	At read cycle time	40		80	ns
$\overline{DS}$ pulse width	t_9	$\overline{DAK}$ fixed at "L"	200		300	ns
$\overline{DAK}$ ↘ ~ $\overline{DS}$ ↗	t_{10}		150		400	ns
$\overline{DS}$ ↗ through next $\overline{BSRQ}$ ↘	t_{11}		40			ns

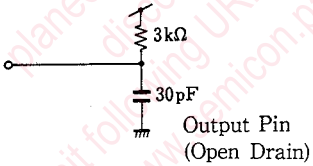
3. Operation Characteristics (tcyc=62.5ns (16MHz) (Continued))

Item	Symbol	Condition	min.	typ.	max.	Unit
$\overline{DS}$ ↗ ~ $\overline{AS}$ ↗	t_{12}		40		75	ns
IWT, IM0−6 hold time to $\overline{DS}$	t_{13}		40		80	ns
$\overline{DS}$ ↗ ~ $\overline{OE}$ ↗	t_{14}	At write cycle time	40		80	ns
Data hold time to $\overline{DS}$	t_{15}		40			ns
$\overline{AS}$ ↘ through data send	t_{16}	At write cycle time	60		110	ns
BSAV ↗ through $\overline{AS}$ ↘	t_{17}		100		300	ns
$\overline{CLK}$ ↗ through $\overline{VAS}$ ↘	t_{20}		15		50	ns
Next CLK ↗ through $\overline{VAS}$ ↗	t_{21}		15		50	ns
CLK ↗ through address output	t_{22}		20		70	ns
Next CLK ↗ through address output time	t_{23}		22		70	ns
CLK ↗ through MST0−2, VM0−3 stop	t_{24}		20		70	ns
Next CLK ↗ through data stop	t_{25}		22		70	ns
CLK ↗ through data stop	t_{26}		22		70	ns
CLK ↗ MST0−2, VM0−3 stop	t_{27}		15		70	ns
CLK ↗ through $\overline{HSYN}$, $\overline{BLNK}$ output/stop	t_{28}				100	ns
CLK ↗ through $\overline{VSYN}$, $\overline{EXSYN}$ output/stop	t_{29}				150	ns
$\overline{BSRQ}$ ↘ ~ $\overline{ACT}$ ↘	t_{30}	BSAV=fixed at "H"	40		75	ns
$\overline{ACT}$ ↘ ~ $\overline{DS}$ ↘	t_{31}		100		150	ns
Address setup time to $\overline{DS}$	t_{32}		90		150ns	
IWT, IM0−6 setup time to $\overline{DS}$	t_{33}		100		150	ns
Data setup time to $\overline{DS}$	t_{34}	At write cycle time	90		150	ns
$\overline{DS}$ ↗ through $\overline{ACT}$ ↗	t_{35}		40		75	ns
Addres hold time to $\overline{DS}$	t_{36}		40		75	ns
Data hold time to $\overline{DS}$	t_{37}		40		75	ns
BSAV ↗ through $\overline{ACT}$ ↘	t_{38}		40		230	ns
Read access time	t_{40}	At read cycle time			150	ns
Data hold time	t_{41}	At read cycle time	5			ns

● AC Characteristics Measuring Load



Output Pin
(Tristate Included)



Output Pin
(Open Drain)

■ Pin Descriptions(MAX Mode)

Pin No.	Symbol	I/O	Description
1 2 79～83	IM5 IM6 IM0～IM4	O	Upper 7bits of the image memory address (lower 16bits are sent in a time sharing manner through IBS00-IBS15.
3～18	IBS00～IBS15	I/O	Pins to serve as data transfer routes between the inside of the DPU and the image memory. Data infromation and address infromation is inputted/outputted synchronously with DS and AS, respectively. IBS00 is the MSB.
19～34	DT00～DT15	I/O	Pins to serve as communication routes for command parameters and read data between the DPU and host processor
35 36	RSI RS0	I	Pins to select communication registers inside the DPU
37	$\overline{HRD}$	I	Pin to specify a transfer direction at DT00-DT15.
38	$\overline{HWT}$	I	Pin to specify a transfer direction at DT00-DT15. Write data for DT00-DT15 is latched at a rear edge.
39	$\overline{IRQ}$	O	Interrupt request signal due to a factor caused inside the DPU. It is outputted as far as there exists an interrupt factor.
40	MAX/MIN	I	MAX/MIN mode switching input. MAX mode at “H” level input time, and MIN mode at “L” level input
41	$\overline{RST}$	I	Reset input pin
42	V_{SS}	—	GND
43	$\overline{BLNK}$	O	Blanking control signal output pin to the CRT unit
44	$\overline{HSYN}$	O	Horizontal sync. signal output pin to the CRT unit
45	$\overline{VSYN}$	I/O	Vertical sync. signal output pin to the CRT unit
46	$\overline{EXSYN}$	I/O	Functions as an output pin when the DPU is placed in the master mode, and as an input pin when placed in the slave mode. In the master mode, it outputs the VSYNC signal at non-interlace time, and only the VYNC signal for an odd-number field at interlace time.
47	CLK	I	Clock input pin to the DPU. Clock with one fourth cycle of a basic video memory cycle
48～50	MST2～MST0	O	Cycle status signal to the video memory. Outputted synchronously with VAS.
51	$\overline{VAS}$	O	Sync. signal to access the video memory. always outputted at 4 clocks a cycle. Used to synchronize the peripheral circuit, which control the video memory, and a DPU operation timing.
52	BSAV	I	Response signal to the BSRQ signal. Data transfer starts when logic “1” of this signal is detected after sending the BSRQ signal.
53	$\overline{BSRQ}$	O	Bus use right request signal outputted prior to data transfer
54	$\overline{DAK}$	I	Response signal to DA outputted from the DPU. Used as an image memory data latch check signal at data send time, and used to inform the DPU at data input time that data infromation to be inputted has been set on the bus.

■ Pin Descriptions(MAX Mode) (Continued)

Pin No.	Symbol	I/O	Description
55	$\overline{DS}$	O	Data information I/O sync. signal. Logic "1" one clock after the AS signal is sent. At data send time, data is sent to BS00-BS14 simultaneously when this signal is set to logic "1", and after this signal is set to logic "0", data send stops one clock later.
56	$\overline{AS}$	O	Control signal to indicate a timing for the DPU to send the lower 16bits of the image memory address to BS00-BS15.
57	IWT	O	Control pin for the DPU to infrom the image memory of a transfer direction. When this signal is of logic "0", it indicates a transfer from the DPU to the image memory.
58	$\overline{OE}$	O	Data transfer control pin for IBS00-IBS15. Set to logic "1" at the timing from the DPU to send address information or write data information.
59~62	VM0~VM3	O	Upper 4-bit adress pins to access the video memory. Sent when the DPU accesses the video memory. VMO is the MSB.
63~78	VBS00~VBS15	I/O	Pins to serve as data transfer routes between the inside of the DPU and image memory. Address information is outputted synchronously with the VAS signal. VBS00 is the MSB.
84	V_{DD}	—	+5V power connection pin

The image bus and host bus in the MAX mode are put in one channel as for a pin configuration in the MIN mode.

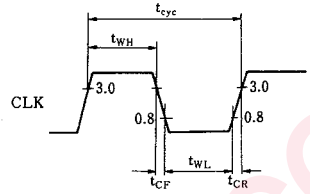
	MAX Mode	MIN Mode	
Image Bus (Address Data Time Sharing) ←	IBS00~IBS15	ADR00~ADR15	→ Image Memory Address Bus
Host Bus ←	DT00~DT15	BS00~BS15	→ Host Image Bus
Address Sync. Signal ←	$\overline{AS}$	—	
	$\overline{OE}$	$\overline{ACT}$	

■ Pin Descriptions(MIN Mode)

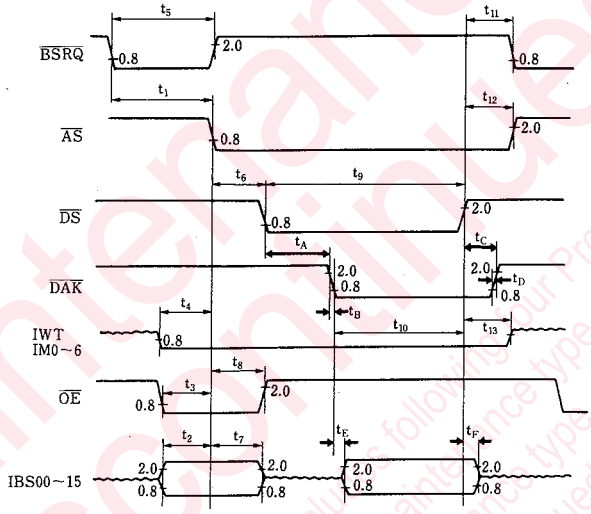
Pin No.	Symbol	I/O	Description
58	$\overline{ACT}$	O	Control signal to indicate that the DPU occupies the image bus (host bus) and executes a bus transfer cycle.
3~18	ADR00~ADR15	O	The lower 15bits of the image (or host) memory address are sent synchronously with the ACT signal.
19~34	BS00~BS15	I/O	Bus to serve as a command/parameter communication route between the DPU and host processor, and an information transfer route between the image memory and DPU.

■ Timing Diagrams

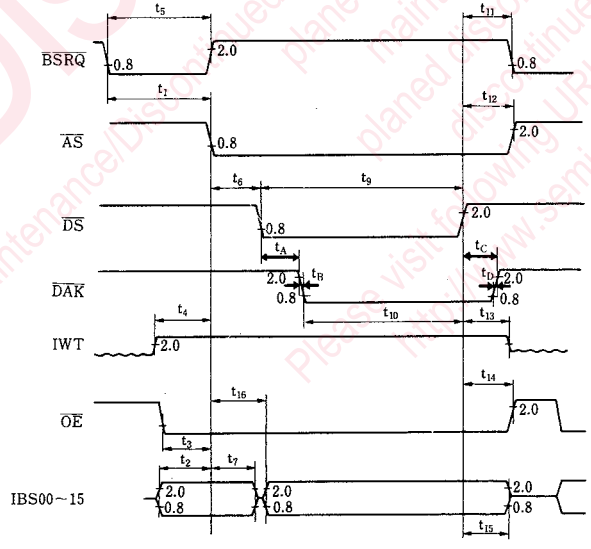
● External Clock Input Timing



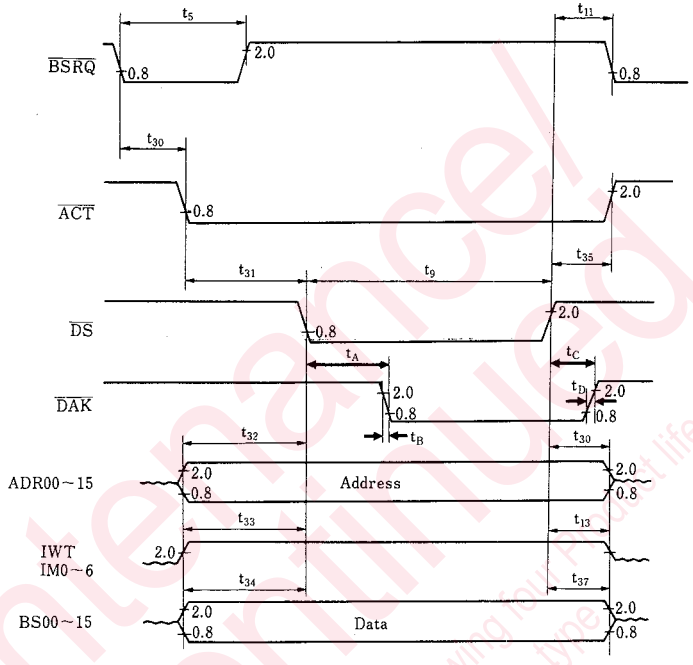
● Image Memory Read Timing (MAX Mode)



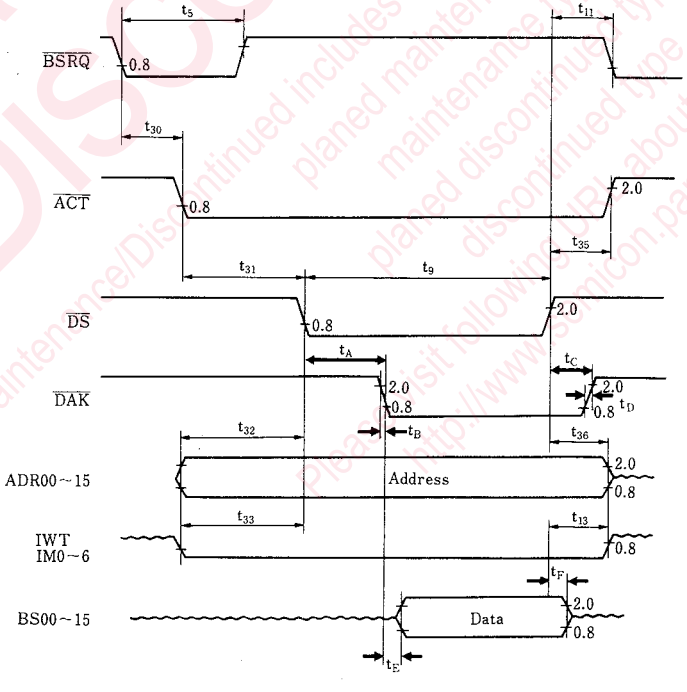
● Image Memory Write Timing (MAX Mode)



● Image Memory Write Timing (MIN Mode)

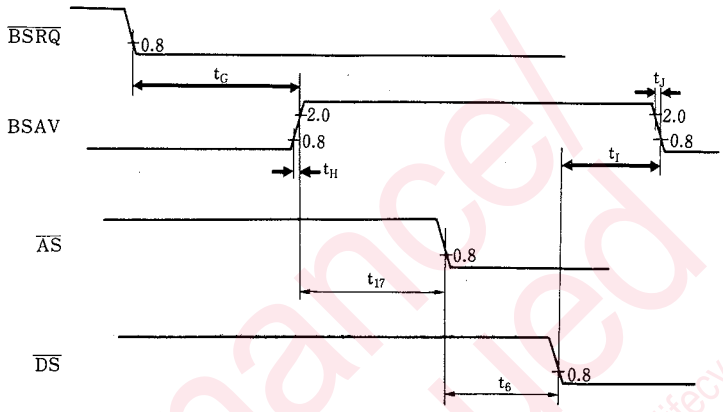


● Image Memory Read Timing (MIN Mode)

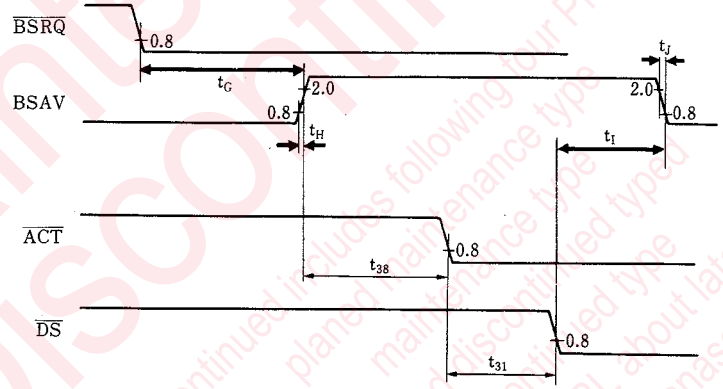


● $\overline{\text{BSRQ}}$, BSAV Timing

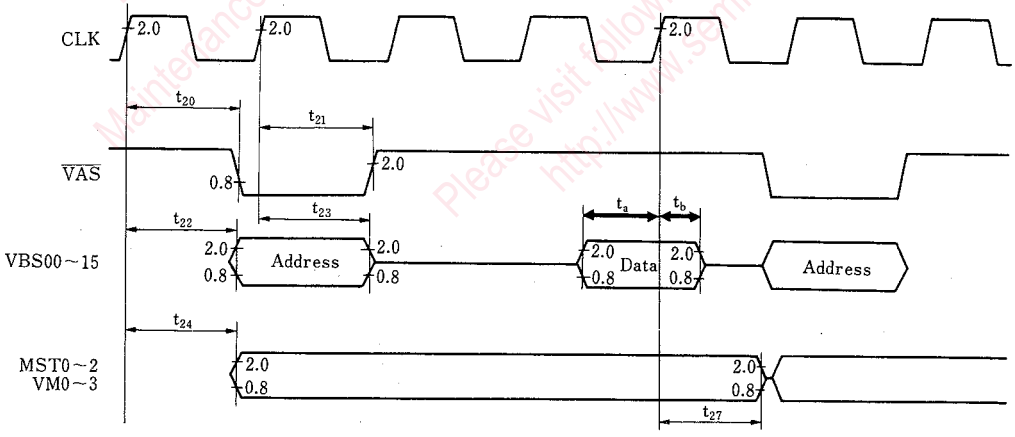
(MAX Mode)



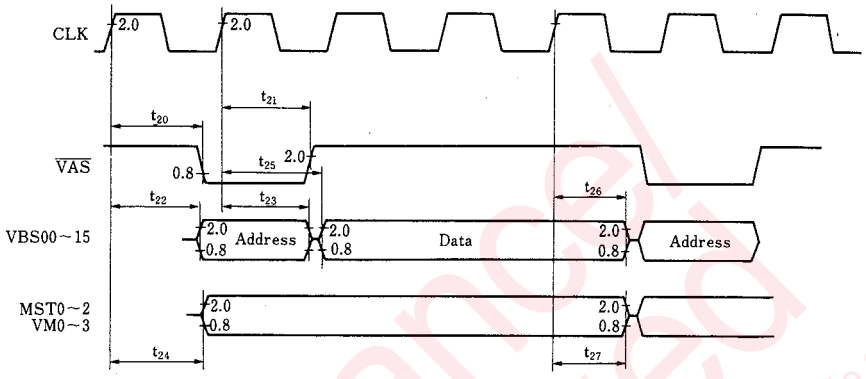
(MIN Mode)



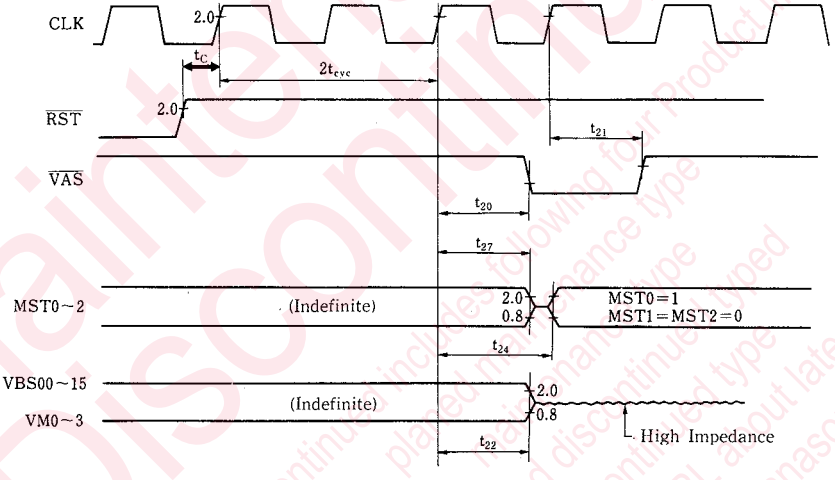
● Video Memory Read Timing



● Video Memory Write Timing

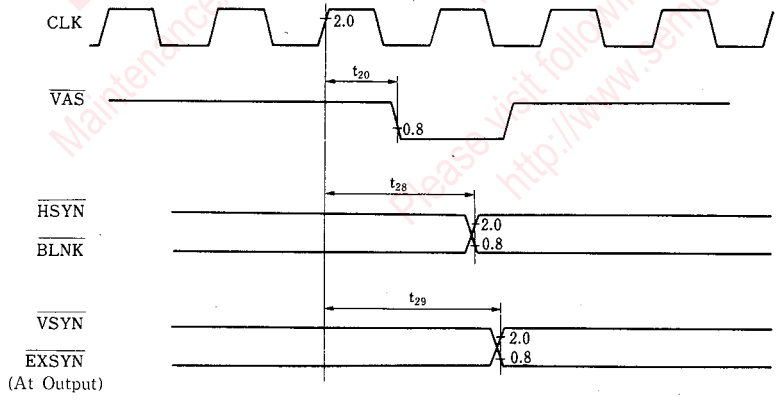


● $\overline{RST}$ Signal and VM Interface



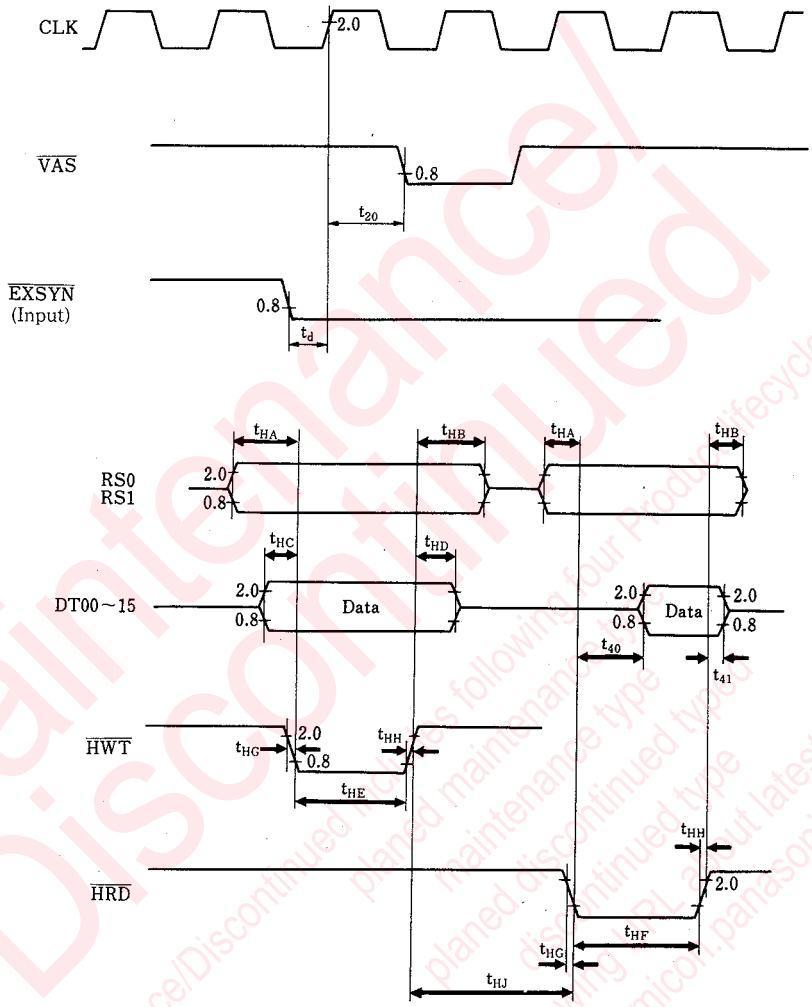
Indefinite means the state where electrical high/low level or high impedance cannot be prescribed.

● $\overline{HSYN}$, $\overline{BLNK}$, $\overline{VSYN}$ Signal Timing



■ Timing Diagrams (Continued)

● EXSYN Input Timing

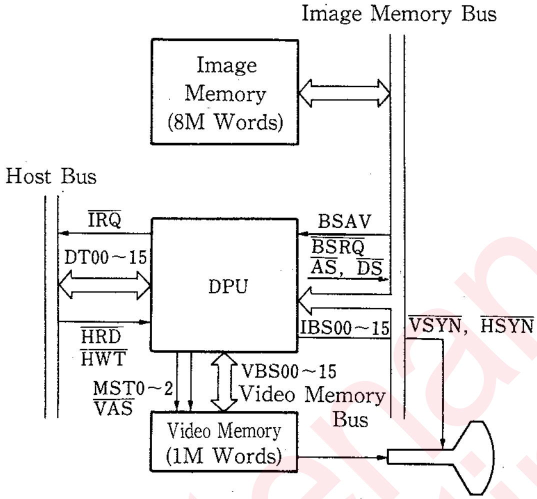


■ DPU Command System

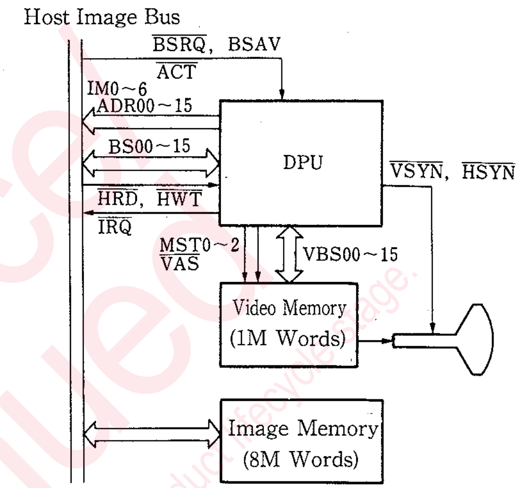
- Command
  - System Definition Command
    - Space Definition Command
    - Video Memory Structure/CRT Sync.
    - Cursor/Line Pattern/Scale Factor Definition Command
  - Operation Command
    - Pointer Control Command
    - Point Plot Command
    - Line Plot Command
    - Area Transfer Command
    - Cursor Command Command
    - CRT Display Control Command
    - Stop Command
  - User Microprogram Control Command

System Configuration

(MAX Mode)



(MIN Mode)



Specifications

Item		Description
Package		84-pin flat package
Process		2μm, CMOS
Integration		Approx. 85,000 elements
Max. clock		16MHz
Memory cycle	Video memory	250ns (max.)*3) (Sync. system)
	Image memory	500ns (max.)*3) (async. system)
Bus width		16bits/word for both internal and external
Memory space	Video memory	1M words*1)
	Image memory	8M words
No. of display pixels		Max. 4,096×4,096 dots
Transfer control	Speed	500ns/word*3)
	Scale factor	1/n~n (n=1~16)
	Min. unit	1 dot
	Raster operation	8 kinds of operations
CRT control	Scan mode	3 kinds
	External sync.	Enabled (VSYN signal)
Cursor control		Optionally shaped (255×255 dots) cursor mask controllable
Graphic		Point draw (direct/relative address)*2)
		Horizontal/vertical segment draw*2)

*1) Cursor working area included
*2) Line pattern register designation
*3) At maximum clock (16MHz)

■ Commands List

Group	Command	Mnemonic	Instruction Code and Parameter
Command Definition System	Space definition command	DFSRCS	0 1 0 1 1 0 0 0 0 0 0 0 0 0 0 V
			SWDT
			SORGH
			SORGL
		DFDSTS	0 1 0 1 1 0 1 0 0 0 0 0 0 0 0 V
			DWDT
			DORGH
			DORGL
	Video memory structure/CRT sync. timing definition command	SYNC	0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0
			HFP
			HS
			HBP
			DPR2
			DPR1
			VS
			VBP
			LPF
			VFP
			ATR
			NR
			PCH
			1 EXS PRI MD SCH IL PF 0 1 1 1 1
	Cursor defintion command	DFCSS	0 1 0 1 1 1 0 0 0 0 0 0 0 0 0 0
			CWDT
			CORGH
			CORGL
		STCS	1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0
			△X
			△Y
			X
			Y
		STCSM	1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 1
			△X
			△Y
			XM
			XY
			XC
			YC

■ Commands List (Continued)

Group	Command	Mnemonic	Instruction Code and Parameter
System definition command.	Scale factor definition command	STZM	0 1 0 1 0 0 1 1 0 0 0 0 0 0 0 0 MX ZX MY ZY
	Line pattern definition command	STPTR	0 1 0 1 0 0 0 1 0 0 0 0 0 0 0 0 DATA
Operation Command	Pointer control command	STSRCP	0 1 0 1 0 1 1 0 0 0 0 0 0 0 0 R X/△X Y/△Y
		STDSTP	0 1 0 1 0 1 1 1 0 0 0 0 0 0 0 R X/△X Y/△Y
		FXSRCP	0 1 0 1 0 1 0 0 0 0 0 0 0 0 0 0 PADRH PADRL
		FXDSTP	0 1 0 1 0 1 0 1 0 0 0 0 0 0 0 0 PADRH PADRL
	Point plot command	RSET	0 0 0 0 0 0 PT S 0 0 0 0 ROP R X/△X Y/△Y
		PSETS	0 0 MD PT S 0 0 0 0 ROP 0
	Line plot command	HLINE	0 1 0 0 0 1 0 D 0 0 0 0 ROP 0 △X
		VLINE	0 1 0 0 0 1 1 D 0 0 0 0 ROP 0 △Y
	Area transfer command	MV	1 0 0 1 Z 0 0 0 0 DIR B ROP 0 △X △Y
	Cursor control command	STRTCS	1 1 0 1 0 M 0 0 0 0 ROP 0 X Y
		MVCS X/△X Y/△Y	1 1 1 1 0 M 0 0 0 0 ROP R
		STPCS	1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0

■ Commands List (Continued)

Group	Command	Mnemonic	Instruction Code and Parameter														
Operation Command	CRT Display Control Command	STDADR	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0
			DADRH														
			DADRL														
		DSTRT	0	1	1	0	1	0	0	0	0	0	0	0	0	0	1
		DSTP	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Parameter Read Command	RDSRCP	0	1	1	1	0	0	1	0	0	0	0	0	0	0	C
		RDDSTP	0	1	1	1	0	1	0	0	0	0	0	0	0	0	C
		RDCSP	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0
		RDSRCD	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0
		RDDSTD	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
		RDMD	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Stop Command	HLT	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0
User Microprogram Control Command	User microprogram control command	LDMP	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
			IMADRH														
			IMADRL														
		SVMP	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1
			IMADRH														
			IMADRS														
		EXMP	1	0	1	1	ENT			0	0	0	0	0	0	0	0

Note) Unused bits in parameters shold be basically Ø.

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