AN280
Application note

Controlling voltage transients in full-bridge driver applications

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Introduction

In applications that involve fast switching of inductive loads, designers must consider the voltage transients that are generated in such applications.To insure a reliable design, the voltage transients must be limited to a level that is within the safe operating conditions of the switching device. This application note discusses the sources of voltage transients in full-bridge applications and techniques that can be used to limit these overvoltage conditions to safe levels. Special attention is given to applications using monolithic implementations of full-bridge circuits like the STMicroelectronics L6201, L6202 and L6203. In this note the example circuits generally show the L6203, but the same circuit can be used with the L6201 and the L6202.

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1 Maximum ratings

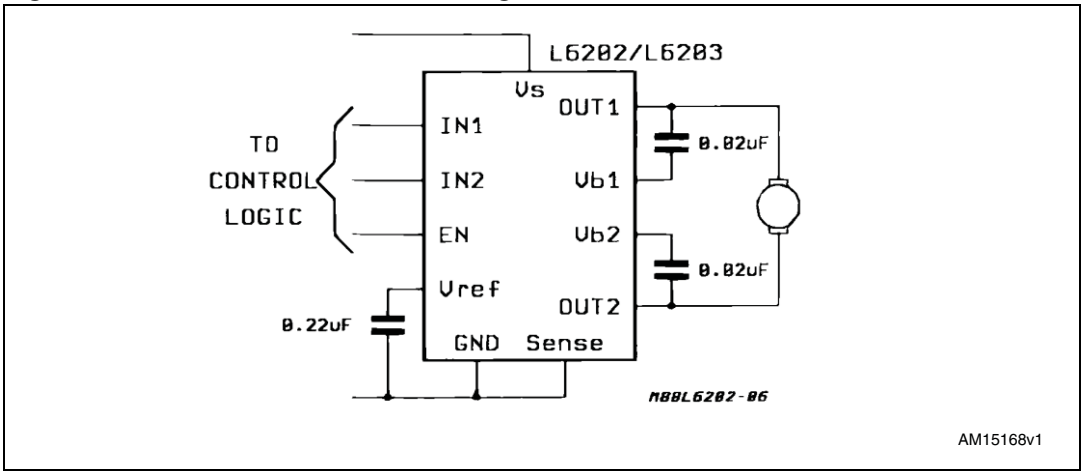
The maximum voltage rating for the bridge driver can be derived from the maximum ratings of the devices used in the output stage and are generally the BV_{ceo} or BV_{dss} of the power devices. In addition to the maximum allowable voltage across the output device, additional limits may be needed on the maximum output voltage above supply or below ground, depending on the implementation of the output stage.

As an example of a full-bridge circuit, consider the STMicroelectronics L6201, L6202 and L6203. These devices are full-bridge drivers implemented with DMOS transistors on a monolithic structure. Using these devices full-bridge drive circuits, like shown in *Figure 1*, are easily implemented. The device has a maximum rating for the supply voltage of 60 V, which implies a maximum BV_{dss} for the output devices of 60 V. In addition, due to the monolithic implementation, the voltage between the two output terminals must not exceed 60 V. Therefore, the maximum ratings that must be considered for the application are:

- V_{supply}: 60 V
- V_{ds} any output: 60 V
- V_{01} - V_{02}: 60 V

Similar maximum ratings exists for any full-bridge application, with the exception of the differential output voltage limit, which doesn't exist for discrete implementations.

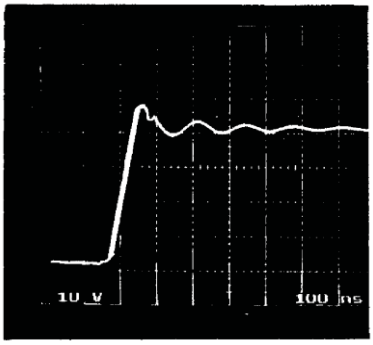
Figure 1. DC motor drive circuit using the L6203



2 Source of voltage transients

To protect against the overvoltage that may occur as a result of the inductive property of the load, voltage clamps are normally employed to limit the voltage across the output devices. In bridge applications these clamps are normally a diode bridge that clamps the voltage to one diode drop above supply and one diode drop below ground. However, if the diode switches slower than the transistor, there is a short time where neither the transistor nor the diode is conducting and the voltage rise is limited only by the capacitance on the node. The result is that a voltage overshoot occurs during the time before the diode turns-on. When the bridge is built with DMOS power transistors, the intrinsic body diode is often used as the clamp. This is true for the L6201, L6202 and L6203. As can be seen in the *Figure 2*, the turn-off time of the DMOS device in the L6203 is in the range of 25 to 50 ns while the turn-on time of the intrinsic drain to source diode is in the range of 150 ns. This difference in switching time is characteristic of many DMOS devices.

Figure 2. Output switching waveform for the L6203



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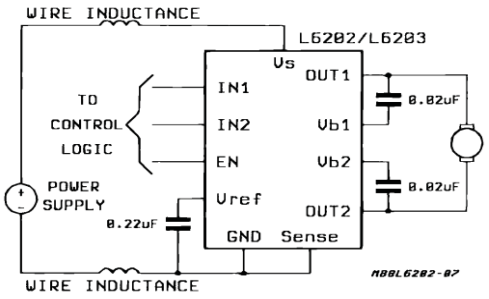
The second main factor contributing to the transients is the parasitic inductance in the wiring or printed circuit board layout. *Figure 3* shows the parasitic inductances in the DC motor application. When the current flowing in these parasitic inductances is rapidly switched, the inductive property of the wire causes a voltage transient. When large currents are rapidly switched, as with DMOS transistors, large voltage transients can be induced across even small parasitic inductances. For an inductive load driven by an H-bridge the change of current in the power supply lead is equal to twice the load current when the bridge is switched off or the bridge is switched from one diagonal pair of transistors being on the other pair. The time that it takes to switch the current is essentially the turn-off time of the output device. In this case the resulting voltage across the inductance is given by the equation:

Equation 1

$$V = L \cdot \frac{di}{dt} = L \cdot 2 \cdot \frac{II}{Toff}$$

Figure 3. Parasitic wiring inductances in DC motor drive circuit

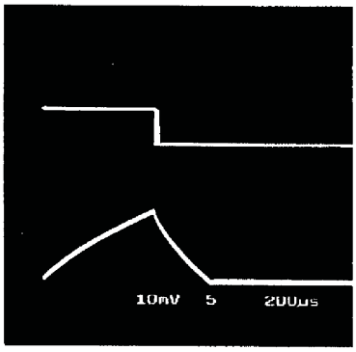


In fast switching applications, using the L6202, where the switching time is as short as 25 ns, the induced voltage spike can become quite large. For example if the DC motor in *Figure 3* was driven with 4 A and the bridge was switched off, a parasitic inductance of only 15 nH produces a 5 V spike. Since the current is reversed in both the supply and ground leads the device can see a 10 V spike between the power supply pin and chip ground, if the inductance of both wires are the same.

As a design example, consider a DC motor driver shown in *Figure 1* with the following system characteristics:

- Supply voltage: max 46 V, min 38 V
- Peak motor current: 5 A
- Chopping frequency: 50 kHz

Figure 4. Enable input and motor current for examples



For evaluation, the motor is driven with a peak current of 4 A. *Figure 4* shows the input signal for the L6202 on the Enable pin and the motor current used in the evaluation.

Here the bridge is energized and the load current is allowed to build up to 4 A. When the 4 A peak is reached, the bridge is disabled and the current decays through the intrinsic diodes in the DMOS power stage. All figures in the remainder of this note are taken under these operating conditions.

3 Power supply filtering

To reduce the effect of the wiring inductance a good high frequency capacitor can be placed on the board near the bridge circuit to absorb the small amount of inductive energy in the leads. It should be noted that this capacitor is usually required in addition to an electrolytic capacitor, which has poor performance at high frequencies.

3.1 Operating voltages

Figure 5. Supply voltage

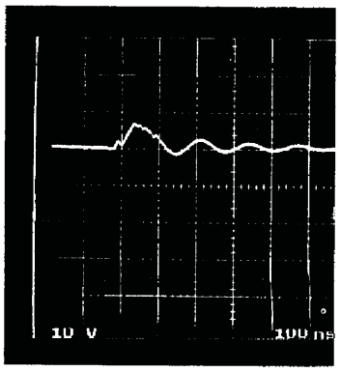


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Figure 5 and *Figure 6* show the spike on the power supply pin of the L6203 and the output pins when the bridge was disabled. These waveforms were present when the device was mounted on a printed circuit board where reasonable care was taken in the layout. When a 0.2 µF polyester capacitor was connected between the supply and ground pin of the L6203 the voltage spike on the power supply was significantly reduced, as shown in *Figure 7*.

Figure 6. V_{01} - V_{02}

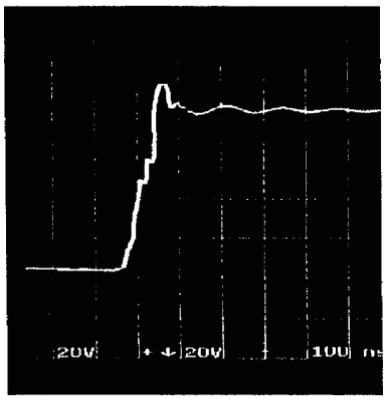

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Figure 7. Supply voltage with 0.2 µF bypass capacitor on supply pin

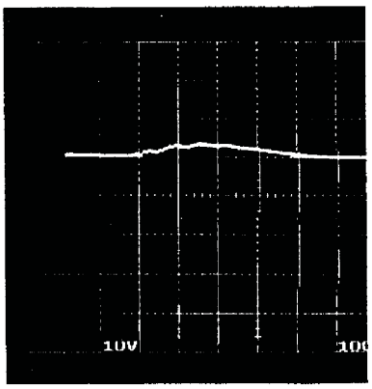
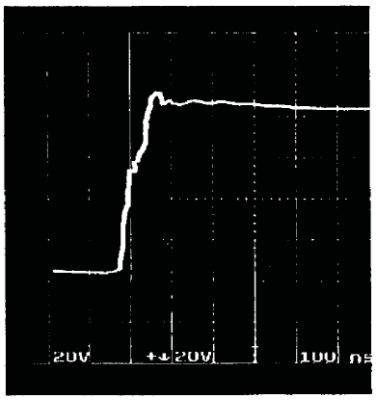


Figure 8. V_{01} - V_{02} with 0.2 µF bypass capacitor on supply pin



Looking at the voltage waveform at the output terminals of the L6202, shown in *Figure 8*, a large spike is still present. The worst case spike is measured between the output terminals of the device (V_{out1} - V_{out2}) since the spikes above the supply and below ground are both present. After the voltage spike on the power supply was eliminated, the transients on the output must be related to the mismatch of switching times between the diodes and power transistors. To control these spikes two possible alternatives are present

1. use faster diodes
2. use an external circuit to slow the voltage rise time across the output when the transistors are turned off

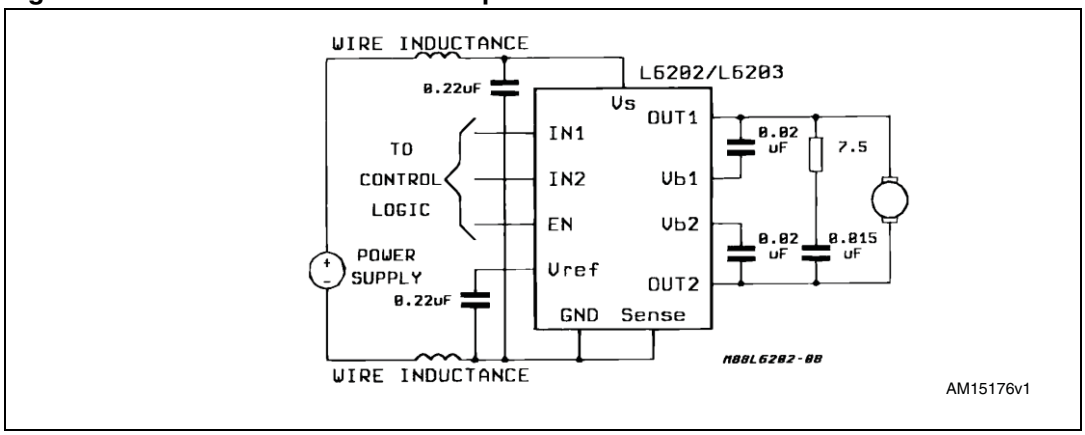
Schottky diodes externally connected to the L6203 would more closely match the switching time of the DMOS power transistors, but they are expensive and require additional board space.

Slowing down the output voltage rise time can be accomplished by connecting a snubber network across the output terminals of the device. *Figure 9* shows the connection for a RC snubbing circuit used with the L6203. With properly selected values the slope of the voltage waveform can be limited to where the diodes have sufficient time to turn on and clamp the remaining inductive energy.

4 Snubber design considerations

The function of the snubber network is to limit the rate of change of the voltage across the motor (output terminals of the L6203) when one of the DMOS devices is turned off. Using the RC snubbing circuit shown in *Figure 9*, the rate of change of the voltage on the output is dominated by the capacitor while the resistor is used primarily to limit the peak current flowing through the power transistor when it turns on.

Figure 9. RC snubber circuit on output



The time constant of the motor current is much longer than the switching time, due to the inductance of the motor. At the time of switching the DC motor can be assumed to be a constant current generator equal to the peak current at switching. If this current is switched into the snubber, the voltage across the snubber network jumps to a value equal to the snubber resistance times the motor current. After the initial step, the rate of change is limited by the motor current charging the snubber capacitor. To properly size the snubber network the resistor is selected such that the maximum motor current produces a voltage less than the minimum power supply voltage. If the resistor is larger than this value, the snubber is ineffective since the capacitor doesn't limit the voltage rise until the voltage has become greater than the power supply. For the design example, the maximum resistance for the snubber is given by the equation:

Equation 2

$$R_{max} = \frac{V_{smin}}{I_{peak}} = \frac{38V}{5A} = 7.6 \text{ ohm}$$

The snubber capacitor is calculated from the peak current and the target rise time. The capacitance is given by the equation:

Equation 3

$$C = Ipeak\frac{dt}{dv} = 5A\frac{150ns}{50V} = 0.015\ \mu F$$

When the snubber network is installed in the application the voltage transients on the terminals of the L6203 are greatly reduced, as shown in *Figure 11*. The drawback of a snubber network of this type is that a current spike flows into the transistor when it is switched on as the capacitor is discharged. The theoretical peak value of this spike is given by the equation:

Equation 4

$$I = \frac{V_{smax}}{R} = \frac{42V}{7.5ohm} = 5.6\ A$$

Figure 10. Supply voltage with snubber

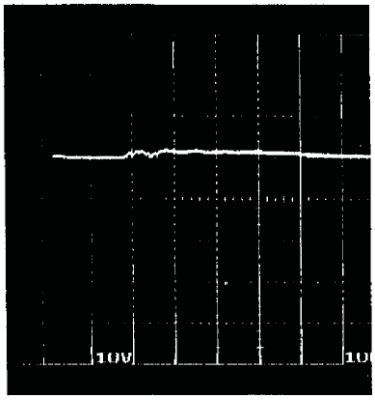
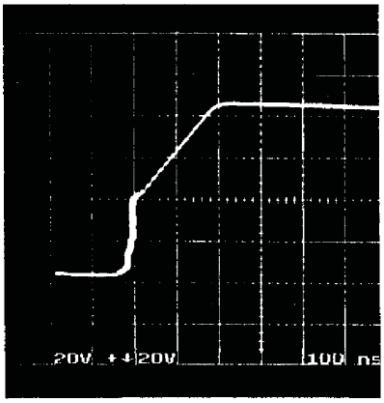


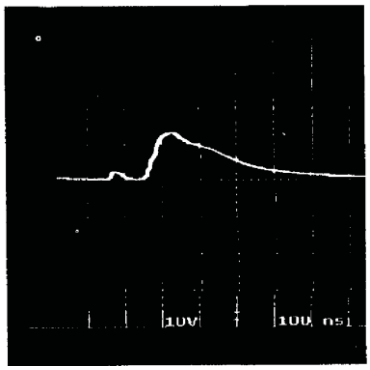
Figure 11. V_{01} - V_{02} with snubber



This peak current flowing in the snubber is added to the load current when the device is turned on and the total peak current in the transistor is the sum of the snubber circuit current plus the load current. In practice, the peak current measured is usually much less than the calculated peak, due to the capacitors internal resistance and the resistor inductance. *Figure 12* and *Figure 13* show the peak current in the snubber network in the design example.

4.1 Current in the snubber circuit

Figure 12. Turn-on 2.0 A/div



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The power dissipated in the snubber resistor is the sum of the dissipation during the turn-on and turn-off of the bridge. The resistor dissipation is:

Equation 5

$$Pd = (I1^2 \cdot R \cdot DC) + (I2^2 \cdot R \cdot DC)$$

where

- I1 = current at turn-on
- I2 = current at turn-off
- R = snubber resistor
- DC = duty cycle of current flow

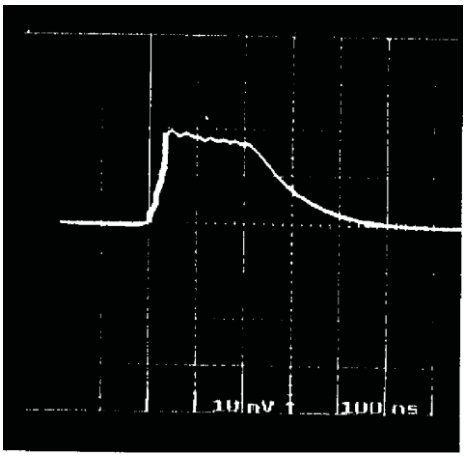
For the design example the power dissipation, not considering the duty cycle is:

Equation 6

$$Pd = ((2.5)^2 \cdot 7.5 \cdot 0.0\dot{1}) + ((5)^2 \cdot 7.5 \cdot 0.0\dot{1}) = 0.469 + 1.875 = 2.344W$$

If the device is chopping for only a portion of the time the dissipation in the resistor is reduced.

Figure 13. Turn-off 2.0 A/div



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5 Conclusion

With the 0.2 µF bypass capacitor and the snubber circuit in place the voltage transients measured in the application have been limited to within safe values for the L6202. As shown in *Figure 10* and *Figure 11*, the power supply voltage, the voltage across each of the DMOS transistors and the voltage across the output of the bridge (V_{out1} - V_{out2}) are all within the maximum rating of the device with some margin.

To insure reliable performance of an H-bridge drive circuit, the designer must insure that the device operates within the maximum ratings of the device(s) used in the circuit. One of the critical parameters to consider is the maximum voltage capability of the devices. To maintain the reliability, the voltage transients due to switching inductive loads must be maintained within the ratings of the device. Two techniques used to control the voltage transients in fast switching applications are proper bypass filtering of the power supply and snubbing the outputs to control voltage rise times. Using these two techniques the voltage transients in a DMOS bridge application can be controlled to within safe levels.

6 Revision history

Table 1. Document revision history

Date	Revision	Changes
24-Jan-2004	1	Initial release.
13-Jul-2004	2	Changed title in cover page.
07-Nov-2012	3	Minor text changes. Added references to the L6201 and L6202 devices. Revised *Equation 1*.