

HD74CBT1G126

Single FET Bus Switch

R04DS0016EJ0200 Rev.2.00 Jan 10, 2014

Description

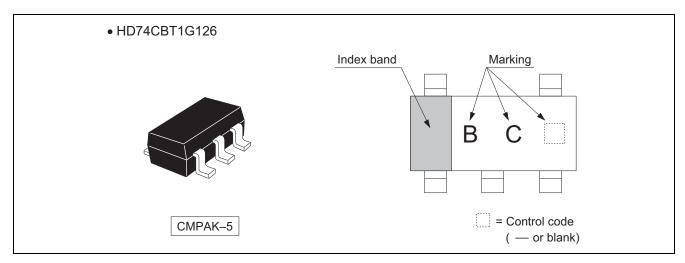
The HD74CBT1G126 features a single high-speed line switch. The switch is disabled when the output enable (OE) input is low.

Features

- Minimal propagation delay through the switch.
- 5 Ω switch connection between two ports.
- TTL-compatible input levels.
- Ultra low quiescent power.
 - Ideally suited for notebook applications.
- Ordering Information

Part Name	Package Type	Package Code (Previous code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74CBT1G126CME	CMPAK-5pin	PTSP0005ZC-A (CMPAK-5V)	СМ	E (3,000pcs / Reel)

Outline and Article Indication

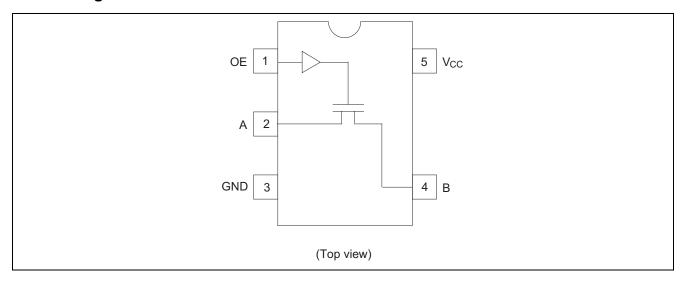


Function Table

Input OE	Function
Н	A port = B port
L	Disconnect

H: High level L: Low level

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V _{CC}	-0.5 to 7.0	V	
Input voltage range *1	VI	-0.5 to 7.0	V	
Input clamp current	I _{IK}	-50	mA	V _I < 0
Continuous output current	I _O	128	mA	$V_O = 0$ to V_{CC}
Continuous current through V _{CC} or GND	I _{CC} or I _{GND}	±100	mA	
Maximum power dissipation at Ta = 25°C (in still air) *2	P _T	200	mW	
Storage temperature	Tstg	-65 to 150	°C	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

- 1. The input and output voltage ratings may be exceeded even if the input and output clamp-current ratings are observed.
- 2. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V _{CC}	4.0	5.5	V	
Input voltage range	VI	0	5.5	V	
Output voltage range	V _{I/O}	0	5.5	V	
Input transition rise or fall rate	Δt / Δν	0	5	ns / V	$V_{CC} = 4.5 \text{ to } 5.5 \text{ V}$
Operating free-air temperature	Та	-40	85	°C	

Note: Unused or floating inputs must be held high or low.

DC Electrical Characteristics

 $(Ta = -40 \text{ to } 85^{\circ}C)$

Item	Symbol	V _{CC} (V)	Min	Typ *1	Max	Unit	Test conditions
Clamp diode voltage	V _{IK}	4.5	_	_	-1.2	V	I _{IN} = -18 mA
Input voltage	V _{IH}	4.0 to 5.5		_	_	V	
Input voltage	V _{IL}	4.0 to 5.5	_	_	0.8	V	
		4.0		14	20		V_{IN} = 2.4 V, I_{IN} = 15 mA Typ at V_{CC} = 4.0 V
On-state switch resistance *2	R _{ON}	4.5	_	5	7	Ω	$V_{IN} = 0 \text{ V}, I_{IN} = 64 \text{ mA}$
		4.5	_	5	7		$V_{IN} = 0 \text{ V}, I_{IN} = 30 \text{ mA}$
		4.5	_	10	15		$V_{IN} = 2.4 \text{ V}, I_{IN} = 15 \text{ mA}$
Input current	I _{IN}	0 to 5.5	_	_	±1.0	μΑ	V _{IN} = 5.5 V or GND
Off-state leakage current	loz	5.5	_	_	±1.0	μΑ	$0 \le A, B \le V_{CC}$
Quiescent supply current	Icc	5.5	_	_	1.0	μΑ	$V_{IN} = V_{CC}$ or GND, $I_O = 0$ mA
Increase in I _{CC} per input *3	Δlcc	5.5	_	_	2.5	mA	One input at 3.4 V, other inputs at V _{CC} or GND

Notes: For condition shown as Min or Max use the appropriate values under recommended operating conditions.

- 1. All typical values are at V_{CC} = 5 V (unless otherwise noted), Ta = 25°C.
- 2. Measured by the voltage drop between the A and B terminals at the indicated current through the switch. Onstate resistance is determined by the lower voltage of the two (A or B) terminals.
- 3. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Capacitance

 $(Ta = 25^{\circ}C)$

	Item	Symbol	V _{cc} (V)	Min	Тур	Max	Unit	Test conditions
Cor	ntrol input capacitance	C _{IN}	5.0	_	3	_	pF	V _{IN} = 0 or 3 V
Inpu	ut / output capacitance	C _{I/O (OFF)}	5.0	_	5	_	pF	$V_O = 0$ or 3 V, OE = V_{CC}

Note: This parameter is determined by device characterization is not production tested.

Switching Characteristics

 $(Ta = -40 \text{ to } 85^{\circ}C)$

 $V_{CC} = 4.0 \text{ V}$

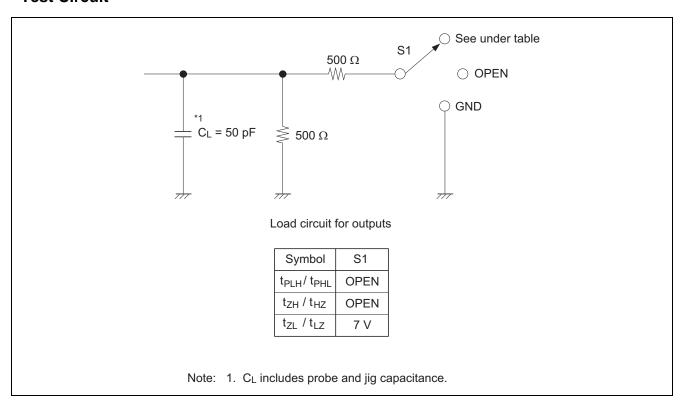
Item	Symbol	Min	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Propagation delay time *1	t _{PLH} t _{PHL}		0.35	ns	$C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	A or B	B or A
Enable time	t _{ZH}	_	5.5	ns	$C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	OE	A or B
Disable time	t _{HZ}		4.5 4.5	ns	$C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	OE	A or B

 $V_{CC} = 5.0 \pm 0.5 \text{ V}$

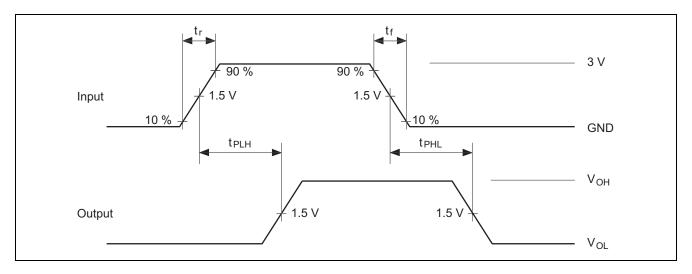
Item	Symbol	Min	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Propagation delay time *1	t _{PLH} t _{PHL}	_	0.25	ns	$C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	A or B	B or A
Enable time	t _{ZH}	1.6	4.9	ns	$C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	OE	A or B
Disable time	t _{HZ}	1.0 1.0	4.2 4.8	ns	$C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	OE	A or B

Note: 1. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

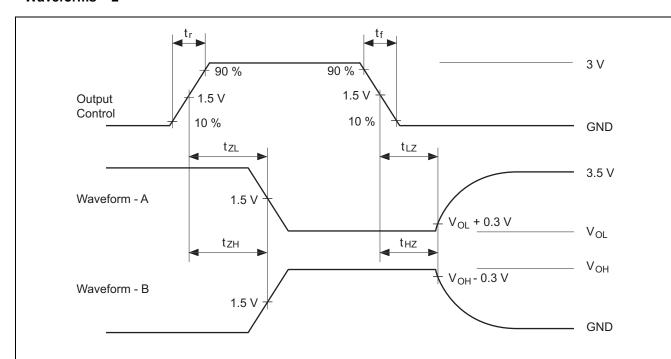
Test Circuit



Waveforms - 1



Waveforms - 2

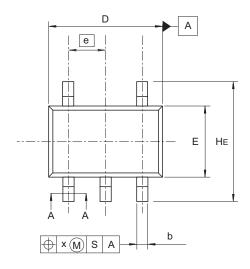


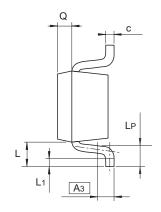
Notes: 1. All input pulses are supplied by generators having the following characteristics : PRR \leq 10 MHz, Z_O = 50 $\Omega,\,t_{f}\leq$ 2.5 ns, $t_{f}\leq$ 2.5 ns.

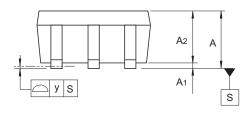
- 2. Waveform A is for an output with internal conditions such that the output is low except when disabled by the output control.
- 3. Waveform B is for an output with internal conditions such that the output is high except when disabled by the output control.
- 4. The output are measured one at a time with one transition per measurement.

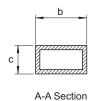
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
SC-88A	PTSP0005ZC-A	CMPAK-5 / CMPAK-5V	0.006









Reference	Dimensions in millimeters					
Symbol	Min	Nom	Max			
Α	8.0		1.1			
A ₁	0		0.1			
A ₂	8.0	0.9	1.0			
A_3		0.25				
b	0.15	0.22	0.3			
С	0.1	0.13	0.15			
D	1.8	2.0	2.2			
E	1.15	1.25	1.35			
е	_	0.65	_			
HE	1.8	2.1	2.4			
L	0.3	_	0.7			
L ₁	0.1	_	0.5			
LP	0.2		0.6			
Х			0.05			
y Q		_	0.05			
Q	_	0.25	_			

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Renesas Electronics America Inc. 2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A. Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited 1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K Tel: +44-1628-651-709, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd. 7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China Tel: +86-10-2035-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 LanGao Rd., Putuo District, Shanghai, China
Tel: +86-21-2226-088, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 161F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd. 13F, No. 363, Fu Shing North Road, Taipei, Taiv Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd. 80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949 Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd. 12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea Tel: +82-2-558-3737, Fax: +82-2-558-5141

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