BLF2425M9L30; BLF2425M9LS30

Power LDMOS transistor

Rev. 1 — 3 June 2015 Objective data sheet

1. Product profile

1.1 General description

30 W LDMOS power transistor for Industrial, Scientific and Medical (ISM) applications at frequencies from 2400 MHz to 2500 MHz.

The BLF2425M9L30 and BLF2425M9LS30 are drivers designed for high power CW applications and are assembled in a high performance ceramic package.

Table 1. Typical performance

RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
CW	2450	32	30	18.5	61

1.2 Features and benefits

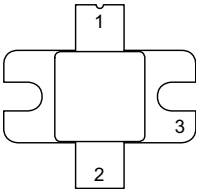
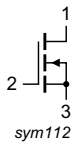
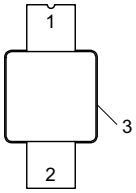
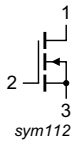
- High efficiency
- High power gain
- Excellent ruggedness
- Excellent thermal stability
- Integrated ESD protection
- Designed for broadband operation (2400 MHz to 2500 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Industrial, scientific and medical applications in the frequency range from 2400 MHz to 2500 MHz

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF2425M9L30 (SOT1135A)			
1	drain		
2	gate		
3	source [1]		
BLF2425M9LS30 (SOT1135B)			
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF2425M9L30	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT1135A
BLF2425M9LS30	-	earless flanged ceramic package; 2 leads	SOT1135B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j\text{-}case)}$	thermal resistance from junction to case	T_{case} = 50 °C; P_L = 30 W [1]	0.9	K/W

[1] When operated with a CW signal.

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.3 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 30 mA	1.4	1.9	2.4	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	6.2	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 30 mA	-	0.264	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 1 A	-	0.41	0.76	Ω

Table 7. RF characteristics

Test signal: CW at f = 2450 MHz; RF performance at V_{DS} = 32 V; I_{Dq} = 20 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 30 W	17	18.5	-	dB
RL_{in}	input return loss	P_L = 30 W	-	–8	–6	dB
η_D	drain efficiency	P_L = 30 W	57	61	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The BLF2425M9L30 and BLF2425M9LS30 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 20 mA; P_L = 30 W (CW); f = 2450 MHz.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data. Typical values unless otherwise specified.

f	Z_S	Z_L
(MHz)	**(Ω)**	**(Ω)**
2400	9.0 – 12.5j	12.0 – 2.0j
2450	9.1 – 17.9j	10.4 – 4.3j
2500	16.0 – 17.3j	10.3 – 4.2j

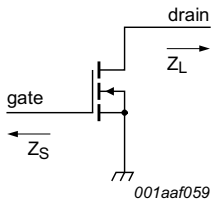
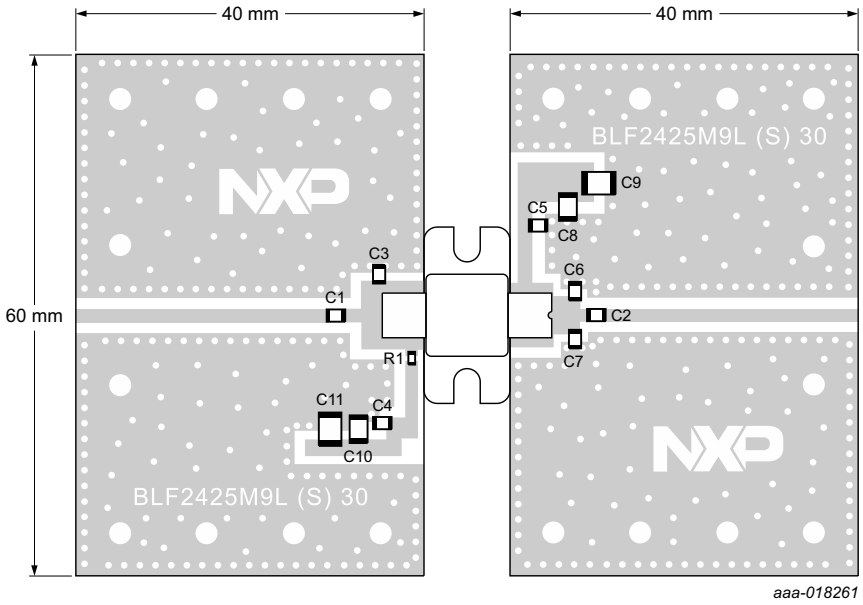


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Duroid 6035HTC; height = 0.762 mm.

See Table 9 for a list of components.

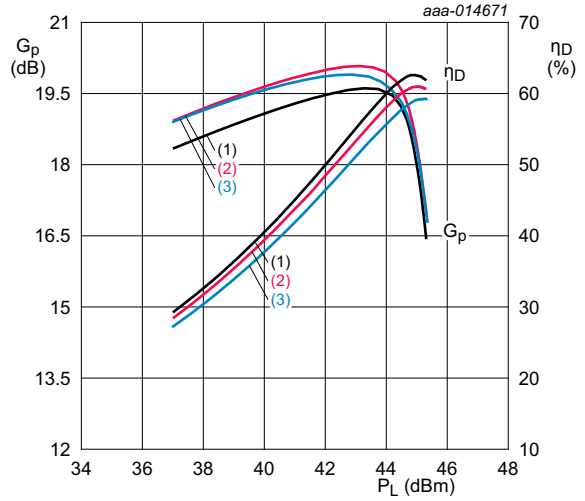
Fig 2. Component layout

Table 9. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C2, C4, C5	multilayer ceramic chip capacitor	15 pF	ATC100A150FT150XT
C3	multilayer ceramic chip capacitor	0.3 pF	ATC100A0R6BT150XTV
C6, C7	multilayer ceramic chip capacitor	0.8 pF	ATC100A0R8BT150XTV
C8, C10	multilayer ceramic chip capacitor	100 nF	GRM21BR71H104KA01L
C9, C11	multilayer ceramic chip capacitor	4.7 μF	GRM32ER71H475KA88L
R1	SMD resistor	9.1 Ω	SMD 0603

7.4 Graphical data



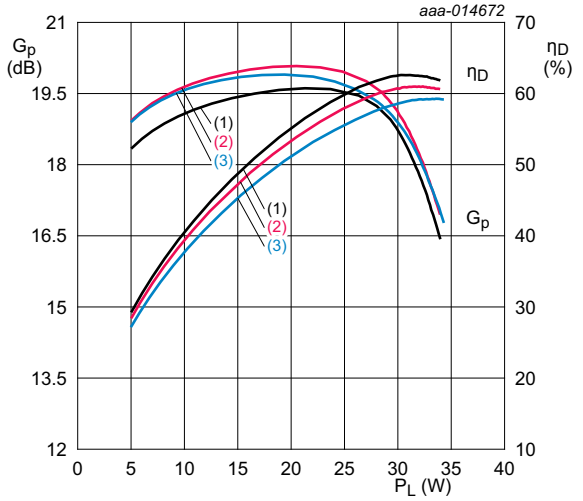
V_{DS} = 32 V; I_{Dq} = 20 mA.

(1) f = 2400 MHz

(2) f = 2450 MHz

(3) f = 2500 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



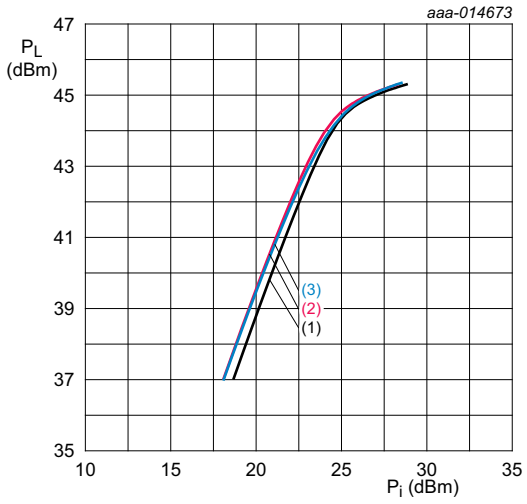
V_{DS} = 32 V; I_{Dq} = 20 mA.

(1) f = 2400 MHz

(2) f = 2450 MHz

(3) f = 2500 MHz

Fig 4. Power gain and drain efficiency as function of output power; typical values



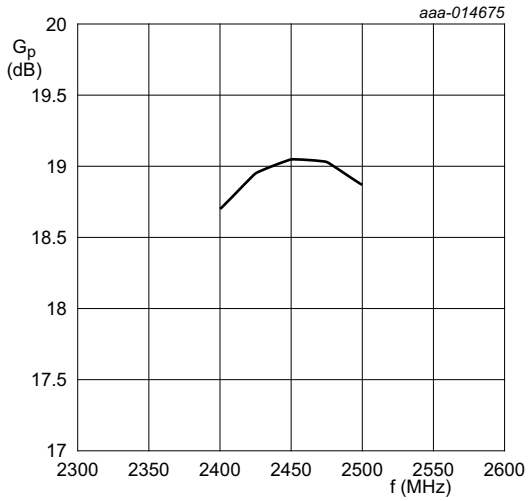
V_{DS} = 32 V; I_{Dq} = 20 mA.

(1) f = 2400 MHz

(2) f = 2450 MHz

(3) f = 2500 MHz

Fig 5. Output power as a function of input power; typical values

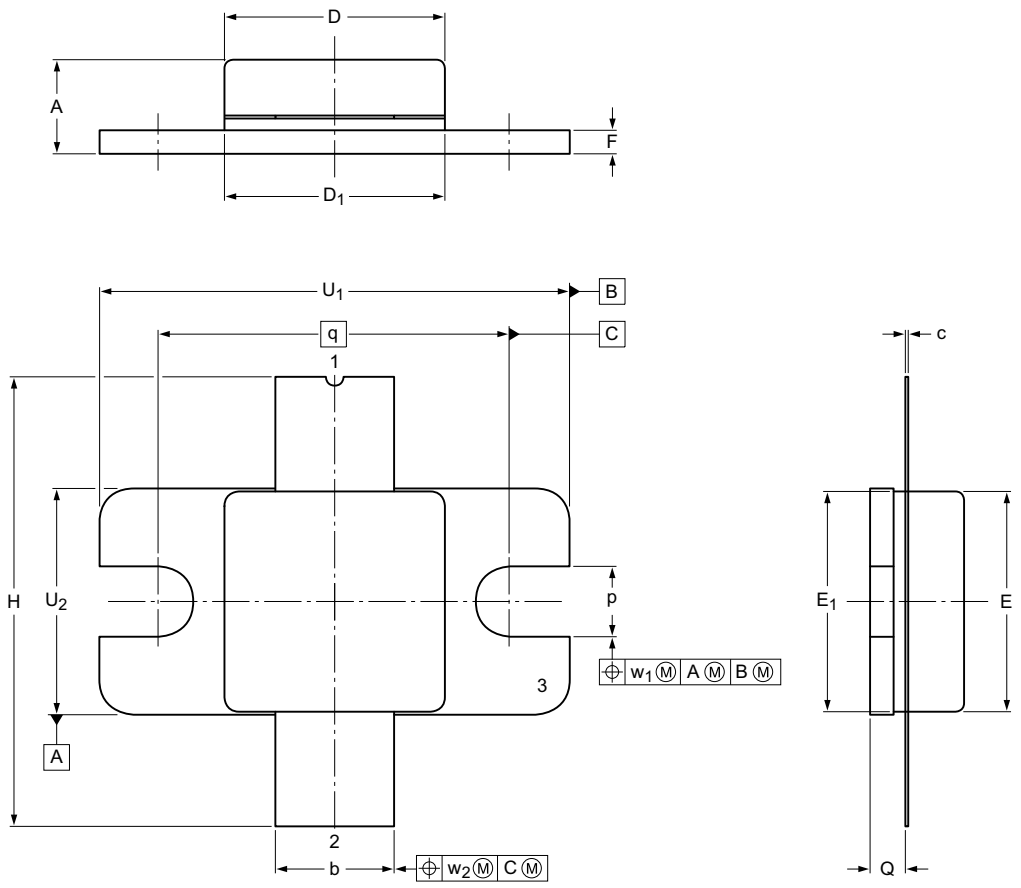


V_{DS} = 32 V; I_{Dq} = 20 mA; P_L = 30 W.

Fig 6. Power gain as a function of frequency; typical values

8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT1135A**



Dimensions

Unit[1]		A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	max	4.65	5.26	0.18	9.65	9.65	9.65	9.65	1.14	19.94	3.30	1.70		20.45	9.91		
	nom												15.24			0.25	0.51
	min	3.76	5.00	0.10	9.40	9.40	9.40	9.40	0.89	18.92	2.92	1.45		20.19	9.65		
inches	max	0.183	0.207	0.007	0.38	0.38	0.38	0.38	0.045	0.785	0.130	0.067		0.805	0.39		
	nom												0.6			0.01	0.02
	min	0.148	0.197	0.004	0.37	0.37	0.37	0.37	0.035	0.745	0.115	0.057		0.795	0.38		

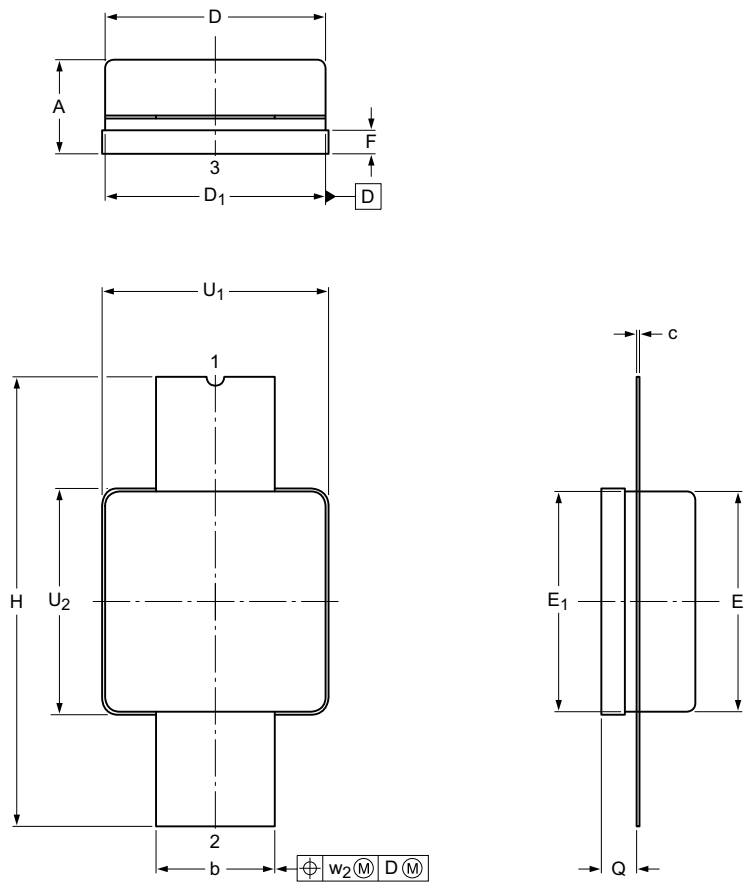
Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1135a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1135A						~~09-10-12~~ 09-12-14

Fig 7. Package outline SOT1135A

Earless flanged ceramic package; 2 leads **SOT1135B**



Dimensions

Unit[1]		A	b	c	D	D_1	E	E_1	F	H	Q	U_1	U_2	w_2
mm	max	4.65	5.26	0.18	9.65	9.65	9.65	9.65	1.14	19.94	1.70	9.91	9.91	0.51
	nom													
	min	3.76	5.00	0.10	9.40	9.40	9.40	9.40	0.89	18.92	1.45	9.65	9.65	
inches	max	0.183	0.207	0.007	0.38	0.38	0.38	0.38	0.045	0.785	0.067	0.39	0.39	0.02
	nom													
	min	0.148	0.197	0.004	0.37	0.37	0.37	0.37	0.035	0.745	0.057	0.38	0.38	

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1135b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1135B						~~09-10-12~~ 09-12-14

Fig 8. Package outline SOT1135B

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF2425M9L30_M9LS30 v.1	20150603	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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